

VHDL-AMS Model for Switched Resistor $\Delta\Sigma$ Modulator

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Abstract: This paper introduces modeling of switched resistor (SR) $\Delta\Sigma$ modulator in analog mixed signal (AMS). Such design consists of 2nd order single bit SR $\Delta\Sigma$ modulator with dissipated power of 0.65mW and 3rd order digital decimation filter. SR technique is better than the other techniques for simplicity, less noise and low power dissipated in hardware realization. The proposed digital filter design consists of a third order Cascaded integrator Comb filter (CIC). The system occupies a small silicon area due to no multipliers used. Our design and simulation are implemented using Mentor Graphics VHDL-AMS tools. The final result has resolution of 12-Bit using 32 Oversampling ratio.

Keywords: Switched resistor, Delta Sigma modulator, Cascaded integrator Comb filter

1. Introduction

Most of the signals in their natural form are Analog, but it is really difficult to store, transmit or process signal in analog form hence it is often required to convert signal in digital form by using some type of device called analog to digital converter (ADC) [1].

ADC is preferred to be designed in low power and high speed in order to achieve long battery life for portable system. Also minimum number of battery cells reduces the volume and weight of the system [2].

There are different types of analog to digital conversion techniques available today, each having its own advantages and disadvantages. ADCs are categorized into two types namely Nyquist rate converters and oversampling converters depending on the sampling rate. Table 1 shows the difference between Nyquist rate converters and oversampling converters. $\Delta\Sigma$ ADCs come in oversampling converters group. Over sampling converters reduce the requirements of analog circuitry at expense of faster and more complex digital circuitry [3].

Table 1: Nyquist and Oversampling converters

Type	Sampling frequency	Noise power	Anti-aliasing filter
Nyquist converter	$f_s=2f_m$	$\frac{\Delta^2}{12}$	narrow
Oversampling converter	$f_s=OSR*2f_m$	$\frac{\Delta^2}{(12 \times OSR)}$	wide

This paper is organized as follows: Section 2 describes VHDL-AMS modeling. In Section 3 describes SR $\Delta\Sigma$ modulator and digital filter. Experimental results are discussed in Section 4. Conclusion is introduced in Section 5.

2. VHDL-AMS Modeling

VHDLAMS models can support nature types for several physical domains. Natural types are properties of conservative nodes (also referred to as ports or terminals) of models. At least one specific nature exists for each domain.

An across and a through quantity is associated with each nature [4]. The following Table 2 links the across and through quantities for each nature type.

Table 2: Linking the across and through quantities for each nature type

Nature	Across	Through
Electrical	Voltage	Current
Fluidic	Pressure	Flow rate
Magnetic	Magneto motive force	Magnetic flux
Translational	Displacement	Force
Rotational	Angle	Torque
Thermal	Temperature	Heat flow

SystemVision provides simulation capability for mixed-signal and mixed-technology (multi-physics) designs. Models and modeling techniques from VHDL-AMS, VHDL, C, and SPICE formats are supported. [5]. For example a VHDL-AMS code of capacitor included in SystemVision library is shown in Fig.1.

```

library IEEE;
use IEEE.electrical_systems.all;

entity capacitor is
    generic (
        cap          : capacitance;    -- Capacitance [F]
        v_ic         : real := real'low; -- Initial voltage (activated by
        );                               -- IF statement below) [V]
    port (
        terminal p1, p2 : electrical);
end entity capacitor;

-- Ideal Architecture (I = C * dV/dt)
-- Includes initial condition
-- -----
architecture ideal of capacitor is
    quantity v across i through p1 to p2;
begin
    if domain = quiescent_domain and v_ic /= real'low use
        v == v_ic;
    else
        i == cap * v'dot;           -- Fundamental equation
    end use;
end architecture ideal;

-- Copyright (c) 2001 Mentor Graphics Corporation
    
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Figure 1: VHDL-AMS code of capacitor

3. SR $\Delta\Sigma$ ADC Structure

In general $\Delta\Sigma$ ADCs need relatively imprecise analog circuits and digital decimation filtering. The sigma-delta ADC works on the principle of $\Delta\Sigma$ modulation. The sigma-delta modulation is a process for encoding high-resolution

signals into lower resolution signals using pulse-density modulation. It samples the input signal at a rate much higher than the Nyquist rate.

Fig.2 shows the block diagram of a $\Delta\Sigma$ ADC. It consists of a $\Delta\Sigma$ ADC modulator and a digital decimation filter. The modulator is realized in analog technique to produce a single bit stream and a digital Decimation filter to achieve a multi bit digital output [3].

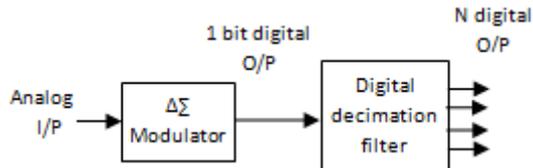


Figure 2: $\Delta\Sigma$ ADC block diagram

3.1 2nd Order SR $\Delta\Sigma$ Modulator

The second order Sigma-Delta modulator consists of two summing integrator, a 1-bit quantizer and a 1-bit D/A converter in a feed-back structure. The modulator output has only 1-bit (two levels) of information, i.e., 1 or -1 [3].

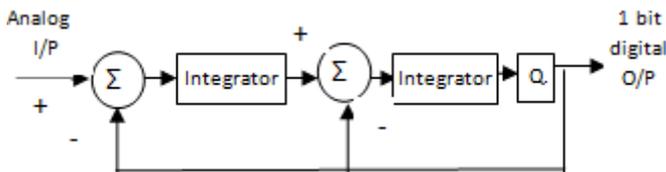


Figure 3: 2nd order $\Delta\Sigma$ modulator block diagram

Analog filters (ex. integrators) are key building blocks in many systems. Like many other analog circuits, traditional filters are adversely affected by a low supply voltage. One of the most fundamental low-voltage issues in analog design is the reduction in available signal swing. To achieve the same dynamic range as their high-voltage counterparts, low-voltage circuits must achieve better noise and distortion performance. This is difficult because low-voltage operation will increase the nonlinearity, leading to more distortion. Conventional switched-capacitor (SC) filters have difficulty working at low supply voltages because of the floating switch in the signal path.

Continuous-time (CT) filters are also strongly affected by a low supply voltage. One of the most critical issues in integrated CT filters is the corner frequency deviation caused by variations in process, voltage and temperature.

To suppress this time-constant variation, a SR filter (integrator) is often used.

The tuning range will be changed by varying duty cycle of the clock as stated in eq. (1) [6].

$$R_{eq} = \frac{R_{on}}{D} \quad (1)$$

The order of modulator is determined by the order of used integrator.

Then, the using SR technique, circuit complexity is reduced, and no need to change the topology. Moreover the nonlinearity is reduced [7]. Fig.4 Shows a simple SR

integrator used for proposed $\Delta\Sigma$ Modulator and Fig.5 shows its simulation result.

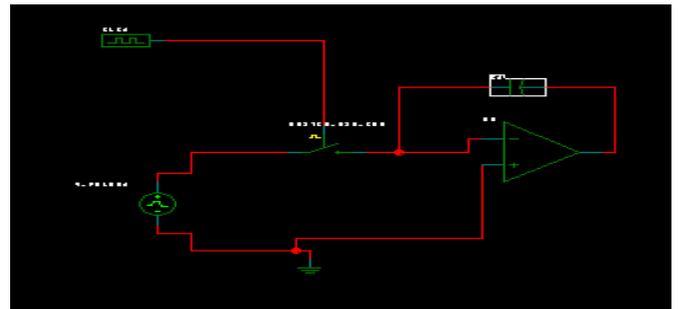


Figure 4: SR integrator circuit

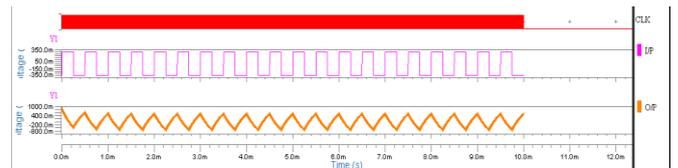


Figure 5: SR integrator simulation results

The quantizer in Fig.3 is actually a comparator if single bit modulator is used. The comparator is coded in Spice and then the code is imported to SystemVision. Both the differential node and integrator is mapped in this work as a SR summing integrator as shown in Fig.6.

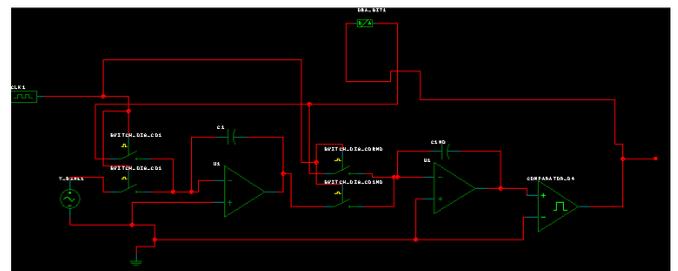


Figure 6: 2nd order SR $\Delta\Sigma$ modulator circuit

It is clearly evident that the output (single bit) is pulse width modulated according to the input sine wave. The number of 1's increases at the positive peak of the input sine wave and the no of 0's are more at the negative peak. There are equal number of 1's and 0's when the input signal is at zero amplitude, which is the expected response of a Sigma Delta Modulator [8]. Fig.7 shows the output of 2nd order single bit SR $\Delta\Sigma$ modulator with OSR of 32 at 2 kHz sine wave input. The power dissipation of modulator is 0.65 mW by SystemVision.

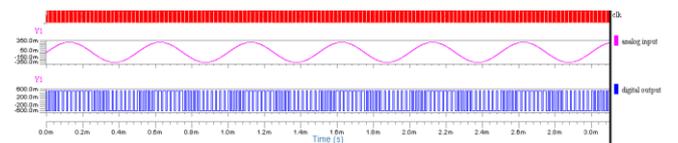


Figure 7: 1st order SR $\Delta\Sigma$ modulator circuit time domain simulation results

The output bit stream is applied to MATLAB to obtain PSD as shown in Fig. 8. The resulted SNDR is 51.13 dB.

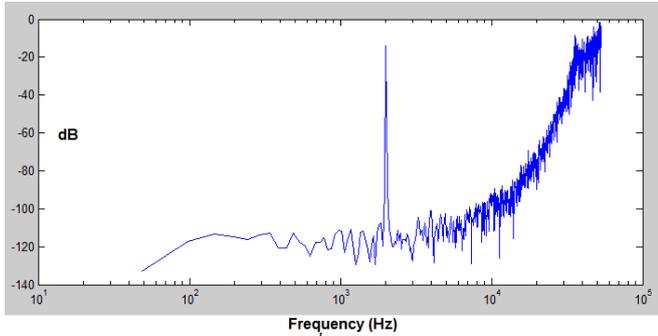


Figure 8: PSD of 2nd order SR $\Delta\Sigma$ modulator

3.2 Digital filter and Decimation

The main objective of digital decimation filter is to remove out of band quantization noise, increase resolution bits, and down sampling. The 1-bit modulator stream is digitally filtered to obtain an N-bit representation of the analog input. In simplified terms the 1-bit modulator stream is accumulated over (K) sampling cycles and divided by (K), where (K) is the oversampling ratio. This yields a decimated value which is the average value of bit stream from the modulator.

A preferred decimation filter can be realized using cascaded integrator comb filter (CIC) with transfer function given by eq. (2).

$$H(z) = \left(\frac{1 - z^{-K}}{1 - z^{-1}} \right)^L \quad (2)$$

Where L is the filter order, in this work L=3 for 2nd order modulator.

There is much architecture for implementing CIC filter such as polyphase structure, non-recursive structure, and IIR-FIR structure.

The IIR-FIR structure provides the lowest area by increasing oversampling ratio compared with others [9]. So in this paper the IIR-FIR is chosen.

From eq. (2), the numerator represents the transfer function of a differentiator and denominator represents transfer function of integrator.

A simple block diagram of CIC that follows eq. (2) is shown in Fig.9

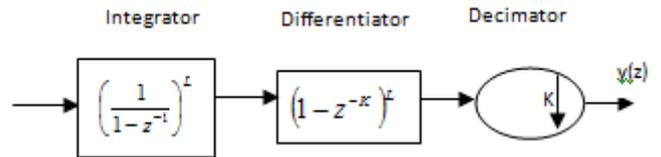


Figure 9: Direct CIC block diagram

The differentiator circuit needs K (oversampling ratio) delay elements, which are implemented using registers. The number of delay elements increases as oversampling ratio will increase, and as well the number of registers bits that are used to store the data. This type of implementation becomes Complex and requires more area as we go for higher order and higher sampling rates. This problem can be overcome by implementing a decimation stage between the integrator and Differentiator stages as shown in Fig.10 [10].

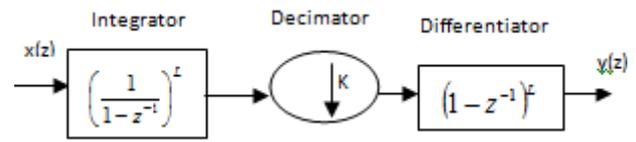


Figure 10: Modified CIC block diagram

The one bit digital integrator and differentiator is a combination of delay element and a simple full adder, as shown in Fig.11 a & b respectively [11].

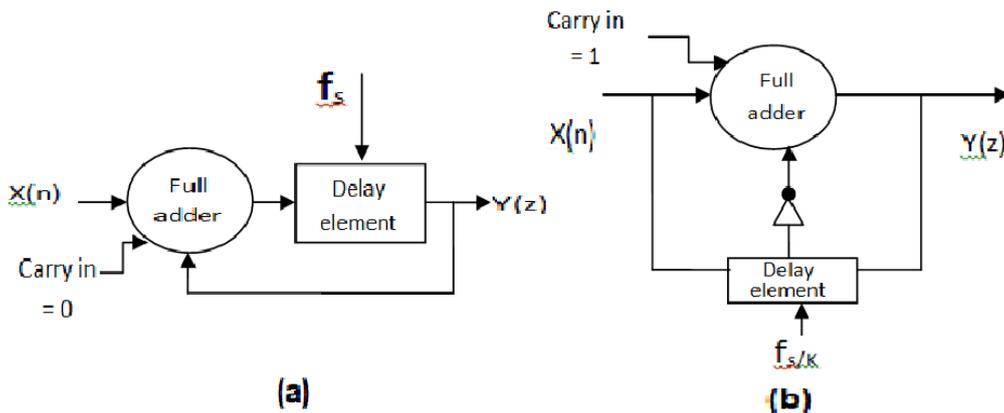


Figure 11: One bit digital integrator (a) and differentiator (b)

A clock divider is needed for both down sampling and differentiator. By operating the differentiator at lower frequencies, a reduction in the power consumption is achieved.

To generate the required clock output for the differentiator of the CIC filter. As $32 = 2^5$, N=5, we need 5-stage T-flip flops to achieve a frequency division by 32. Whenever the input and output of a T-flip flop are given as inputs to an AND

gate, only the ON time of the input clock is transmitted to the output. The output of the AND gate remains at logic '1' during this ON time only [10].

T-flip flop is not included in SystemVision library; it's only JK- flip flop. T- flip flop is created from JK- flip flop By inverting K by J and connecting Q' to J. Fig.12 Shows the clock divider circuit and its simulation wave forms are shown in Fig.13.

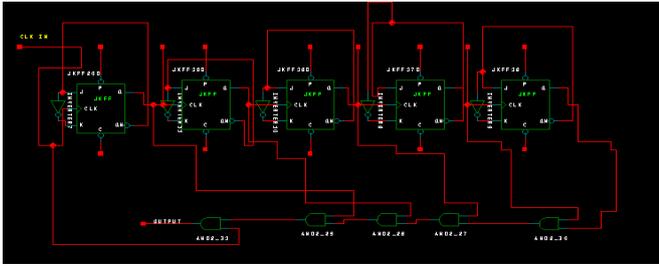


Figure 12: Clock divider by 32 circuit

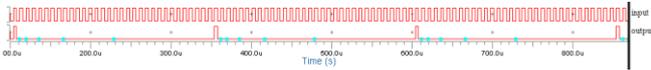


Figure 13: clock divider by 32 circuit wave forms

A single integrator is unstable due to the single pole at $z=1$. There is a chance of register overflow and data may be lost. To avoid this problem of register overflow, 2's complement coding scheme is used. By using the 2's complement number representation, the data will not be lost due to register overflow as long as the register used to store the data is long enough to store the largest word given by $K \times 2^N$. Here N is the number of input bits to that particular integrator stage. Internal word width (W) needed to ensure not run time overflow is estimated from eq. (2) [10].

$$W = (1 \text{ sin bit}) + (\text{Number of input bits}) + (\text{Number of stages "filter order L"}) \quad (2)$$

$$\log_2(\text{Decimator factor})$$

In our case $W=17$. Then a coder 2's complement circuit is needed to convert a single bit of modulator output to 17 2's complement bits as illustrated in table 3.

Table 3: ADCs features

I/P single bit	O/P 17 bits 2's complement
0	00000000000000001
1	11111111111111111

The circuit that responsible for existing above table is shown In Fig.14.

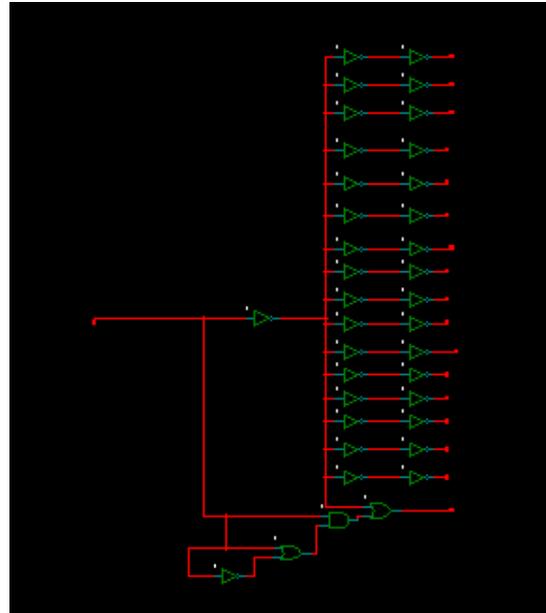


Figure 14: 17 bit 2's complement coder

The overall digital filter was implemented as in Fig.15. Note that down samplers were realized using D flip-flops clocked at the lower frequency [11].

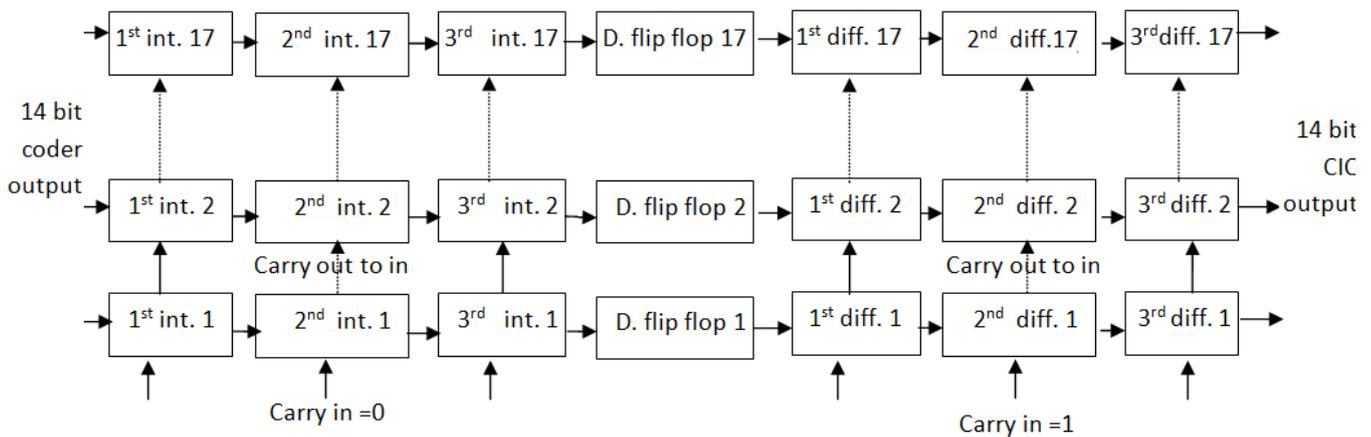


Figure 15: The overall CIC filter

4. Experimental Results

The output of the CIC is a two's complement 17-bit data. This data has to be converted into binary form and also the least significant bits should be dropped in order to achieve the required resolution as given in eq. (3) & (4).

$$N_{final} = N_{i/p} + N_{inc} \quad (3)$$

$$N_{inc} = \frac{50 \log K - 12.9}{6.02} \quad (4)$$

In equation (3)&(4), N_{inc} is the increase in resolution and K

is the oversampling ratio. So, for $K=32$, the output resolution achieved is 12 bits. Hence, we select 13-Bits (1-sign bit +12 resolution bits) from the 17-bit output of the differentiator and drop the lower 4 bits [10].

The applied sine wave input to the ADC is 0.6 Vp-p, 2 kHz with a bandwidth of 4 kHz and the applied oversampling clock frequency is 256 kHz.

In the first case, since the output frequency is at 8 kHz and the input signal is at 2 kHz, there exist four output data words in one clock cycle of the input signal. Fig.16 shows

Experimental results showing the four waveforms for digital output codes.

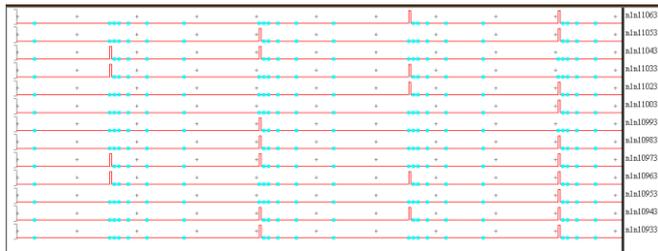


Figure 16: ADC O/P

$$1LSB = \frac{V_{FSR}}{2^N} \quad (5)$$

Substituting the previous value in equation (5) the resulted value is 0.0000732. The output of the CIC filter is in 2's complement form. The desired 13-Bits output is converted from 2's complement to equivalent binary form and actual analog voltage (by multiplying 1 LSB with decimal value). Table 4, which shows the 13-Bit 2's complement output, binary output, its decimal equivalent, and the actual analog voltage.

Table 4: O/P results

2's complement	Binary form	Decimal value	Analog equivalent
0011000011000	0011000011000	1560	0.113
0110001110011	0110001110011	3187	0.232
1001100001010	0110011110110	-3318	-0.242
1100110111111	0011001000001	-1610	-0.117

It can be observed that alternative outputs have approximately same magnitude.

5. Conclusion

A SR 2nd order $\Delta\Sigma$ modulator and 3rd order CIC decimation filter have been designed using VHDL_AMS Mentor Graphics system vision tools. The SR ADC has been obtained resolution 12-Bit using 32 Oversampling ratio. The SR integrator used in $\Delta\Sigma$ modulator offers component reduction and tunable ability. The power dissipated of 2nd order SR $\Delta\Sigma$ modulator is 0.65mW.

References

[1] Prerna Gupta, Head & Prof. Rita Jain, "Simulation & Analysis of Sigma-Delta A/D Converter using VHDL-AMS" International Journal of Scientific Engineering and Technology, Volume No.1, Issue No.2, April 2014

[2] Bharti D.Chaudhari, Priyesh P.Gandhi, "A 1.8V 8-bit 100-MS/s Pipeline ADC in 0.18 μ m" International Journal of Science and Research (IJSR), volume 3 Issue 5, May 2014.

[3] Dr. Khalid K. Mohammed, "Design and Implementation of Decimation Filter for 15-bit Sigma-Delta ADC Based on FBGA" International Journal of Engineering and Innovative Technology (IJEIT) Volume 3, Issue 10, April 2014

[4] <http://www.hamster-ams.com>.

[5] <http://www.mentorgraphic.com>.

[6] eter Kurahashi "Duty-cycle Controlled Switched Resistor Technique for Continuously Tunable, Low-Voltage Circuit", Doctor Thesis, Oregon State University, Jun 2010.

[7] A. Osman " Design of Low Power Sigma Delta Modulator in VLSI", Master Thesis, Mansoura University, 2010.

[8] Anand K Chamakura, " IDDQ Testing of A CMOS First Order SIGMA-DELTA Modulator of an 8-BIT Oversampling ADC", Master thesis, Louisiana State University, August 2004.

[9] Bibin John, Fabian Wagner and Wolfgang H. Krautschneider", Comparison of Decimation Filter Architectures for a Sigma-Delta Analog to Digital Converter", Institute of Nanoelectronics, Hamburg University of Technology, Germany.

[10] Hemalatha Mekala, " Third Order CMOS Decimator Design For Sigma Delta Modulator", Louisiana state university, agricultural and mechanical college, December 2009.

[11] Özge Gürsoy, Orkun Sağlamdemir, Mustafa Aktan, Selçuk Talay, Günhan Dündar," Low-Power Decimation Filter Architectures For SIGMA-DELTA ADC's", Boğaziçi University, Department of Electrical and Electronics Engineering,, Bebek, Istanbul, Turkey