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Implementation of Control Area Network with Flexible Data Rate Protocol Controller

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Abstract: ***Control Area Network (CAN) is widely used in automotive networks with the bit rate of 1MBPS which is a lower bandwidth with other protocols. To unblock the progress of CAN, Bosch introduced Control Area Network with Flexible Data rate (CANFD) Protocol. CANFD protocol is a robust with longer messages transmission in short time and these messages are transmitted with high security. This paper presents the implementation of CANFD Controller with the bit rate of 2MBPS .Implemented in Spartan FPGA xa7a100t-2Icsg324.***

Keywords: Bit Stream Processor, Bit Timing Processor, Error, Frame

1. Introduction

In vehicular systems there was a cumbersome wiring replaced by Electronic Control Units (ECUs) and there is a need of communication between these units. For that a serial communication protocol was developed in 1981 by Robert Bosch named as Controller Area Network CAN Protocol. Bosch published a specification in 1991[1]. With the impact of vlsi technology, ECU nodes are increased which effects the bandwidth of CAN protocol. CANFD impede the CAN bandwidth limitation example processing the multiple CAN frames with the single CANFD frame. CANFD [11]keeps most of the software, hardware especially physical layer of CAN.

CANFD improves the bandwidth limitation of CAN by using two bit rates one for arbitration phase with long bit time and data phase with short bit time . The bit timings of CANFD protocol are defined by time configuration registers. CANFD transmits a high data payload of 64bytes to secure long frames CANFD uses different CRC sequences.

2. Literature Survey

Many industrial users and manufacturers grouped then introduced the CAN in automation in 1992. In automotive systems there is a high degree of electromagnetic interference disturbs the data transported between transmitter and receiver. The specification [1] gave the error detection mechanisms which are firstly stated in [2]. J.Charzinskhi [3] gave the analytical model for the undetectable errors at receivers he explained the probability of error at receiver using a two-state symmetric binary channel model.

Analytical approach is a theoretical method so one author [4] conducts experiment on the occurrence of undetectable errors with a simulation approach and compares the result with the analytical approach [3]. G.Cena et al.[5] proposed a new protocol Star CAN for the extension of CAN network or improve the bit rate without changing the degree of compatibility of CAN. RyoKurachi et al.[6] developed a new protocol named as Scalable CAN protocol which is based on existing CAN[1]. In this paper, CAN challenges were explained and proposed a new protocol with new collision resolution algorithm.

Flex Ray, LIN are other automotive protocols. FlexRay [7] gave a data rate of 10 Mbps this is a complex protocol which is of star topology and a high cost embedded network standard. Local Interconnect Network LIN [8] bus is a simple protocol which is a low cost embedded network standard. Originally CAN was available with single chips now CAN is placed as interface in many FPGAs so CAN is used in many applications like [9][10].

How a CANFD achieves high data rate with increase of data payload is explained by F.Hartwich [12]. Dr.Arhur Mutter [13] introduces a metric phase margin which is used to assess the robustness of CANFD bus.

3. CANFD Implementation

The implementation of Control Area Network with Flexible Data rate protocol follows the CAN implementation with additional contol bits. CANFD uses a Non Retun to Zero(NRZ) coding The different CANFD frame formats are Data frame, Error frame, Overload frame and Inter frame .

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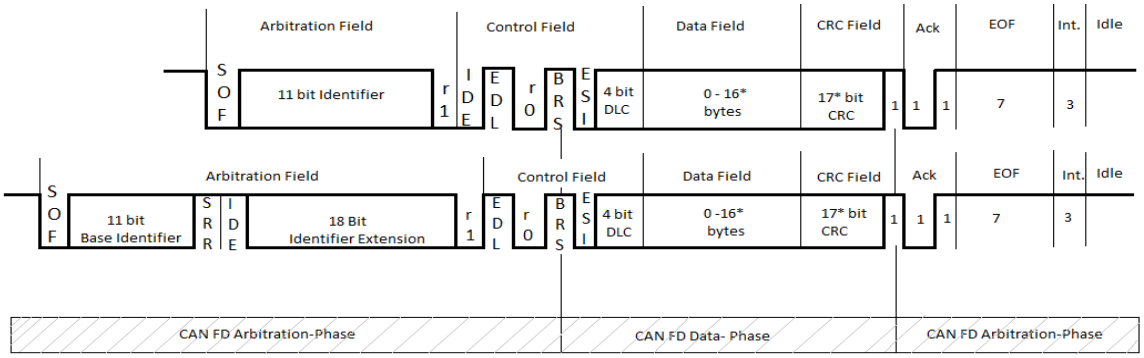

Figure 3.1: CANFD Data Frame Format with 11 bit identifier and with 29 bit identifier

The new bits in CANFD are
EDL: Extended Data Length indicates transmission and receive of a high data payload.
r1,r0: reserved bits transmitted as a dominant.
BRS: Bit Rate Switch indicates whether switch to short bit timing or not in Data phase.
ESI: The error state in transmission of this protocol is indicated by this bit.
DLC with extended bytes as

Table 1: Extended Data Length.

DLC	1001	1010	1011	1100	1101	1110	1111
Byte	12	16	20	24	32	48	64

The security of data is important one when transmission and receive of data. In CANFD protocol data payload can be up to 64 bytes for that different Cyclic Redundancy Checks(CRC) polynomials CRC_17= $x^{17}+x^{16}+x^{14}+x^{13}+x^{11}+x^{6}+x^{4}+x^{3}+x^{1}+1$ CRC_21= $x^{21}+x^{20}+x^{13}+x^{11}+x^{7}+x^{4}+x^{3}+1$are proposed in [14] for different data payloads. The acknowledgment field of CANFD protocol contains ack field and ack delimiter the bus transmitter sends recessive in ack field and if there is correct reception of frame receiver sends a dominant bit else sends recessive bit at that time resynchronization takes, ack delimiter is always recessive.

Error flag (six dominant)and error delimiter(eight recessive) are two fields of Error frame. This frame can be send only in error is detected by receiver. The Over load frame consists overload flag(six dominant) and overload delimiter(eight recessive) fields this frame is send when the last bit of end of frame of data frame or error delimiter or overload delimiter. Inter frame is send in between of a frame is send consecutively. This frame contains three recessive bits as a intermission field if last bit is dominant a hard synchronization will happens.

Error Meachanisms in CANFD are bit error bus always monitors each bit of control field which are a fixed one if recessive comes as a dominant bit error is high and resynchronization will happens. CRC error compares the generated and calculated CRC's . Acknowledgement error detected in receive of dominant bit in receive side when transmitter sends a recessive bit. Stuff error shall be detected while a consecutive ones and zeros are in data and crc sequence.Form error detected when fixed bit patterns contains illegal bits.

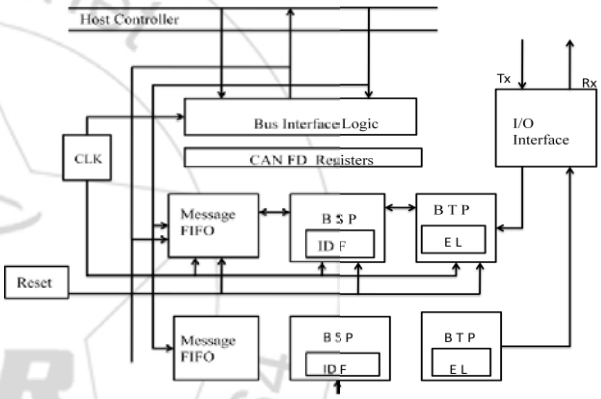

Figure 3.2: CANFD block view

The CANFD block view is shown in Fig3.2. The Bit Timing Processor [BTP] is a block here how hard synchronization and resynchronization of frames is done. When errors are come how the bus will respond is done here in Error logic EL. The synchronization specifications like baud rate pre scalar, time segment values are given by CANFD registers.

In the Bit Stream Processor BSP block, the bus transition happens . Identifier filtering IF is choosing a priority node done by acceptance masking. A message FiFo is used for storing data . CANFD is working below 100MHZ which is a low peripheral so that APB bus interface is used to communicate with host. CAN transceiver is used as I/O interface.The simulated waveforms of transmission of 12 bytes of data.

Figure 3.3: Simulated Waveform

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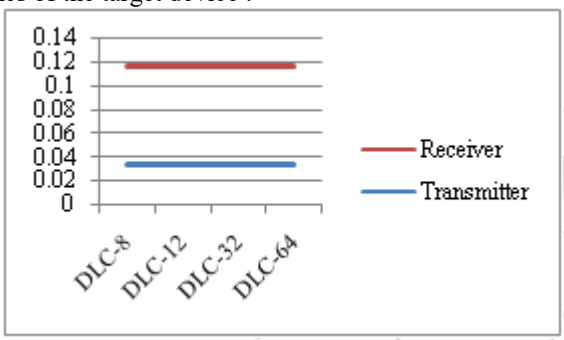
4. Conclusion

The CANFD Protocol implemented in verilog coding compiled using synposys VCS simulator and implemented in Xilinx with bit rate of 2MBPS in arbitration phase and 15 MBPS in data phase. The synthesis report follows:

Table 2: Synthesis Report

Device Utilization Summary	Transmitter Usage	Receiver usage	Available	Utilization of Transmitter	Utilization of Receiver
Number of Slices	157	51	960	16%	5%
Number of slice flipflops	135	50	1920	7%	2%
Number of 4 input LUT's	303	92	1920	15%	4%
Number of Bonded IOB's	50	13	83	60%	15%
Number of GCLKs	1	1	24	4%	4%

Power analysis of Transmitter and receiver is shown below xa3s100e-4cpg132 it is measured under different data frames of the target device .



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