International Journal of Science and Research (IJSR)
ISSN (Online): 2319-7064
Index Copernicus Value (2013): 6.14 | Impact Factor (2014): 5.611

The High Speed Multiplier by using Prefix Adder with MUX and Vedic Multiplication

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Abstract: ***In this paper, we propose a novel architecture to perform high speed Multiplier by using Kogge Stone Adders with Mux and Vedic Multiplication. The Adder employed in implementing the paper is Kogge Stone Adder by using MUX which is a parallel prefix form of Carry Look Ahead Adder & widely used adder in the industries of the present day. One of the most efficient sutra in vedic mathematics named as Urdhva Triyakbhyam strikes a difference in the actual multiplication process. Since the adder used generates the carry signal in O(logn) time, it is widely considered to be the fastest adder design possible. Proposing Kogge Stone Adder by using MUX provides less components, less path delay and better speed compare to other existing Kogge Stone Adder and other Adders. In this research, we have implemented KSA with Mux and Vedic Multiplication. This work estimates the performance of proposed design in terms of Logic and route delay. The experimental results show that the performance of KSA with MUX and Vedic Multiplication is faster compared to other Adders. The proposed algorithm is developed using verilog HDL. Implementation has been done using Xilinx14.2, Spartan 6,***

Keywords: Vedic Mathematics, UrdhvaTriyakbhyam, High Speed Kogge Stone Adder, 14.2 Spartan 6 Device Family.

1. Introduction

In Digital Computer Design adder is an important component and it is used in multiple blocks of its architecture. In many Computers and in various classes of processor specialization, adders are not only used in Arithmetic Logic Units but also used to calculate addresses and table indices. There exist multiple algorithms to carry on addition operation ranging from simple Ripple Carry Adders to complex CLA. The basic operations involved in any Digital Signal Processing systems are Multiplication, Addition and Accumulation. Addition is an indispensible operation in any Digital, DSP or control system. Therefore fast and accurate operation of digital system depends on the performance of adders. Hence improving the performance of adder is the main area of research in VLSI system design. The performance and simulation results were presented. In nearly all digital IC design today, Addition and Multiplication is the most fundamental operation for any low power digital system, Digital Signal Processing (DSP) or control system. A fast and precise operation of a digital system is deeply influenced by the performance of the used Adders and Multipliers. Adders are basic component in any of the existing digital systems because of their wide use in other arithmetic operations such as subtraction, multiplication and division. Hence, performance of the binary adder would greatly advance the execution of binary operations inside a circuit consisted of such blocks. When taking into account the other parts of ICs, like area or power, the designer will discover that the hardware for addition will be a huge contributor to these areas. It is therefore valuable to select the right adder to develop and employ in a design because of the many factors it aspects in the overall ICs.

2. Objective

The aim of this work is to design and implement high speed Kogge-stone adder by using MUX with UT algorithm of Vedic mathematics and its multiplication concept and evaluate the performance of Kogge-stone adder for binary addition to reduce the size and increase the efficiency or processors speed. Implementation of this multiplier has been done on Xilinx 14.2 Spartan 6 series.

3. Vedic Multiplier

Vedic mathematics is defined as the ancient Indian system of mathematics which is based on sixteen principles or vedic mathematical formulae known as Sutras. The „Vedic" word derived from the word „Veda" which means the store house of all knowledge, this was reconstructed by ShriBharati Krishna Tirtha. According to him it reduces the cumbersome mathematical calculations into simple ones and find its applications in computing and DSPs. We discussed vedic multiplication algorithm to digital multipliers as multipliers play an important role in today"s Digital Signal Processing (DSP) and various other applications. With updating in technology advancement, many researcher scholars have tried and are trying to design, develop or implementation of multipliers which provide either of following features – high speed, less power consumption, regularity of layout and hence less area or even combination of them in one multiplier. This will used in making of various high speeds, low power, compact VLSI circuits. Multiplication is a mathematical operation that its simplest is an abbreviated method of adding an integer to itself, a defined number of times. A number (multiplicand) is added to itself a number of times as defined by another number (multiplier) to form a result (product).

In this research a simple digital multiplier based on the vedic mathematics sutra named UrdhvaTriyakbhyam (vertically and crosswise) sutra. In this sutra is presented as much more efficient multiplication algorithm as compared to the conventional process.

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A. UrdhvaTiryakbhyam

UrdhvaTiryakbhayam (UT) sutra is the vedic multiplication formula from the ancient Vedic mathematic which is suitable for the multiplication of decimal number, hexadecimal number and binary number. In figure 1 shown below the multiplication of two decimal numbers. UT algorithm has such features that are compatible with the digital systems, also it provides the fast computation because the partial product and their sums are calculated parallel. The Urdhav is a Sanskrit word which means vertical and Tiryagbhyam‟ means “crosswise” in English, UT vedicalgorithm computes crosswise and vertical operations between any two given numbers. The method is customized for the multiplication is based on the theory in which generation of the partial products and additions are done concurrently which increases the speed of multiplication operation and performance.

B. UT Multiplier

UT is a novel conception through which throughput is obtained concurrently. Creation of partial products and their addition is obtained using UT algorithm which is described in figure 1. It reduces the need of resources from processors to function at high frequencies demands which are its unique feature and due to this it differs from other conventional process. Other benefits of Vedic UT based Multiplier is that as the number of bits increases, area and gate delay increases at a faded rate as contrast to other multipliers. Hence it is efficient in all terms such as power, time & area.

$$S_0 = A_0 + B_0 \quad (1)$$

$$C_1S_1 = A_1B_0 + A_0B_1 \quad (2)$$

$$C_2S_2 = C_1 + A_1B_1 \quad (3)$$

Based on above equations, the final result is $C_2S_2S_1S_0$. Similarly, the other cases can be calculated for all 2x2 bits module, 4x4, 8x8, 16x16 and nxn bits module so on.

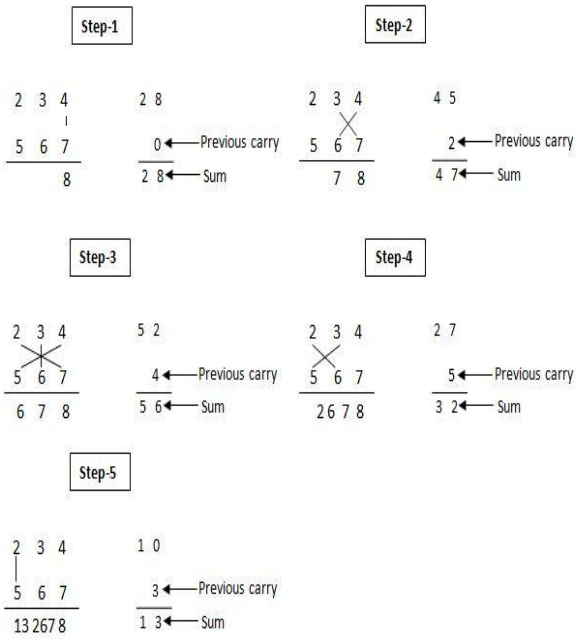

Figure 1: Multiplication of two decimal numbers using UT vedic algorithm

Above example shows that how UT vedic algorithm can be done by following all the steps.

4. MUX as a XOR Gate

XOR gate is the special type of gate which is represented by plus sign with encirclement. The matter of complexity can be reduced by the aid of designing of the gates. Less number of gates provides the less area for attractive designing in digital processing. XOR gate is comprised with five gates (Two AND, two NOT and one OR gate). XOR gate can also be replaced by Multiplexer (MUX). In digital electronics we are having two types of universal gates like NAND and NOR gate. By using any universal gate we can design any type of gate. Likewise MUX behaves like as universal gate that means by using MUX any type of gate can be designed. To design the 2 inputs XOR gate one input of MUX must be invert to the other and both input would be connected together. Another input of XOR gate would be applied to the select line of the MUX. So, the output of the MUX would be as same as the output of XOR Gate. The advantage of this type of designing that is Differential Cascode Voltage Switch Logic (DCVSL) as a MUX is that it produces both true and complementary outputs when provided with true and complementary inputs.

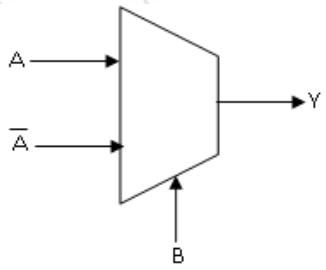

Figure 2: A MUX block diagram for working as a XOR gate

5. Kogge-Stone Adder (KSA)

The Kogge-Stoneadder is the special and fast adder. The Kogge–Stone adder is a parallel prefix form carry look ahead adder. It generates the carry signals in O(logn) time, and is widely considered to be fastest adder in the industry. An illustration of 4-bit kogge stone adder by taking two 4 bit inputs is shown in Figure 3. Kogge stone adder is comprised with three units such as preprocessing, carry generator and post processing unit.

$$P = A_i \oplus B_i \quad (4)$$

$$G = A_i \; B_i \quad (5)$$

$$C_i = G_i \quad (6)$$

$$S_i = P_i \oplus C_{i+1} \quad (7)$$

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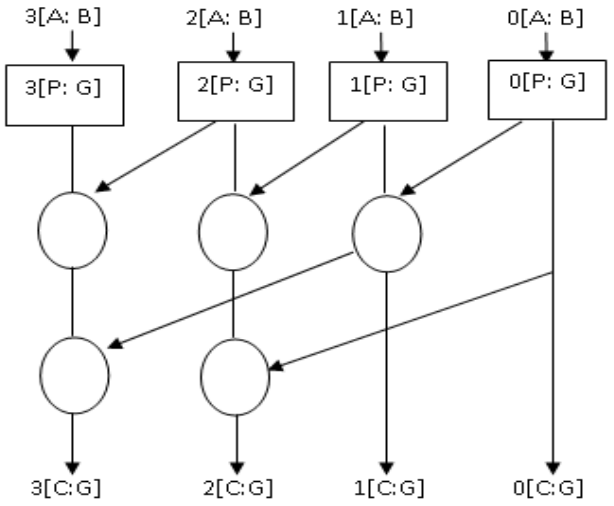

Figure 3: A Basic Building Block of KSA

In kogge stone adder XOR can be replaced by MUX which provide different structure and gives the true and complement value at a time.

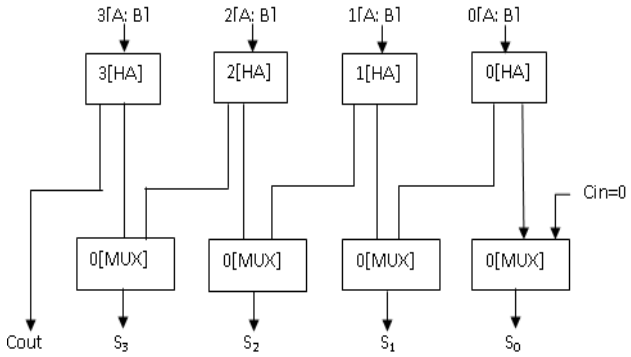

Figure 4: Proposed KSA by using MUX

6. Design and Implementation

Technology is scaling down from micro scale to nano scale day by day. These are the main motivation to develop and implement a high speed multiplier using KSA with Vedic mathematics sutra algorithm is applied, because it execute simple operation and give up results quickly. The two step mainly generation of partial product and addition of partial product involves in multiplication method, these two steps are concurrently compute by the UT algorithm of Vedic Mathematics. This chapter describes the implementation of Vedic multiplier using KSA, with the objective to develop a high speed multiplier based on Vedic sutra in order to improve the reliability and performance of the digital system. This is just one of the many probable applications of the Vedic Mathematics to Engineering and some severe efforts are needed to fully utilize the potential of this interesting field for the progression of Engineering andTechnology

A. Experimental Setup

To design and implement 4x4 bit KSA using MUX, An Vedic Algorithm is applied between the four bit of multiplier and multiplicand say A [3:0], B [3:0] and produce the multiplication result in P[7:0] bit

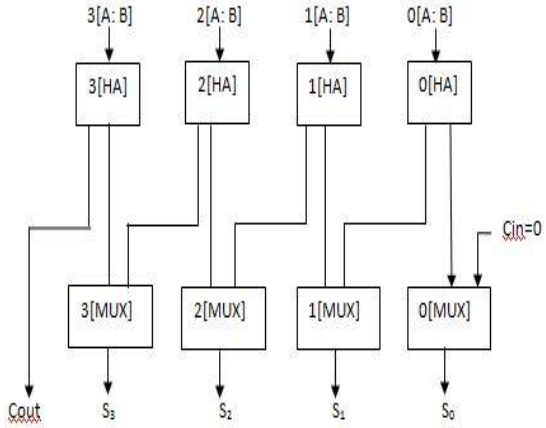

Figure 5: 4 bit KSA using MUX

The four 2-bit fault tolerant reversible vedic multiplier is required to implement an 4-bit multiplier

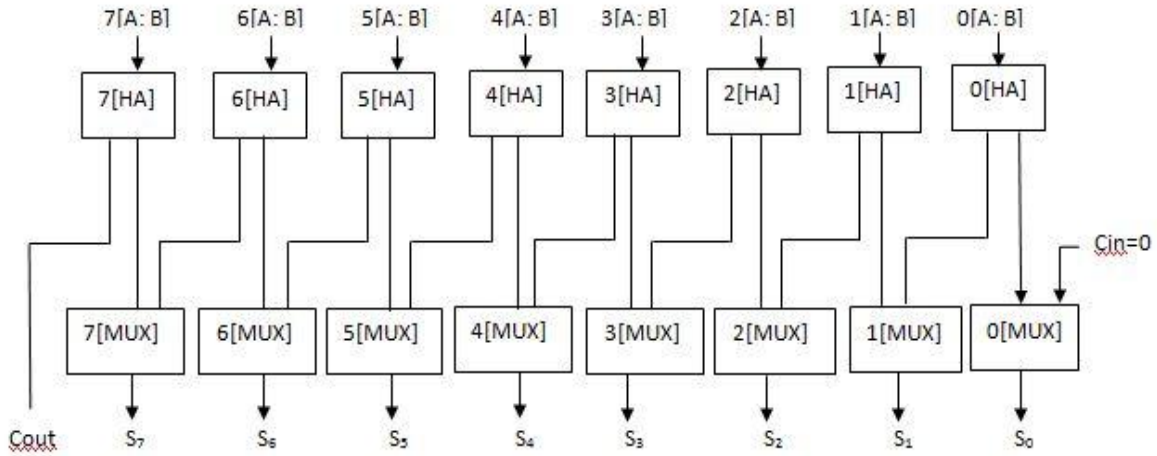

Figure 6: 8 bit KSA using MUX

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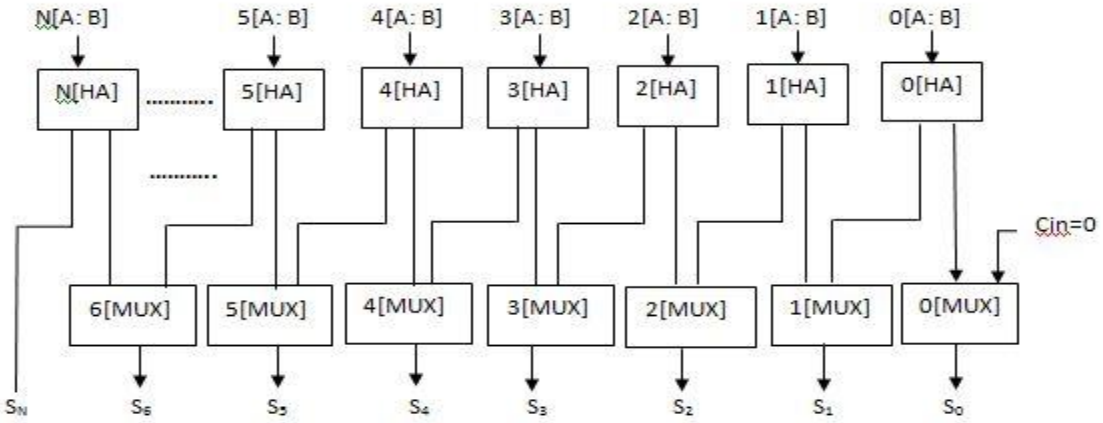

Figure 7: n bit KSA using MUX

Similarly, we have presented the block diagram of 8 bit KSA using MUX in Fig. 6 and n bit KSA using MUX is shown in Fig 7.

B. Design Implementation

The design of proposed Vedic Multiplier is based on a UT algorithm of multiplication. Here the modular (smaller) blocks are used to design the complex one. The 4×4 bit Vedic multiplication unit is further realized by incorporating four similar modules of 2×2 multipliers. The processing in the form of block diagram is depicted in Figure 8 for 4×4 multiplier. VHDL (Verilog Hardware Description Language) is used for the design of vedic multiplier.

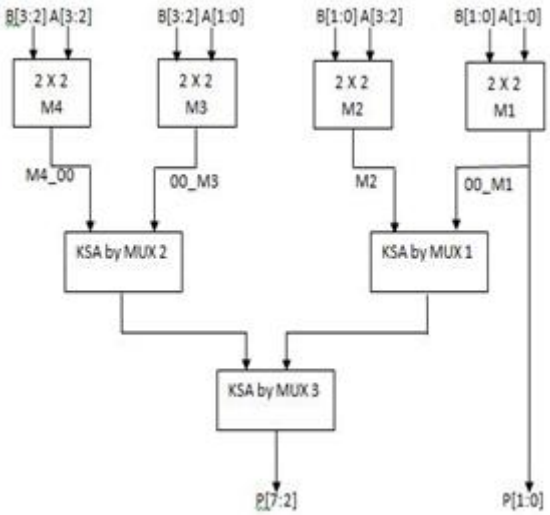

Figure 8: 4x4 Vedic multiplier using KSA (MUX)

7. Simulation Results

Kogge-Stone Adder. All the parameters those are in table 1 are experimented by Xilinx 14.2 Spartan 6 series. KSA adder has less propagation or path delay than to RCA adder. Combinational path delay is an important factor for the IC designing in VLSI technology and ULSI technology. And for designing the high speed processor propagation delay must be less as possible as. For the low order designing parameter are approximately same but as soon as increasing the number of orders are concerned both adders have different-different scale parameters, Xilinx Spartan 6 (Family), XC6SLX9 (Device), TQG144 (Package), -3 (Speed Grade) has only 5720 slices LUTs and 102 bonded IOBs.

Table 1: Comparison between RCA and KSA (MUX) adder

Order	Adder	No. of slices LUTs (5720)	No. of bonded IOBs (102)	Propagation Delay (ns)
2 bit	RCA	3	7	5.456
	KSA (MUX)	3	7	5.439
4 bit	RCA	6	13	6.480
	KSA (MUX)	5	13	5.439
8 bit	RCA	12	25	8.397
	KSA (MUX)	9	25	5.439
16 bit	RCA	24	49	12.230
	KSA (MUX)	17	49	5.439

The design has been synthesized and simulates using Xilinx. The performance of proposed KSA (MUX) is analyzed and compared with conventional RCA. As above table shows the comparison between RCA and KSA (using MUX) for the number of LUTs at different bits particularly 2, 4, 8, 16 bits and it was observed that the performance of KSA is quite good as compared to the RCA.

We have also compared the parameters and their values in case of RCA using Vedic multiplications and KSA (MUX) using Vedic multiplications with details shown below in the table 2.

Table: 2 Comparison between Vedic multipliers by using RCA and KSA (MUX)

Multiplier	Components	No. of slice LUTs (5720)	No. of bonded IOBs (102)	Propagation Delay (ns)
4 bit Multiplier by using RCA	a. (2X2) Vedic multiplier b. 4,6,7 bit RCA	20	18	9.332
4 bit Multiplier by using proposed KSA	a. (2X2) Vedic multiplier b. 4,6,7 bit proposed KSA	17	18	7.881

Eventullay, according to table for wishing the designing the high speed Vedic multiplier has compared two devices such

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as RCA and KSA (MUX). For the desingning of multipliers components are the same. But both are having the different-diffrerent parameter like slices, LUTs, IOBs and propagation delay. The main object of this research is that to reduce the propgation delay and slices. If slices are reduced than area of the circuit will automatically reduced. The parameter of te slices are directly proportional to the propgation delay. So as soon as slices are decreased the propagation delay automatically decreased. The simulation of 4 bit Vedic multiplier by using KSA (MUX) is shown in figure 9.

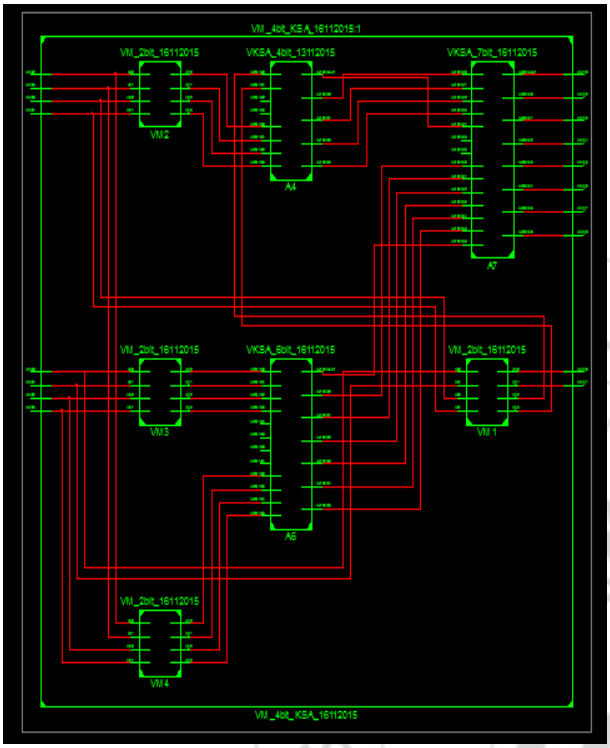

Figure 9: Simulation of 4 bit Vedic multiplier by using KSA (MUX)

8. Conclusion and Future Work

In Low power Very Large Scale Integration (VLSI) circuits or digital circuits and processing systems designing of high performance and portable devices are very important part. The main parameters of considerations in VLSI circuits are high speed, small area and low cost. The significance of low power is increasing day by day because of changing tendency, packaging and cooling cost, portable systems and reliability. In this research work we studied the parallel prefix form such as Carry Look Ahead Adder and design and implement high speed Kogge-stone adder by using MUX has been done. The future aspects for this research is to design a filter to rescue the blurred signal in Image signal Processing, and design high speed ALU and GPU.

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