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Cascaded Multilevel Inverter with Developed H Bridge Units

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Abstract: ***Nowadays, the multilevel inverters have received much attention because of their considerable advantages such as high power quality, lower harmonic components, lower dv/dt and lower switching Losses. There are three main types of multilevel inverters, Diode clamp multilevel inverter, flying capacitor multilevel Inverter, and cascaded multilevel inverter. The Cascaded multilevel inverters have received special attention due to the modularity and simplicity of control. Here, a new single- phase cascaded multilevel inverter based on novel H-bridge units is introduced. In order to generate all voltage levels (even and odd) at the output, different algorithms can be to determine the magnitudes of dc voltage sources. Then, the new algorithms are compared to investigate their advantages and disadvantages. This topology is able to increase the number of output voltage levels by using a lower number of power electronic devices such as switches, power diodes, driver circuits, and dc voltage sources that lead to reduction in installation space and cost of the inverter. In addition, in the new cascaded multilevel inverter, not only the number of required power electronic devices is reduced, but also the amount of the blocked voltage by switches, and the number of different voltage amplitudes of the used sources is decreased. These features are some of the most important advantage of the new topology. Simulation is done in MATLAB 2009a environment and the waveforms are obtained. For the experimental setup the dc sources selected are 2V, 4V, 14V, 28V.***

Keywords: Cascaded multilevel inverter, developed H-bridge, multilevel inverter

1. Introduction

The term multilevel began with the use of basic three level Converter and later several multi- level converter topologies have been developed. However, the concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources by obtaining a staircase voltage waveform. Capacitors, batteries, and renew- able energy voltage sources can be used as the multiple dc voltage sources. The commutation of the power switches aggregate these multiple dc sources in order to achieve high voltage at the output. However, the rated voltage of the power semiconductor switches depends only upon the rating of the dc voltage sources to which they are connected. Plentiful multilevel converter topologies have been proposed during the last two decades. Moreover, abundant modulation techniques and control paradigms have been developed such as sinusoidal pulse width modulation (SPWM), selective harmonic elimination (SHE-PWM), space vector modulation (SVM) etc. In addition, many multilevel converter applications focus on industrial medium-voltage motor drives, utility interface for renewable energy systems, flexible AC transmission system (FACTS), and traction drive systems. There are three main types of multilevel inverters they are diode clamp multilevel inverter, flying capacitor multilevel inverter, and cascaded multilevel inverter. Among these cascaded multilevel inverters are widely used in various industrial applications due to its simplicity and modularity. In this topology several H-bridge inverters are connected in series to get a sinusoidal voltage output. The output voltage is the sum of the voltage that is generated by each cell. Each cell can provide the three different voltages such as zero, positive and negative voltages. Advantages of this type of multilevel inverter is that it needs less number of components comparative to the Diode clamped or the Flying capacitor, so the price and the weight of the inverter is less than that of the two former types also it eliminate the need of bulky transformer case of conventional multi phase inverters, clamping diodes required in case of diode clamped inverters and flying capacitors required in case of flying capacitor inverters. The cascaded multilevel inverters are of two types symmetric and asymmetric. In the symmetric topology, the values of all of the dc voltage sources are equal. This characteristic gives the topology good modularity. But the number of the switching devices rapidly increases as the number of output voltage level increases. A symmetrical topology with n equal dc voltage sources can offer 2n + 1 distinct voltage levels at output. In order to increase the number of output voltage level, the value of the dc voltage sources are selected to be different, these topologies are called asymmetric cascaded multilevel inverters. For n such cascaded inverters, with unequal dc voltage sources one can achieve 2^{n+1} distinct voltage levels. Therefore, the asymmetric cascaded multilevel inverters increase the number of output levels by using power semiconductor devices that are the same as the symmetric ones [1], [2], [3], [4]. In this paper, a new single-phase cascaded multilevel inverter with series connection of H bridge units is introduced. This cascaded multilevel inverter with developed H bridge unit can produce higher levels of output voltage with reduced no: of switches drivers and dc voltage sources. Simulink model of a 49 level inverter is also presented.

2. Developed H Bridge Topology

Fig 1 shows the basic unit of new cascaded multilevel inverter. (S_{L1}, S_{L2}, S_{R1}, S_{R2}, S_a, and S_b) are the switches and dc voltage sources (V_{L1} and V_{R1}) are the dc voltage sources.

The main advantage of the new basic unit over the H-bridge is that, this basic unit is able to generate seven different levels at the output, whereas three output levels are only generated in the H-bridge. If equal magnitudes of the dc voltage sources used, the developed inverter can generate five levels at the output. To generate higher numbers of output levels, the magnitude of dc voltage sources have to be selected differently.

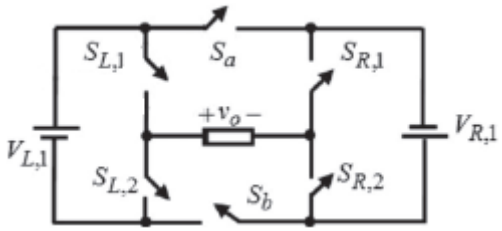

Figure 1: Developed H bridge unit

The main parameter in calculating the total cost of the inverter is the maximum amount of the blocked voltage by switches. If the values of the blocked voltage by switches are reduced, the total cost of the inverter decreases. Therefore, in order to calculate this index, it is necessary to consider the amount of the blocked voltage by each of the switches. According to Fig. 1, the values of the blocked voltage by switches S_{R1}, S_{R2}, S_{L1}, S_{L2}, S_a, S_b and are give as,

$$V_{SR,1} = V_{SR,2} = V_{SR,1} \quad (1)$$

$$V_{SL,1} = V_{SL,2} = V_{SL,1} \quad (2)$$

$$V_{Sa} = V_{Sb} = \left(V_{SR,1} + V_{SR,1}\right) \quad (3)$$

The maximum amount of the blocked voltage by all of the used switches in the basic unit, i.e., V_{block1}, is equal to,

$$V_{Block} = 4\left(V_{SR,1} + V_{SR,1}\right) \quad (4)$$

It is important to note that the existence of all voltage levels at the output is based on suitable selection of the magnitude of dc voltage sources. Thus, in order to generate all voltage levels at the output, different algorithms to determine the magnitude of dc voltage sources are proposed. Some of these algorithms had been presented for conventional cascaded inverters in the literature, but they could be also used in the new topology or any inverter. According to each of the algorithms, the number of output voltage levels (N_{level}), the maximum amplitude of the producible output voltage (V_{omax}), the number of different voltage amplitudes of the used sources ($N_{variety}$), and the maximum amount of the blocked voltage by switches (V_{block}) will be different.

Algorithm for symmetric topology is the simplest one. Using this algorithm 5 levels can be obtained as the output of a single basic unit. Details about the algorithm,

Magnitude of dc voltage sources,

- $V_{R,J} = V_{L,J}, Vdc$, Where j=1,2. . . n (5)
- $N_{level} = 4n + 1$ (6)
- $V_{omax} = 2n\ V_{dc}$ (7)
- $V_{block} = 8n$ Vdc (8)

There are different algorithms for asymmetric topologies. Details about one of the algorithm for asymmetric topology,

Magnitude of dc voltage sources,

- $V_{R,J} = 7^{n-1} * V_{dc}, V_{L,J=}2 * 7^{n-1} * V_{dc}$ (9)
- $N_{level} = 7^n$ (10)
- $V_{omax} = \frac{7^{n-1}}{2} * V_{dc}$ (11)
- $V_{block} = 2*7^{n-1} * V_{dc}$ (12)

Table I shows the generated output voltage levels based on the different switching patterns in the developed basic unit for symmetric topology. In this table, 1 and 0 indicate the on and off states of the switches, respectively. As shown in Table I, this basic unit is able to generate five levels (three positive levels, three negative levels, and one zero level) at the output. In addition, in each switching pattern, one power switches from each leg ($S_{L,1}$ or $_{SL,2}$), ($S_{R,1}$ or $S_{R,2}$), and S_a or S_b are turned on simultaneously.

TABLE I: Developed H bridge basic unit switching pattern (symmetrical)

State	$S_{L,1}$	$S_{L,2}$	$S_{R,1}$	$S_{R,2}$	S_a	S_b	V_o
1	1	0	0	1	0	1	$V_{L,1}$
2	1	0	1	0	0	1	$V_{L,1} + V_{R,1}$
3	1	0	1	0	0	1	$V_{L,1} + V_{R,1}$
4	1	0	1	0	1	0	0
4	0	1	0	1	0	1	0
5	0	1	1	0	1	0	$-V_{L,1}$
6	0	1	0	1	1	0	$-(V_{L,1} + V_{R,1})$
7	1	0	1	0	0	1	$V_{L,1} + V_{R,1}$

The magnitude of the dc voltage sources is considered as follows:

$$V_{L,n} = V_{dc} \quad (13)$$

$$V_{R,n} = V_{dc} \quad (14)$$

Table II shows the generated output voltage levels based on the different switching patterns in the developed basic unit for asymmetric topology. The magnitude of the dc voltage sources is considered as follows;

$$V_{L,n} = V_{dc} \quad (15)$$

$$V_{R,n} = 2 * V_{dc} \quad (16)$$

TABLE II: Developed H bridge basic unit switching pattern (asymmetrical)

State	$S_{L,1}$	$S_{L,2}$	$S_{R,1}$	$S_{R,2}$	S_a	S_b	V_o
1	1	0	0	1	0	1	$V_{L,1}$
2	0	1	1	0	0	1	$V_{R,1}$
3	1	0	1	0	0	1	$V_{L,1} + V_{R,1}$
4	1	0	1	0	1	0	0
4	0	1	0	1	0	1	0
5	0	1	1	0	1	0	$-V_{L,1}$
6	1	0	0	1	1	0	$-V_{R,1}$
7	0	1	0	1	1	0	$-(V_{L,1} + V_{R,1})$

A new cascaded multilevel inverter can be made by series connection of n number of the developed H-bridge basic units. This inverter is shown in Fig. 2. According to this figure, the output voltage of the modified cascaded multilevel inverter is the sum of output levels of all units and is given by,

$$V_O(t) = V_{O,1}(t) + V_{O,2}(t) + \cdots V_{O,n}(t) \quad (17)$$

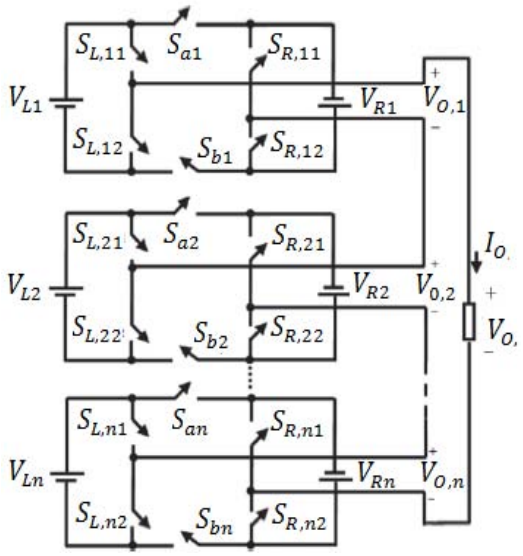

Figure 2: Cascaded multilevel inverter with developed H bridge unit

In the new cascaded multilevel inverter, the number of switches (N_{switch}), driver circuits (N_{driver}), and dc voltage sources (N_{source}) are calculated as follows,

$$N_{switch} = N_{driver} = 6n \quad (18)$$

$$N_{source} = 2n \quad (19)$$

3. Simulation of Basic Unit

The fig.3. shows the Simulink model of developed basic unit for cascaded multilevel inverter. The unit contains six power switches ($S_{L,1}$, $S_{R,1}$, $S_{L,2}$, $S_{R,2}$, S_a, S_b), two dc sources and a resistive load. The switching sequence is loaded into the switch logic block in the simulink model using if else loop. The sampling time is specified using the repeating sequence. The sampling period here is 0.00125 ms. Circuit specification for symmetric topology is V_{L1}= 2.5 V, V_{R1}= 2.5 V, output voltage obtained is 5 V. The switching pattern is shown in Table III. Symmetrical configuration of the inverter using the algorithm discussed earlier is simulated here. The output voltage obtained using this symmetrical topology contains 5 levels of voltage. Fig. 3 and Fig. 4 shows output voltage and blocked voltage.

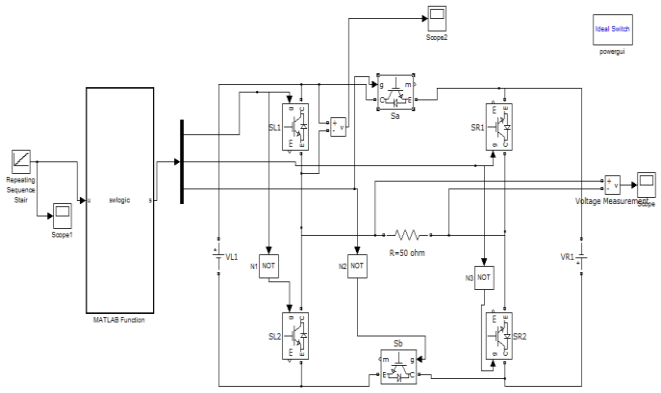

Figure 3: Simulink model of Basic unit

Table 5.2. Basic unit switching pattern (symmetrical)

State	$S_{L,1}$	$S_{L,2}$	$S_{R,1}$	$S_{R,2}$	S_a	S_b	V_o
1	1	0	1	0	1	0	0 V
2	1	0	0	1	0	1	$V_{L,1} = 2.5$ V
3	1	0	1	0	0	1	$V_{L,1} + V_{R,1} = 5$ V
4	1	0	1	0	0	1	$V_{L,1} + V_{R,1} = 5$ V
5	1	0	0	1	0	1	$V_{L,1} = 2.5$ V
6	1	0	1	0	1	0	0 V
7	1	0	1	0	1	0	0 V
8	0	1	1	0	1	0	$-V_{L,1} = -2.5$ V
9	0	1	0	1	1	0	$-(V_{L,1} + V_{R,1}) = -5$ V
10	0	1	0	1	1	0	$-(V_{L,1} + V_{R,1}) = -5$ V
11	0	1	1	0	1	0	$-V_{L,1} = -2.5$ V
12	0	1	0	1	0	1	0 V

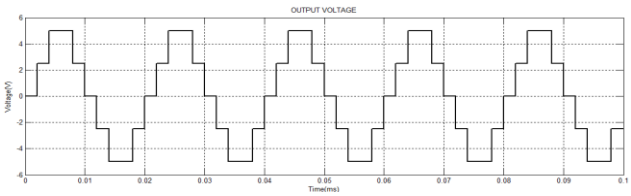

Figure 4: Output voltage (Symmetric)

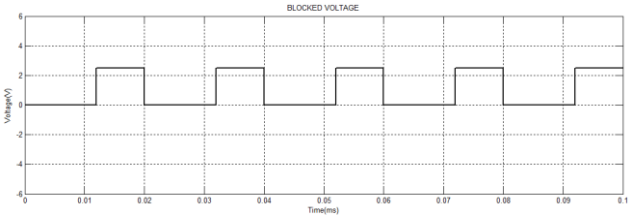

Figure 5: Blocked voltage across S_{L1}(Symmetric)

Circuit specification for asymmetric topology is VL1= 2.5 V, VR1= 5 V, output voltage obtained is 7.5 V. The output voltage obtained using asymmetrical topology contains 7 levels of voltage. The switching pattern is shown in Table IV. The seven levels of voltage that is obtained are 0, 2.5, 5, 7.5, -2.5, -5 and -7.5. Fig 6 and 7 shows the output and blocked voltage waveform.

Table 5.4. Basic unit switching pattern (asymmetrical)

State	$S_{L,1}$	$S_{L,2}$	$S_{R,1}$	$S_{R,2}$	S_a	S_b	V_o
1	1	0	1	0	1	0	0 V
2	1	0	0	1	0	1	$V_{L,1} = 2.5$ V
3	0	1	1	0	0	1	$V_{R,1} = 5$ V
4	1	0	1	0	0	1	$V_{L,1} + V_{R,1} = 7.5$ V
5	1	0	1	0	0	1	$V_{L,1} + V_{R,1} = 7.5$ V
6	0	1	1	0	0	1	$V_{R,1} = 5$ V
7	1	0	0	1	0	1	$V_{L,1} = 2.5$ V
8	1	0	1	0	1	0	0 V
9	0	1	0	1	0	1	0 V
10	0	1	1	0	1	0	$-V_{L,1} = -2.5$ V
11	1	0	0	1	1	0	$-V_{R,1} = -5$ V
12	0	1	0	1	1	0	$-(V_{L,1} + V_{R,1}) = -7.5$ V
13	0	1	0	1	1	0	$-(V_{L,1} + V_{R,1}) = -7.5$ V
14	1	0	0	1	1	0	$-V_{R,1} = -5$ V
15	0	1	1	0	1	0	$-V_{L,1} = -2.5$ V
16	0	1	0	1	0	1	0 V

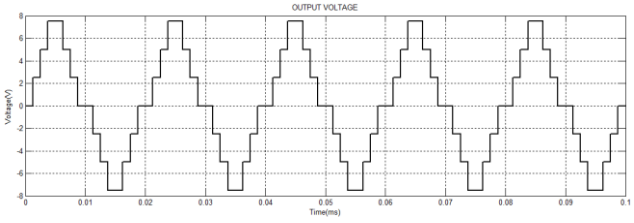

Figure 6: Output voltage (Asymmetric)

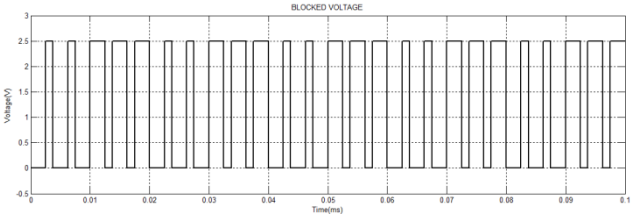

Figure 7: Blocked voltage across S_{L1}(Asymmetric)

4. Simulation of Two Basic Units Connected In Series

Fig. 8 shows the simulink model for cascaded multilevel inverter with developed H bridge units. This is obtained by connecting two basic units in series. The circuit has a total of 12 switches and 4 dc sources. The 4 dc sources are equal in magnitude, 2 V (symmetrical). This multilevel inverter is capable of generating 9 levels of voltage at the output. This is a symmetrical topology. If asymmetrical is used ie, unequal dc sources are used then up to 49 level output can be obtained. Since asymmetric topology gives more no: of levels it is preferred. The switching pattern for obtaining the required output is loaded into the switch logic unit. The switch logic unit generates the gate signals required for the switches. The dc voltage sources are set at the required magnitudes before simulation. The magnitude of dc source is chosen as 2V for symmetric topology and the magnitude of dc source is chosen as 2V, 4V, 14V and 28V for asymmetric topology. The resistance is taken as 50 Ohm. Table V shows the switching pattern for cascaded (two basic units) multi-level inverter in symmetrical topology with developed H bridge units for obtaining 9 levels in output.

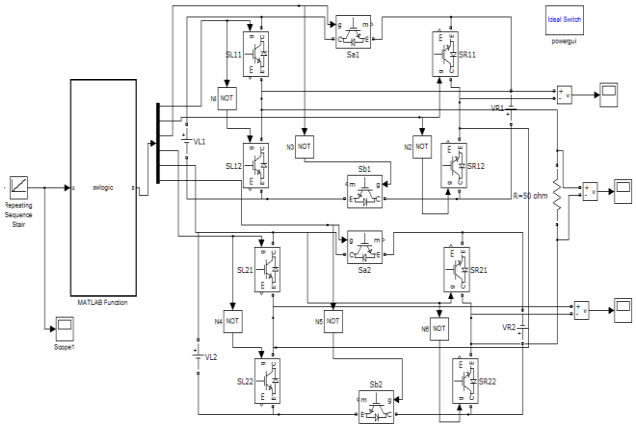

Figure 8: Simulink model of cascaded multilevel inverter

TABLE V: cascaded multilevel inverter switching pattern (symmetric

State	S_{L11}	S_{L12}	S_{R11}	S_{R12}	S_{a1}	S_{b1}	S_{L21}	S_{L22}	S_{R21}	S_{R22}	S_{a2}	S_{b2}	$V_o(V)$
0	1	0	1	0	1	0	1	0	1	0	1	0	0
1	1	0	0	1	0	1	1	0	1	0	1	0	2
2	1	0	1	0	0	1	1	0	1	0	1	0	4
3	1	0	1	0	0	1	1	0	0	1	0	1	6
4	1	0	1	0	0	1	1	0	1	0	0	1	8
5	1	0	1	0	0	1	1	0	1	0	0	1	8
6	1	0	1	0	0	1	1	0	0	1	0	1	6
7	1	0	1	0	0	1	1	0	1	0	1	0	4
8	1	0	0	1	0	1	1	0	1	0	1	0	2
9	1	0	1	0	1	0	1	0	1	0	1	0	0
10	0	1	1	0	1	0	1	0	1	0	1	0	-2
11	0	1	0	1	1	0	1	0	1	0	1	0	-4
12	0	1	0	1	1	0	0	1	1	0	1	0	-6
13	0	1	0	1	1	0	0	1	0	1	1	0	-8
14	0	1	0	1	1	0	0	1	0	1	1	0	-8
15	0	1	0	1	1	0	0	1	1	0	1	0	-6
16	0	1	0	1	1	0	1	0	1	0	1	0	-4
17	0	1	1	0	1	0	1	0	1	0	1	0	-2
18	1	0	1	0	1	0	1	0	1	0	1	0	0

Fig. 9 shows the various waveforms obtained using symmetrical topology with two basic units connected in series.

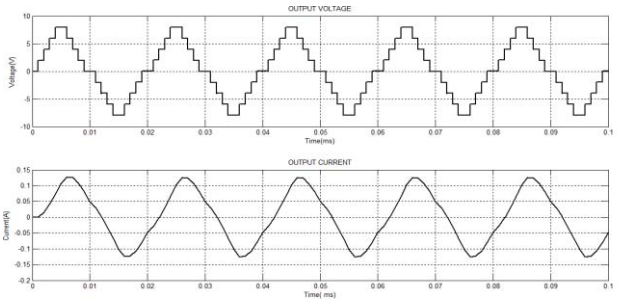

Figure 9: Output voltage of cascaded multilevel inverter (Symmetric)

Table VI and VII shows the positive and negative voltage switching pattern for cascaded (two basic units) multilevel inverter in asymmetrical topology with developed H bridge units for obtaining 49 levels in output. Fig. 10 shows the output voltage and current for asymmetric topology using two basic units. Circuit specifications are V_{L1} = 2 V, V_{R1} = 4 V, V_{L2} = 14 V, V_{R2} = 28 V output voltage obtained is 48 V.

TABLE VI: cascaded multilevel inverter switching pattern (positive sequence)

State	S_{L11}	S_{L12}	S_{R11}	S_{R12}	S_{a1}	S_{b1}	S_{L21}	S_{L22}	S_{R21}	S_{R22}	S_{a2}	S_{b2}	$V_o(V)$
0	1	0	1	0	1	0	1	0	1	0	1	0	0
1	1	0	0	1	0	1	1	0	1	0	1	0	2
2	1	0	1	0	0	1	1	0	1	0	1	0	4
3	1	0	1	0	0	1	1	0	0	1	0	1	6
4	1	0	1	0	0	1	1	0	1	0	0	1	8
5	1	0	1	0	0	1	1	0	1	0	0	1	8
6	1	0	1	0	0	1	1	0	0	1	0	1	6
7	1	0	1	0	0	1	1	0	1	0	1	0	4
8	1	0	0	1	0	1	1	0	1	0	1	0	2
9	1	0	1	0	1	0	1	0	1	0	1	0	0
10	0	1	1	0	1	0	1	0	1	0	1	0	-2
11	0	1	0	1	1	0	1	0	1	0	1	0	-4
12	0	1	0	1	1	0	0	1	1	0	1	0	-6
13	0	1	0	1	1	0	0	1	0	1	1	0	-8
14	0	1	0	1	1	0	0	1	0	1	1	0	-8
15	0	1	0	1	1	0	0	1	1	0	1	0	-6
16	0	1	0	1	1	0	1	0	1	0	1	0	-4
17	0	1	1	0	1	0	1	0	1	0	1	0	-2
18	1	0	1	0	1	0	1	0	1	0	1	0	0

TABLE VII: cascaded multilevel inverter switching pattern (negative sequence)

State	S_{L11}	S_{L12}	S_{R11}	S_{R12}	S_{a1}	S_{b1}	S_{L21}	S_{L22}	S_{R21}	S_{R22}	S_{a2}	S_{b2}	$V_o(V)$
0	1	0	1	0	1	0	1	0	1	0	1	0	0
1	1	0	0	1	0	1	1	0	1	0	1	0	2
2	1	0	1	0	0	1	1	0	1	0	1	0	4
3	1	0	1	0	0	1	1	0	0	1	0	1	6
4	1	0	1	0	0	1	1	0	1	0	0	1	8
5	1	0	1	0	0	1	1	0	1	0	0	1	8
6	1	0	1	0	0	1	1	0	0	1	0	1	6
7	1	0	1	0	0	1	1	0	1	0	1	0	4
8	1	0	0	1	0	1	1	0	1	0	1	0	2
9	1	0	1	0	1	0	1	0	1	0	1	0	0
10	0	1	1	0	1	0	1	0	1	0	1	0	-2
11	0	1	0	1	1	0	1	0	1	0	1	0	-4
12	0	1	0	1	1	0	0	1	1	0	1	0	-6
13	0	1	0	1	1	0	0	1	0	1	1	0	-8
14	0	1	0	1	1	0	0	1	0	1	1	0	-8
15	0	1	0	1	1	0	0	1	1	0	1	0	-6
16	0	1	0	1	1	0	1	0	1	0	1	0	-4
17	0	1	1	0	1	0	1	0	1	0	1	0	-2
18	1	0	1	0	1	0	1	0	1	0	1	0	0

Fig. 10 shows the output voltage and current for asymmetric topology using two basic units in asymmetric topology. Circuit specifications are V_{L1}= 2V, V_{R1}= 4 V, V_{L2}= 14 V, V_{R2}= 28 V and output voltage obtained is 48 V.

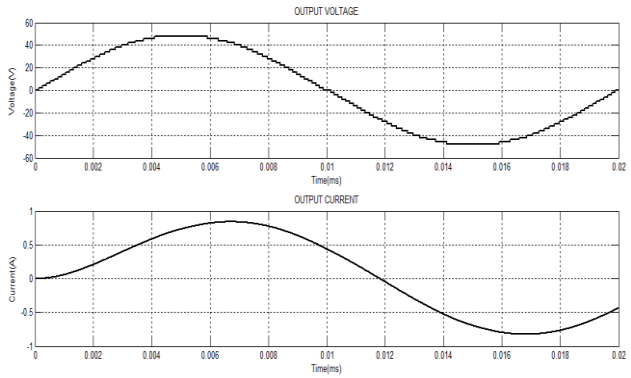

Figure 10: Output voltage and output current

The output voltage is 48 V. The output waveform has 49 levels. 24 positive levels, 24 negative levels and a zero level. This is the maximum no: of levels that can be obtained using two basic units connected in series. The Total Harmonic distortion (THD) of the output is 0.02 pu which is much less than the conventional cascaded multilevel inverter topology. Since asymmetric topology gives more no: of levels it is taken for hardware implementation

5. Experimental Results

The waveforms obtained from the experimental setup of cascaded multilevel inverter in asymmetric topology are shown here. For the experimental setup of single stage inverter the dc source were set at 2.5 V and 5 V and for two stage inverter in asymmetric topology the dc sources selected are 2V, 4V, 14V, 28V and for. All the dc sources are isolated dc sources but the highest one (28v) it can be given through an autotransformer also. The output voltage waveform obtained using single stage inverter have 7 levels and cascaded mulilevel inverter Have 49 levels. Theoreticaly the output of single stage is 7.5 V and experimentally it is obtained as 8 V. Which is almost equal. This is because voltage source was a little uctuating. The output voltage waveform obtained having seven levels is shown in Fig. 11.

The output voltage waveform is similar to the waveform obtained using simulation. Fig. 12 shows the pulses given to the switch S_{L11}. Fig 13 shows the pulses given to the switch S_{R11}. Fig. 14 shows the pulses given to the switch S_a. Fig. 15, Fig. 16, and Fig 17 shows the voltage stress across the switchS S_{L11}, S_{R11} and S_a.

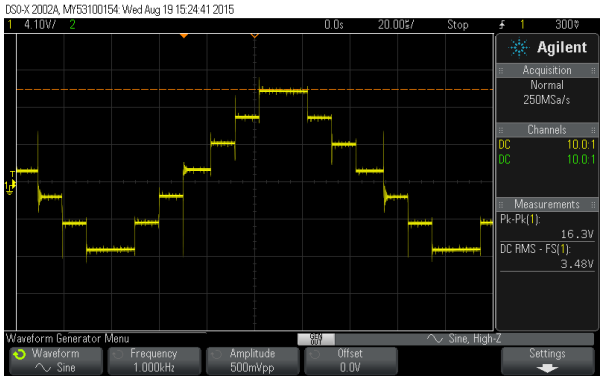

Figure 11: Single stage output

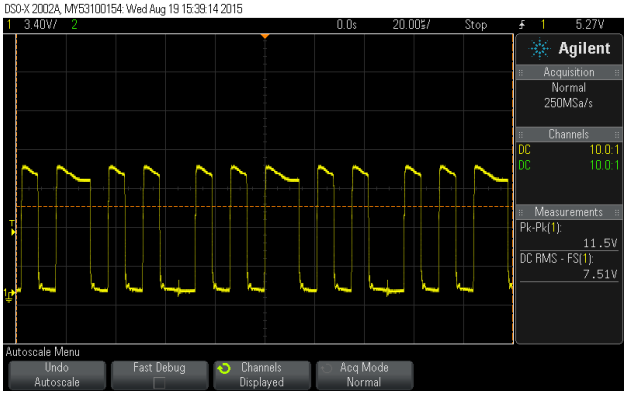

Figure 12: Pulses to S_{L11}

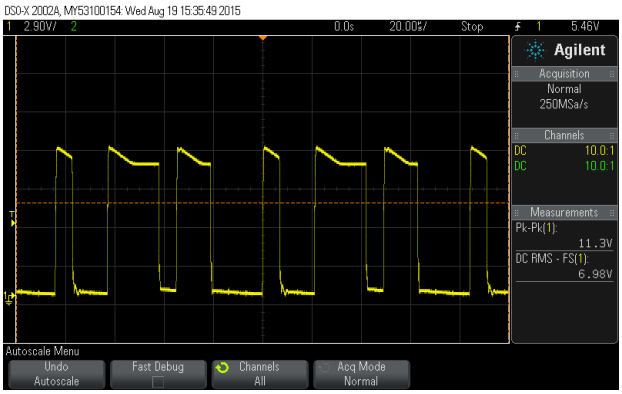

Figure 13: Pulses to S_{R11}

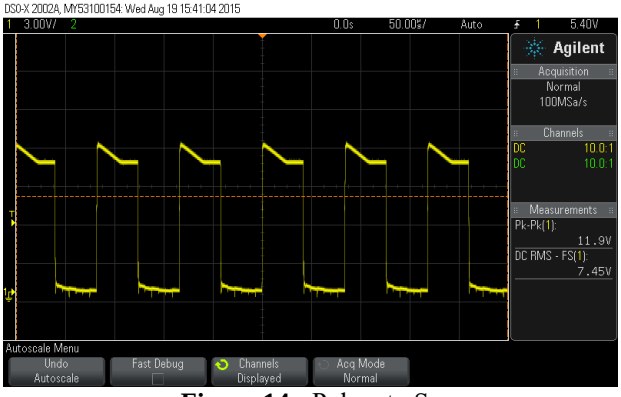

Figure 14: Pulses to S_a

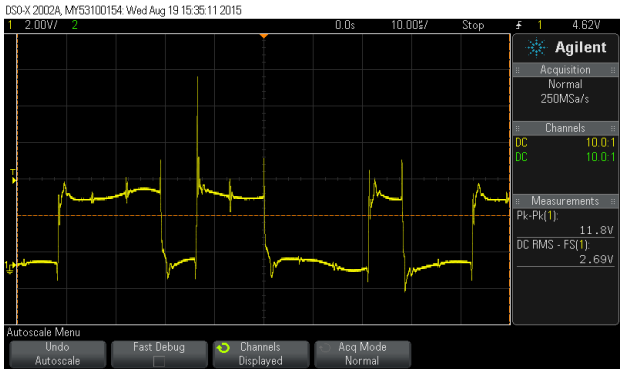

Figure 15: Voltage stress across S_{L11}

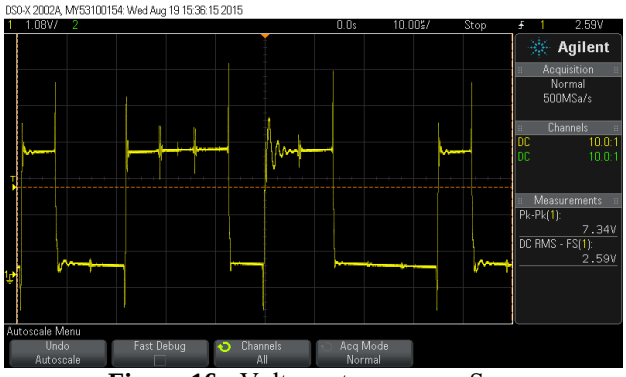

Figure 16: Voltage stress across S_{R11}

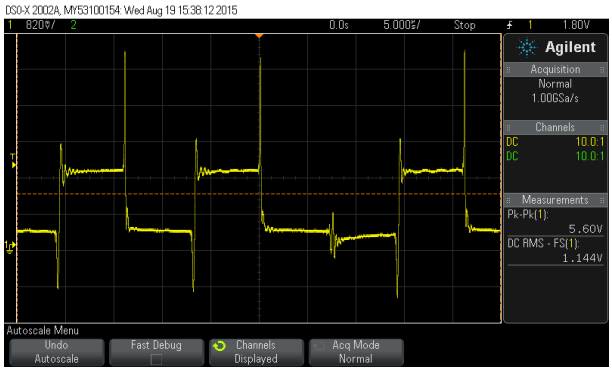

Figure 17: Voltage stress across S_a

The output voltage waveform obtained having 49 levels is shown in Fig. 18. The output voltage obtained have 24 positive levels, 24 negative levels and a zero level. The output voltage waveform is similar to the waveform obtained using simulation. The output voltage obtained is having a peak to peak of 99 V and amplitude as 44.5 V. Th theoretical value is peak to peak 96 V and top value as 48 V. Therefore they are approximately equal.

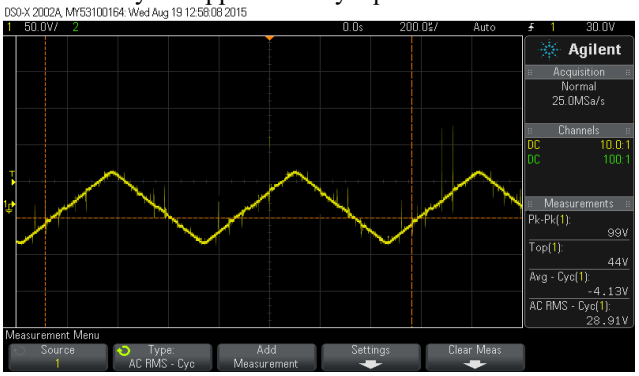

Figure 11: Cascaded multilevel inverter output voltage (Asymmetric)

6. Conclusion

The main advantage of this cascaded multilevel inverter is increasing the number of output voltage levels by decreasing the number of IGBTs, power diodes, driver circuits, and dc voltage sources. Here the cascaded multilevel inverter with developed H bridge unit in symmetric and asymmetric topologies were compared using simulation and the asymmetric topology is found better than symmetric topology since it has more no: of levels and reduced THD. The hardware for asymmetric topology in single stage and with two stages were Set up separately and output waveforms were obtained. The output waveforms obtained were similar to the sim-ulation. The maximum no:of levels obtained using the inverter is 49 levels that is 24 positive levels, 24 negative levels and zero level. In addition, in this inverter, the amount of the blocked voltage by switches is lower than the most of the presented topologies in other papers, except the H-bridge cascaded multilevel inverter.

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