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A Novel Single Phase Eleven-Level Grid-Connected Transformerless Converter Topology for PV Systems

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Abstract: ***The multi-level inverters are used in high power and medium voltage applications, since 1975 and are gaining much attention due to numerous advantages like common mode voltage, operation at both fundamental and high switching frequency, drawing input current with low distortion, reduced harmonic distortions. This paper proposes a single-phase eleven level transformerless grid-connected photovoltaic converter. The common-mode leakage current is minimised using a transient circuit and efficiency is improved by regulating flying capacitor voltage with suitable switching strategy. Simulation results show the effectiveness of the proposed topology.***

Keywords: Photovoltaic (PV) systems, Cascaded H Bridge multilevel inverter (CHBMLI), Pulse width modulation (PWM) inverters, Leakage current, grid connected.

1. Introduction

The demand for electricity is ever growing, fast depletion of fossil fuels, skyrocketing prices of oil, environmental impact, green house effects had led to an alternative source for power generation. Renewable energy sources like, solar energy, wind energy, tidal, Fuel cell, overcomes the above mentioned drawbacks. Photovoltaic (PV) cells convert solar energy to electrical energy by Photovoltaic effect. Though, sunlight is not available continuously, solar energy is used due to its vast availability. PV systems are accepted to be in top position among all renewable electric power generation as it generates direct current electricity without many environmental effects and pollution [1].

The dc power generated from the PV system is converted to ac power, interfacing a PV inverter and then fed into the grid [2]. The multilevel inverter [MLI] has several advantages over the conventional hard switched, two level pwm inverters, like nearly sinusoidal output-voltage waveforms, output current with better harmonic profile, can operate at high voltage with lower dv/dt per switching, hence low switching losses and high efficiency [3]-[6]. Conventional multilevel inverters are classified as diode clamped multi-level inverter (DCMLI) [7]-[9], flying capacitors multi-level Inverter (FCMLI) [10]-[12] and cascaded H-bridge multi-level inverter (CHBMLI) [13]-[15]. A conventional cascaded H-Bridge multi-level inverter consists of number of inverters connected in series. Each H-Bridge is called as cell, for ‗k' cells connected in series, gives an output of (2k+1) voltage levels. This type of inverters require less number of components as compared to other two and so it weighs less and costs less [16]. This paper proposes an eleven level cascaded H-Bridge multi-level inverter consisting of only two cells. The DCMLI used in various applications like dynamic voltage restorers, unified power flow controllers, and static synchronous compensators [17]-[19]. The FCMLIs are used with transmission, distribution as static compensators, distribution static compensators [20], [21]. The CHBMLI‗s are used for high power applications like flexible AC transmission systems, static VAR compensators, series compensation, power line conditioning, interfacing PV systems with grid, voltage balancing and phase shifting [22]. J. Selvaraj et al. proposed a five level MLI with boosting capability using five switches, four diodes and two dc bus capacitors, all connected in series [23]. A seven level MLI was proposed [24], consisting of two bidirectional switches and H bridge in series with three dc- bus capacitors. CHBMLI‗s interfacing PV system with grid or standalone application is proposed [25]-[29]. With different supply voltages, for each full bridge of CHBMLI (asymmetric CFB‗s), the number of switches per output voltage level ratio can be reduced [30].

The proposed topology comprises of two asymmetrical CFB‗s, producing eleven output voltage levels, One CFB is fed by dc voltage source, while the second CFB is fed by flying capacitor. By carefully governing the ratio of two voltages, output voltage level of different sets can be achieved. To reduce ground leakage currents, two additional low power switches and a line frequency switching device (Transient circuit) is included in final topology.

This paper is arranged in the following way: The proposed converter topology and PWM control strategy to maximize the performance, using a low-cost digital signal processor (DSP), is presented in Section II. Flying capacitor regulation, to feed the CFB‗s second full bridge is dealt in Section III. Section IV explains the Operating principle to reduce leakage current. Section V presents the simulation results, and finally section VI concludes the paper.

2. Cascaded H Bridge Multi Level Inverter

A PV system is connected to the grid, interfaced by a CHBMLI. The block diagram of PV system connected to grid through CHBMLI is shown in Fig.1

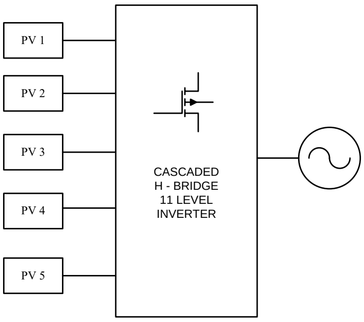

Figure 1: Block diagram of Grid connected PV system

A conventional CHBMLI comprises of a number of H-bridge inverter cells (H-BIC) connected in series with separate dc source each. Three different ac voltage levels $+V_{dc}$, 0 and $-V_{dc}$ respectively can be produced by HBIC at the output terminals by different combination of four IGBT switches S-1, S-2, S-3 and S-4. These switches have low blocking voltage and have high switching frequency. The net ac output voltage of CHBMLI is the sum of output of all individual H-BIC's. Approximately sinusoidal output voltage can be produced by connecting adequate number of H-BIC's and using a suitable modulation scheme. The circuit diagram of a conventional 11 level CHBMLI is shown in Fig.2

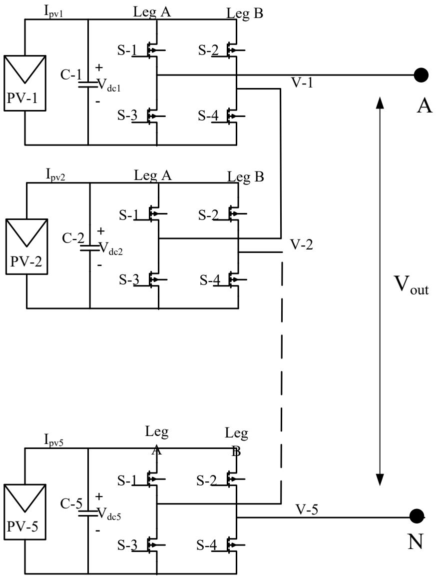

Figure 2: Conventional 11 level CHBMLI

The number of levels obtained from a cascaded inverter is given by $m = 2S + 1$, where m is output phase voltage level, and S is the number of the sources. For example, 11-level CHBMLI will have five H-BIC's and five separated dc sources. The output phase voltage is obtained by the summing up, five H-BIC's output, i.e., $V_{AN} = V_1 + V_2 + V_3 + V_4 + V_5$. The output of an 11 level CHBMLI is shown in Fig.3

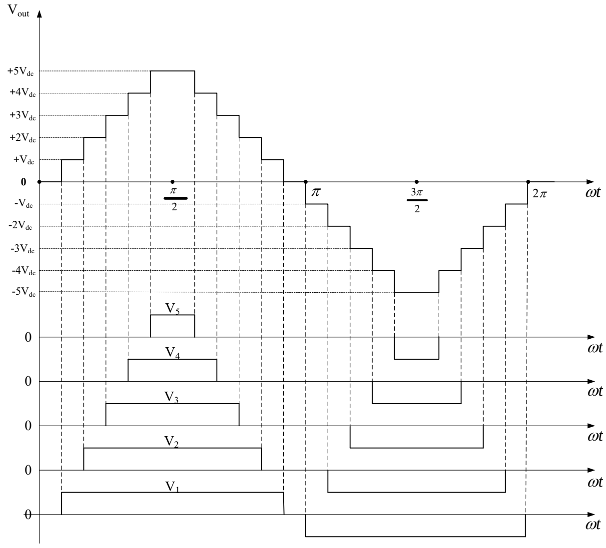

Figure 3: Output Voltage levels of an 11 level CHMLI

CHBMLI are perfect, with non-conventional energy sources with an ac grid, as each H-BIC needs separate dc source. For main traction drives in electric vehicles, CHBMLI are proposed as numerous batteries or ultra-capacitors are well matched to serve as separate dc sources.

3. Proposed Eleven-Level CHBMLI Topology

The proposed single phase eleven level CHBMLI consists of two H-BIC's, the former being supplied by a PV generator and the later fed by flying capacitor. This paper presents a unique PWM strategy, that allows grid connected operation with transformerless converter for the proposed topology, this strategy improves the efficiency by using two legs consisting of, Insulated-gate bipolar transistors with antiparallel diodes in the legs, where high-frequency hard switching commutations occurs. For grid connected operation, phase wire connects an H-BIC, a LC filter and the grid, neutral wire is connected to the other below full H-BIC leg.

The full bridge is supplied by a dc link called High Voltage Full Bridge (HVFB), the other full bridge consisting of flying capacitor.

The major task is the transfer of active power to the electrical grid while using a grid-connected PV converter, controlling the voltage of the flying capacitor is crucial. By choosing the operating zone of the converter depending on the instantaneous output voltage request flying-capacitor voltage V_{fc} is regulated correctly.

Described the following sections, this paper proposed topology of PWM control strategy by using; IGBTs With fast anti n parallel diodes are needed 4 legs. (High-frequency hard switching commutations occur).

The circuit diagram of proposed 11 level CHBMLI is shown in Fig.4.

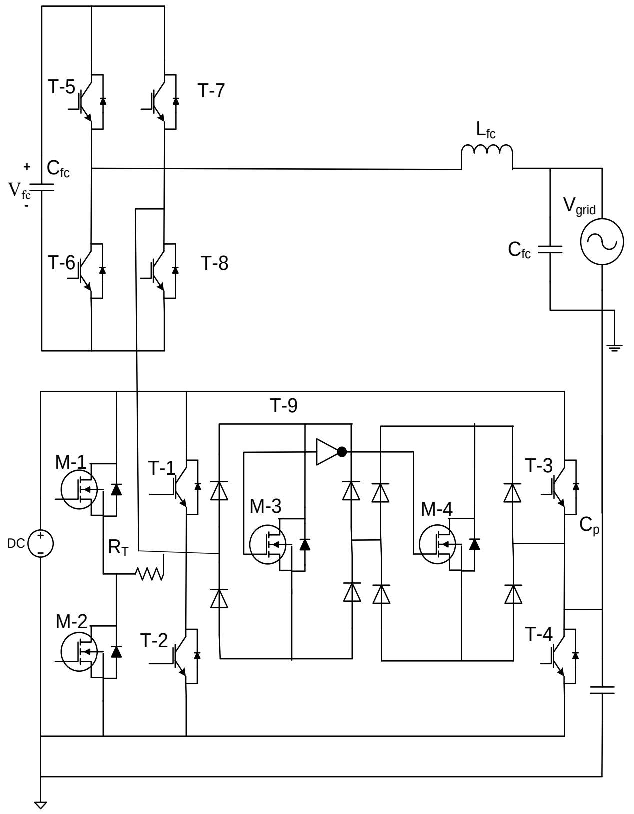

Figure 1: Proposed topology of a 11 level CHBMLI with a Flying Capacitor

Capacitive coupling extracts common mode current which is inversely proportional to switching frequency of the neutral connected leg. Converter operates in different output voltage zones, output voltage switches between two definite voltage levels. Operating zone boundaries change as per dc-link and flying capacitor voltages, also the adjacent zones may overlap as shown in Fig.5. Different operating zones of a 11 level inverter is shown in Fig.5

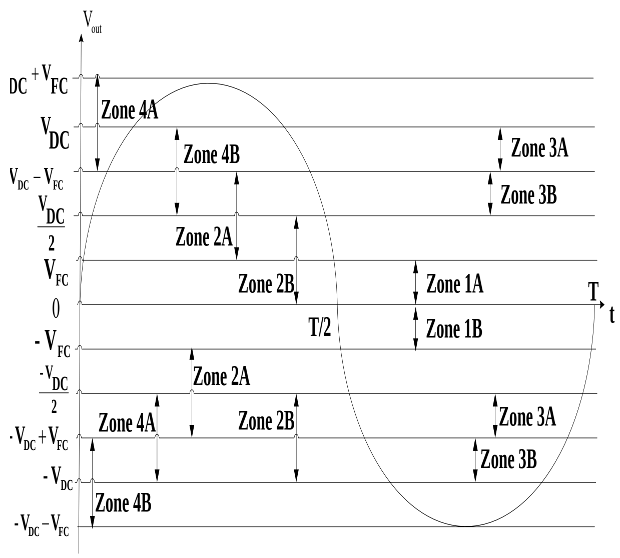

Figure 2: Different operating zones of a 11 level inverter

Table 1: Zonewise Output voltages and switches configuration

Zone	Output Voltage	Devices		
		On	Off	Switching
Zone-4A	$(V_{DC}-V_{fc})$ to $(V_{DC}+V_{fc})$	T1,T4,T8	T2,T3,T7	T5,T6
Zone-4B	$(V_{DC}/2)$ to $(V_{DC}-V_{fc})$	T1,T4,T7	T2,T3,T8	T5,T6
Zone-3A	$(V_{DC}-V_{fc})$ to (V_{DC})	T4,T8	T3,T7	T1,T2T5,T6
Zone-3B	$(V_{DC}-V_{fc})$ to $(V_{DC}/2)$	T4,T7	T3,T8	T1,T2T5,T6
Zone-2A	(V_{fc}) to $(V_{DC}-V_{fc})$	T1,T8	T2,T7	T4,T3,T5,T6
Zone-2B	(0) to $(V_{DC}/2)$	T1,T7	T2,T8	T4,T3,T5, T6
Zone-1A	(0) to (V_{fc})	T2,T4,T8	T1,T3,T7	T5,T6
Zone-1B	$(-V_{fc})$ to (0)	T1,T4,T7	T2,T4,T8	T5,T6
Zone-2A	$(-V_{fc})$ to $(-V_{DC}+V_{fc})$	T2,T7	T1,T8	T3,T4,T5,T6
Zone-2B	$(-V_{DC}/2)$ to $(-V_{DC})$	T2,T8	T1,T8	T3,T4,T5, T6
Zone-3A	$(-V_{DC}/2)$ to $(-V_{DC}+V_{fc})$	T3,T8	T4,T7	T1,T2,T5,T6
Zone-3B	$(-V_{DC}-V_{fc})$ to $(-V_{DC})$	T3, T7	T4,T8	T1,T2,T5,T6
Zone-4A	$(-V_{DC}/2)$ to $(-V_{DC})$	T2,T3,T8	T1,T4,T7	T5,T6
Zone-4B	$(-V_{DC}+V_{fc})$ to$(-V_{DC}-V_{fc})$	T2,T3,T7	T1,T4,T8	T5,T6

Converter can be operated in different operating zones, which depend upon dc-link and flying capacitor voltage, output voltage changes between two specific levels. The flying capacitor voltage contribution to the converter output voltage is positive in zone ‗A', whereas it is negative in zone ‗B'. The switching pattern depends upon the instantaneous fundamental component of output voltage V_{out}^{*}, measured values of flying capacitor voltage V_{fc} and Dc voltage V_{DC}. The converter can produce 11 - output voltage levels by choosing $V_{fc} = \frac{V_{DC}}{4}$.

The grid connected PV system has to transfer active power to grid and controlling the flying capacitor voltage is crucial. As per the required output voltage level, V_{fc} is controlled by selecting the operating zone, depending on these zones V_{fc} can be added or subtracted from the HVFB voltage, during which the capacitor gets charged or discharged. During injecting positive value of current to the grid, the flying capacitor is charged in ‗B' zones and discharged in ‗A' zones. With different switching configuration, the same output voltage can be generated, controlling V_{fc} the converter can be made to operate more in ‗A', zone when V_{fc} is more than a reference value, more in ‗B', zone when V_{fc} is less than a reference value. The explanation would be similar during injecting negative value of current to the grid. Zone ‗A', Zone ‗B', operation is determined by V_{fc}, understood by hysteresis control. The path for current flow by regulating V_{fc}, during charging and discharging of flying capacitor is shown in Fig.5 a & b.

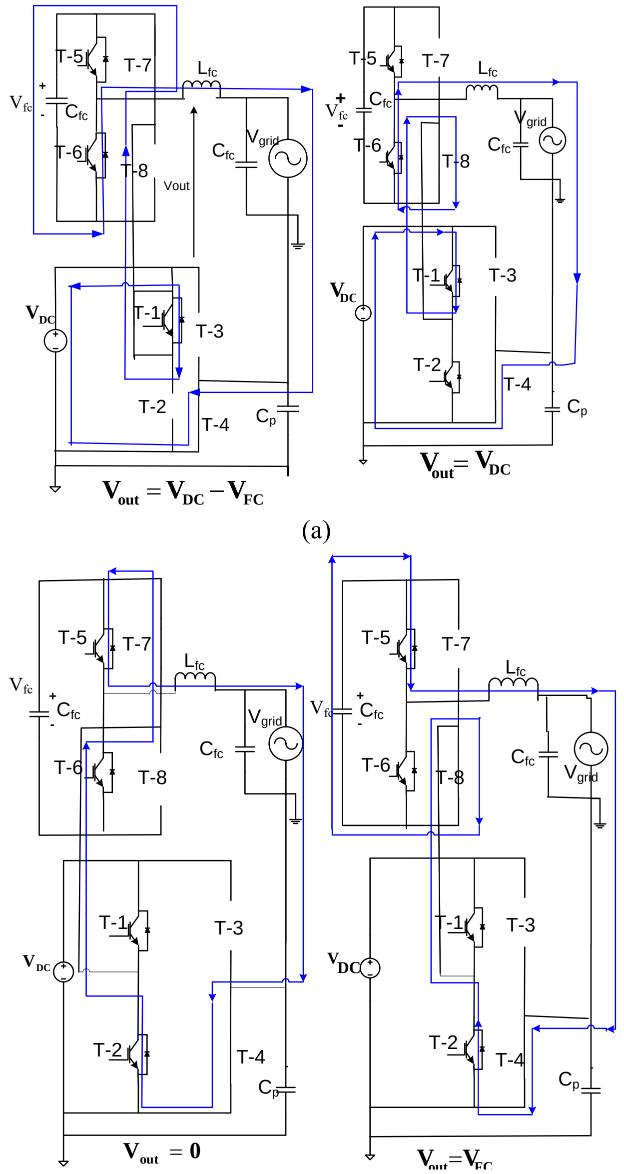

Figure 6: (a) Flying capacitor charging path (b) Flying capacitor discharging path

The above Fig presents control of V_{fc} with positive grid current, $V_{out} > 0$ and $V_{fc} < 0.5V_{DC}$ .If V_{fc} is very small, output voltage level V_{fc} will be replaced with $(V_{DC} - V_{fc})$, hence switching will be between 0 and $(V_{DC} - V_{fc})$, i.e., as in Zone 2B, Fig.5(a) .Likewise, if V_{fc} is very large, output voltage level $(V_{DC} - V_{fc})$ will be replaced with V_{fc}, hence switching will be between V_{fc} and V_{DC}, i.e., as in Zone 2A, Fig.5(b). When $V_{fc} < 0.5V_{DC}$, to minimise current ripple, Zone 3 is chosen when $V_{fc} < V^*_{out} < (V_{DC} - V_{fc})$ limiting level skipping, which occurs when $V_{fc} > 0.5V_{DC}$, therefore Zone A or B can be selected as per voltage algorithm. The converter should be able to work for any vale of (V_{fc}, V_{DC}) condition, as the dc-link voltage can change suddenly due to MPPT approach. The output voltage distortion is minimized by on-line duty cycle computation, the capability of the converter to adjust the flying-capacitor voltage at different operating conditions is important.

For simulations, the grid voltage V_{grid} is sinusoidal having a magnitude of $230\sqrt{2}$. Consider a switching pattern of Table.1, where T3, T4 switch ON at grid frequency and switching OFF at zero crossing of V_{grid} . T4 opens and T3 closes when zero crossing with negative derivative is considered, hence the neutral wire voltage changes from zero to V_{DC} . Because of this, switching causes large surge of leakage current that damages the PV module and decreases the power quality. A transient circuit is designed to reduce the surge current. For better understanding the behaviour of transient circuit, distributed capacitance of PV source is represented with a equivalent parasitic capacitance (C_P) connected between the dc link negative pole and ground. The transient circuit contains two MOSFET‘s M1, M2, bidirectonal switch T9 and resistor R_T . During the operation of converter at Zone 1, the output voltage of HVFB is zero, which is achieved by switching T1 and T3 or T2 and T4 ON, for transient circuit operation at this zone, T1, T2, T3, and T4 are all switched OFF, only T9 is ON, which leads to neutral point floating , keeping the parasitic capacitance (C_P) voltage V_{ground} constant.

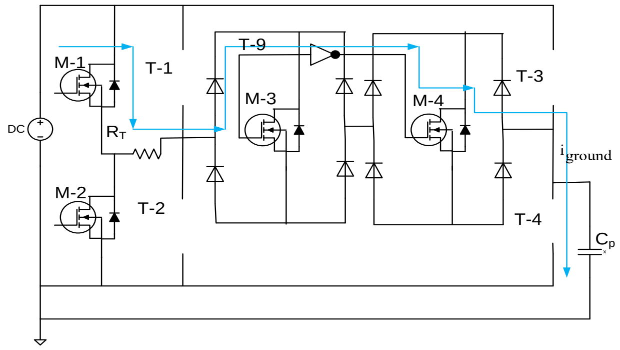

Figure 7: Ground leakage current representation for Transient Circuit

MOSFET, M1 is switched ON if slope of zero crossing is negative, M2 is switched ON if slope of zero crossing is positive, then the parasitic capacitance (C_P) gets charged through R_T , limiting the surge current. The power loss of the resistor in the transient circuit is negligible. The energy lost by charging and discharging th parasitic capacitance (C_P) to V_{DC} over a time period is given by $P_{tc} = (C_P V_{DC}^2)/T$, with C_P = 200nF and V_{DC} =300V. As the output voltage is close is close to grid voltage, the power factor does not influence the transient circuit operation, for correct operation, transient circuit requires grid voltage instantaneous angle which can be acquired by phase-locked loop (PLL) supplied by grid voltage.

4. Simulation Results

The proposed converter was simulated using MATLAB/Simulink, covering broad range of active and reactive power fed to the grid, dc link voltage, and PV parasitic capacitance (C_P), the specifications of different parameters are as follows, dc link voltage V_{DC} =300V, grid sinusoidal voltage V_{grid} =230V, at a frequency 50Hz, the output LC filter consisting of capacitor C_f =1µF, inductor L_f =1.5mH, total distributed grid inductance L_{grid} =40µH, switching frequency of PWM f_S =20kHz, flying capacitor capacitance C_{fc}=500µF, surge limiting resistor R_T =1.5kΩ, current fed to the grid is controlled by proportional integral plus feed forward i_{grid} =8.5A rms.

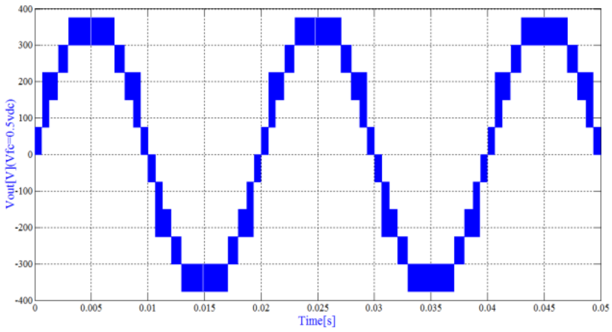

Figure 8: (a) presents the 11-level output voltage for the proposed converter with respect to time

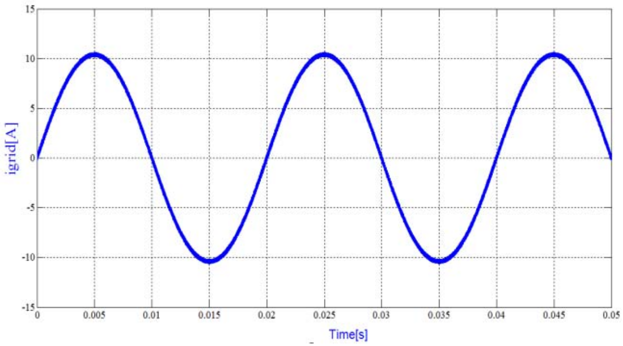

Figure 9: (b) presents the output current for the proposed converter with respect to time

The characteristics of the Transient circuit with a Parasitic capacitance of C_P= 200 nF and a ground leakage current of i_{ground}= 30 mA rms. The ground leakage current can be further reduced by proper design of the common mode filter.

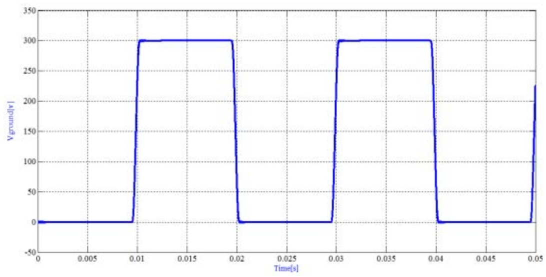

Figure 3: Ground voltage for the transient circuit with 200nF capacitor

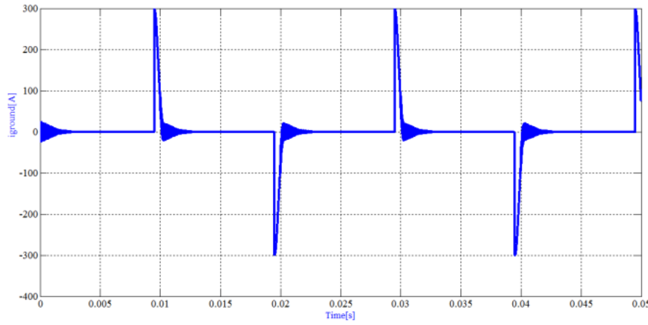

Figure 11: Ground current for the transient circuit with 200nF capacitor

The characteristics of step variation for V_{fc} from 180 to 200 V occurring at a time of 0.1 s. The V_{fc} average value rises to reference value without overshoot.

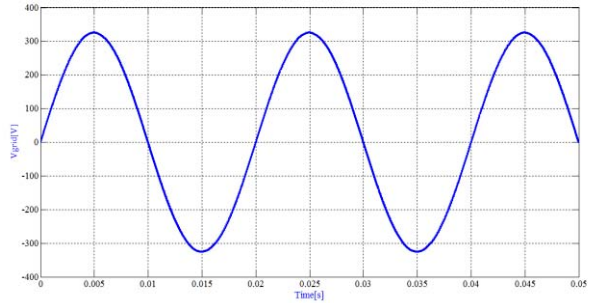

Figure 12: Grid voltage for $0.5V_{fc}$

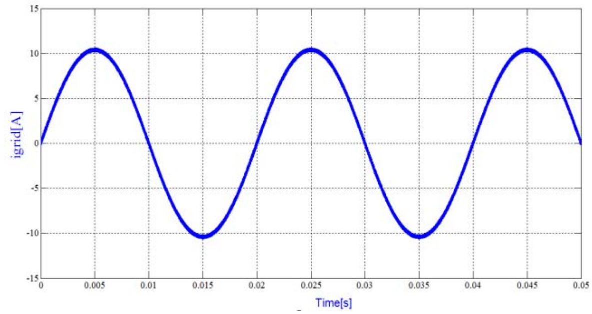

Figure 13: Grid voltage for 0.5Vfc

5. Conclusion

This paper proposes a novel single-phase eleven level transformerless grid-connected photovoltaic converter, consisting of two H-BIC's one is supplied by flying capacitor. The efficiency is improved by developing a suitable PWM strategy and ground leakage current is minimised using a definite transient circuit. Simulation results show the effectiveness of the proposed topology.

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