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Low Phase Noise Ring Oscillator Using Current Steering Technique

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Abstract: ***The design of high performance VCOs has been increasingly more important and still is an active research area. Research on VCOs for the past decade has been concentrated in the areas of higher frequency, lower phase noise, low power, low operating voltage, and increased tuning range. This paper presents the design of CMOS voltage controlled ring oscillator by employing current steering technique. By controlling of coarse or fine controls , the proposed circuit allows limited tuning gain. The lower tuning gain can be less sensitivity voltage which is available at control lines. The proposed delay cell design determining the best possible Configuration for the ring oscillators having the least power consumption and precise delay with lesser sensitivity to the variations in the temperature and supply voltage for frequencies of GHz. Tuning ranges for the proposed multi loop ring oscillator topology have been designed at frequencies from 2.163 GHz to 6.5 GHz in Cadence Virtuoso Tool using 180nm technology with current of 12mA.***

Keywords: CMOS, coarse/fine tuning, multiloop, phase noise, ring oscillator, VCO.

1. Introduction

Now in a day, any communication system needs higher data rates like optical and data link systems. Low noise high frequency VCO are most prominent when we need to design transmitter and receiver blocks in any communication system like optical communication systems or system on chips etc with SATA in data transfer / Storage systems. Generally ring oscillator is very easy to implement its architecture and needs very lesser die area when compared with inductance – capacitance oscillators. In recent days, the technology is going to scale down, as a result low power supply voltage came into existence. The existed tuning schemes leads to the results in more VCO voltage to frequency gain and this VCO voltage to frequency gain further increases the oscillator noise sensitivity. To avoid such these problems like more noise sensitivity in oscillators, different methods have been developed and came into existence such as to implementation of fine/coarse frequency tuning inductance – capacitance tuned oscillators and ring oscillators to provide a maintaining of tuning range more wider as well as tuning gain as moderate. Coarse tuning can be provide by varacter banks which are digitally switched in inductance-capacitance tuned oscillators as well as fine frequency tuning also provided by varacter banks. Generally in almost ring oscillators , tail current of the whole given circuit can be controlled for implementation of coarse/fine tuning , but the above problems when rises in ring oscillators, it leads to risk of up conversion of 1/f noise which is from the tail current which can be flowed through source transistors.

The multi loop technique is used to increase the operating frequency of the circuit to a maximum value. By controlling the current which is flowing through the positive feedback cross coupled nmos pair which includes in self balancing it can implement the fine tuning. The drain current of the positive feedback latched transistors reduces very significantly due to the smaller size of these feedbacks latched transistors. Even there noise up conversions make a less impact (which is also negligible) on noise performance of the given complete circuit.

2. Ring Oscillator Topology and Design

Conventional Delay Cell for Ring Oscillator

The schematic entry of the conventional delay cell is shown in below fig 1. In the below circuit, the transistors nmos N1 and N2 makes the inputs to the primary loops where as pmos transistors P5 and P6 makes the inputs to the secondary loops. The pmos transistor P1 or P2 serves as a load of the delay cell. When is **P+** lower than **Vtn**, transistor N1 shuts off. Since the input voltage at is **VS+** earlier than **VP+,** the secondary input transistor P5, will already be conducting its source current to the load capacitor at the output node **OUT-** . As a result, the time for the output node to rise from low to high is decreased.

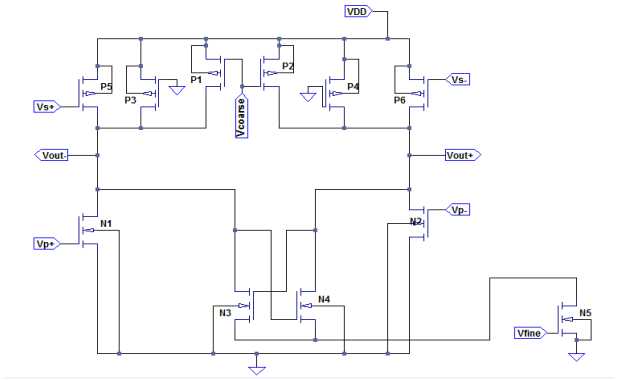

Figure 1: Conventional Delay Cell

The tail's current which is flowing through source transistors avoided in the above delay cell because of too keep the signal swings are maximum which in turn benefit for the SNR ratio. To reduce the levels of oscillations at the

extremes of the frequency tuning. The pmos transistor P3 and p4 acts as load are added extra in parallel with controllable pmos loads P1 and P2. In the conventional delay cells , the gate terminals of pmos transistors P3 and P4 connects to GND for the operation of P3 and P4 in linear region. Coarse tuning can be achieved by changing by changing the load through varying gate terminal voltage of P1 or P2 where as fine tuning can be accomplishes by controlling of the tail current which is flowing through the positive feedback latched transistors N3 and N4.

Proposed Delay Cell for Ring Oscillator

Figure2 shows the proposed delay cell designed by employing current steering technique. In conventional delay cell transistors P3, P4 always turned on, because of continuous current flow. So, conventional delay cell circuit consumes more power. In order to reduce power consumption this proposed delay cell uses current steering technique. By removing the transistors P3 and P4 and introducing the new transistor N6 between the transistors N1 and N2. Due to this there will be power reduction. In this proposed design there will be reduction of tuning sensitivity and the low-frequency noise up-conversion.

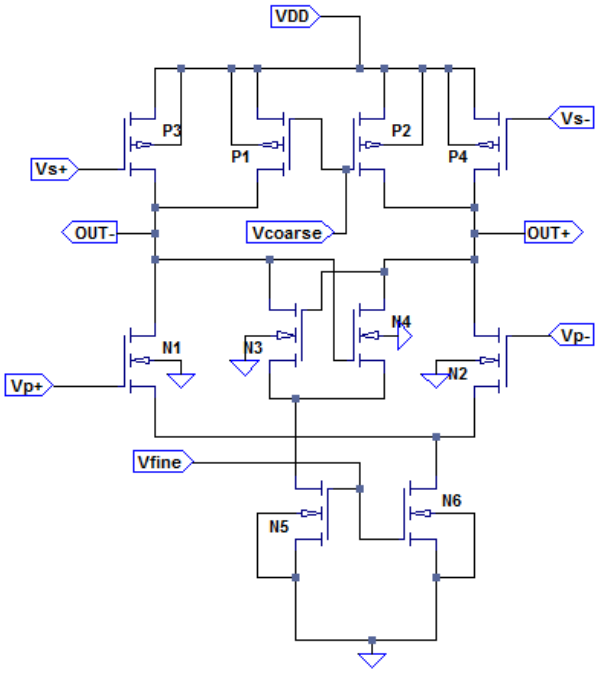

Figure 2: Proposed Delay Cell

3. Transistor Sizing

Table 1: Size of Transistors

Transistor	*Width*	*Functionality*
P3,P4	65um	To increase slew rate
P1,P2	70um	Coarse tuning
N1,N2	63um	Input transistors
N3,N4	64.5um	Cross coupled pair
N5,N6	85um	Fine tuning

Multi loop Ring Oscillator

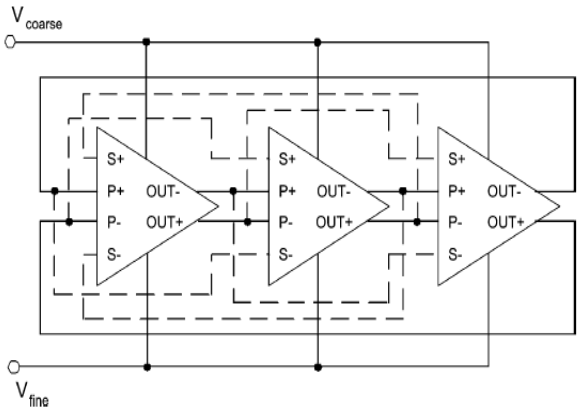

Figure 3: 3 Stage Multi Loop Ring Oscillator

The proposed ring oscillator architecture uses the multi loop techniques. Three staged multi loop ring oscillator is shown in figure 3. The two loops which are primary loop and secondary loops involved in any ring oscillators. Primary loop works like differential ring oscillator whereas the secondary loop gives extra entry into IO transfer function. This additional entry be helped to decreases slew time of output node since the secondary inputs are fed from outputs. These are on a fewer stages prior to current stages.

Different architectural techniques are needed to keep the maximum frequency levels of ring oscillators. Some of different architectural techniques includes the use of sub feedback loops and multi feedback loops etc.

Multi loop architecture which is in fig 3 chooses as basic structure in the proposed work. This multi loop architecture techniques adds the extra feed forward loops. The main work in the proposed method is to decrease the delays of the different stages in multi loop architecture. This reduction of delay can be possible by adding secondary loop inputs S^+ and S^- to every stage in multi loop architecture and switching the secondary inputs earlier than primary inputs during the operation.

Inter coupled feedback in frequency increase different techniques are used to increase maximum frequency which is in similarity with multi loop architecture which is proposed in this work. Phase noise and clock variations have taken into consideration when changing the frequency increase architectures. Most of the ring oscillators uses analog gain stages by keeping the transistors in these analog stages into continuous conduction but in turn which increase to total noise. To reduce this, these transistors can be periodically switch in and out of conduction which reduces noise.

4. Simulation Results

Transient Simulation

A transient simulation is a relatively fast way to verify the functionality of the VCO and estimate its settling time and output frequency. Run a conservative transient analysis for a period of around 10ns. If the oscillations do not start you may need to add an initial condition to one of the output voltages. Plot the output of the oscillator, you can measure the frequency of oscillation using the calculator. Take note

of the time it takes to the VCO to have a stable amplitude since this time will be used in the PSS simulations.

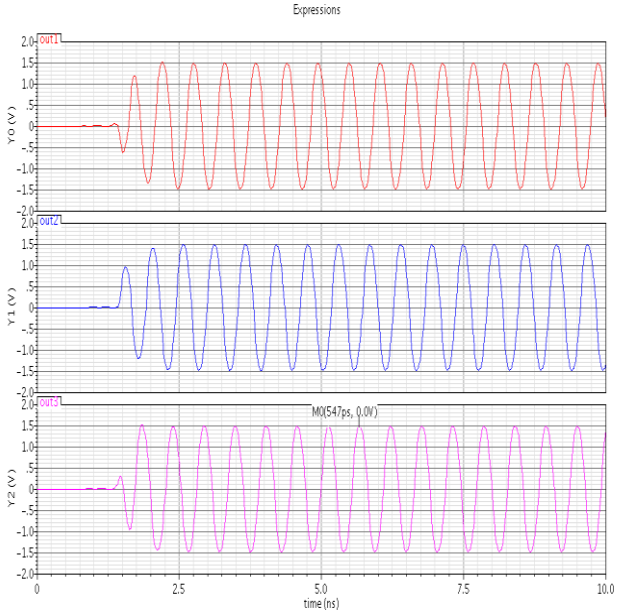

Figure 4: Transient Response of the Ring Oscillator

Periodic Steady State Simulation:

To observe the behavior of the Ring Oscillator with respect to the tuning voltage, a parametric simulation can be used. Set the control voltage as a variable and sweep in the range shown in figure 5. Keep both, the transient and the PSS simulations active. The simulation results (output waveform and phase noise) will show multiple curves.

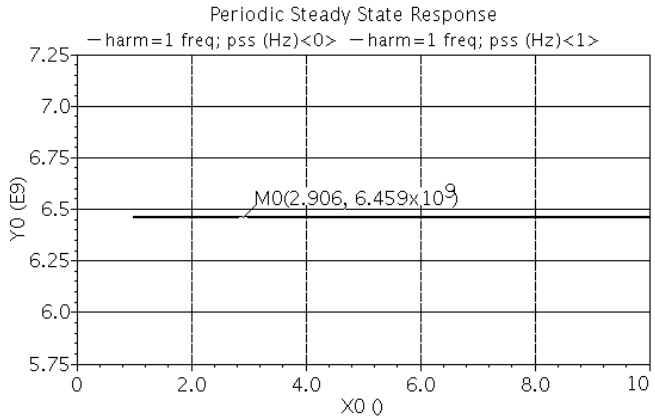

Figure 5: Periodic steady state response at Maximum frequency

Phase Noise at Low Frequencies

Figure 6 shows the Phase noise of 2.1 GHz center frequency at offset of 1MHz.

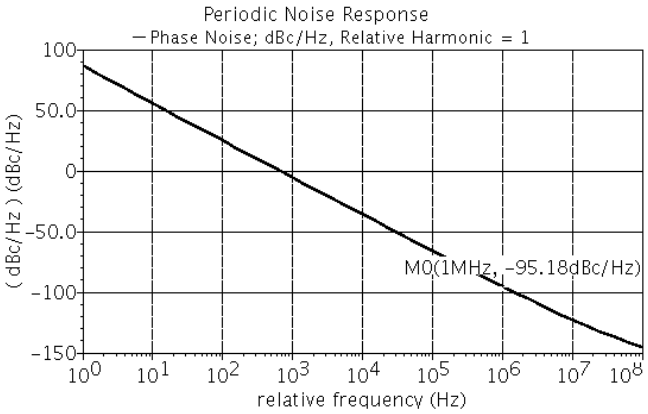

Figure 6: Phase noise of 2.1GHz center Frequency at an offset of 1MHz

5. Comparisons

Table 2: Comparisons between reference delay cell and proposed delay cell

	Parameter	Reference Delay cell	Proposed Delay cell
1	Minimum frequency	2.243GHz	2.163GHz
2	Maximum frequency	5.15GHz	6.5GHz
3	Tuning range	2.243GHz– 5.15GHz	2.163GHz– 6.5GHz
4	Output noise	7uv at 2GHz	4.6uv at 2GHz
5	Phase noise at 1MHz offset	-91dBc/Hz	-93dBc/Hz
6	Current	12.84 mA	12 mA

6. Conclusion

The rapid growth of wireless communication systems has led to a growing demand for RF components, including oscillators, frequency synthesisers, mixers, LNAs etc. One of the most important. One of the main challenges in the design of ring oscillators (ROs) is to increase their oscillation frequency. Generally ring oscillator is very easy to implement its architecture and needs very lesser die area when compared with inductance – capacitance oscillators. In recent days, the technology is going to scale down, as a result low power supply voltage came into existence. The existed tuning schemes leads to the results in more VCO voltage to frequency gain and this VCO voltage to frequency gain further increases the oscillator noise sensitivity.

The design of ring VCO is concentrated from maximum oscillation frequency and tuning range perspective using current steering technique. The ring proposed is giving tuning range of 2.163GHz to 6.5GHz and phase noise at center frequency of 6.5GHz at an offset of 1MHz. Finally the proposed ring oscillator giving improved performance when compared to the reference ring oscillator.

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