Fig 2 shows the circuits based on proposed concept. The first circuit shows the proposed circuit using NMOS as the extra device and the second circuit shows the proposed circuit using PMOS as the extra device.

3. Circuit Implementation

It is found that hold power dissipation is considerable lower in both the cases compared to their conventional counterpart. It is also found that reduction in power dissipation as obtained with the leakage current of an NMOS device such as in proposedcircuit-1 is lower than proposed circuit-2. In case of proposed inverters, it is observed that reduction in static power dissipation is not proportionally transferred to total power reduction. This is understandable from the fact that dynamic power dissipation becomes relatively larger compared to conventional design due to extra node in the proposed technique. Nevertheless, simulation results show that a decrease in static power dissipation is more than an offset created by dynamic power dissipation due to extra node. It is justified from the fact that switching voltage (VC) of extra node is only a little fraction of VDD and thus dynamic power dissipation is inherently lower in the proposed methodology.

The proposed CMOS inverter circuits are similar to that of the conventional inverter; the only difference being the proposed circuits uses two more extra transistors. The proposed circuit–1 uses two extra NMOS transistors in which one of the NMOS is connected in parallel to the inverter configuration and the other transistor is used to connect the node to the ground. The drain of NMOS which is in parallel is connected to Vdd and source to the node Vc. The gate and drain are shorted for this transistor. The proposed circuit – 2 uses an extra NMOS as well as a PMOS transistor which is connected in parallel to the inverter configuration. The drain of PMOS in parallel is connected to the node and the gate and source are shorted and connected to Vdd. The NMOS is used to connect the node to the ground.

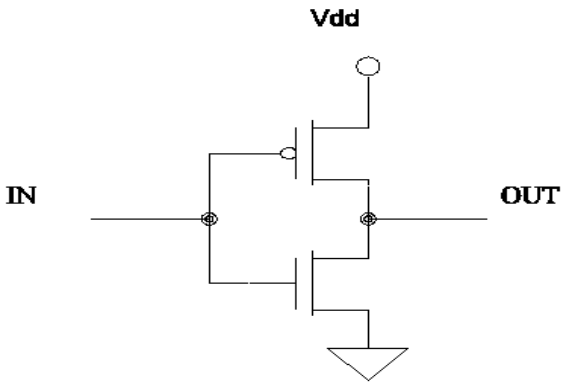

Figure 3: Circuit Schematic of Conventional CMOS inverter

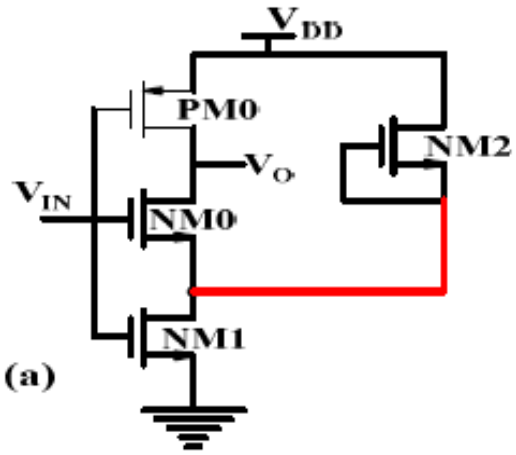

Figure 4: Circuit Schematic of proposed circuit - 1

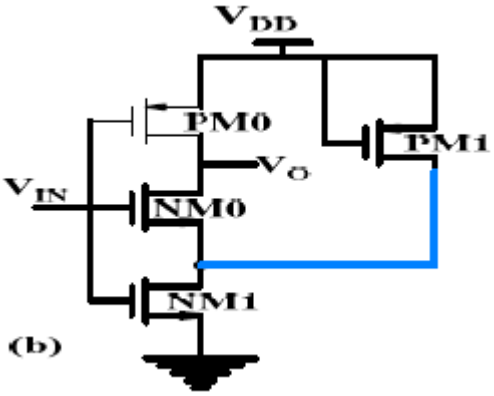

Figure 5: Circuit Schematic of proposed circuit - II

4. Simulation Results

The circuits were simulated using NG spice tool. NG Spice is a mixed-level/mixed-signal circuit simulator. It is the Open Source successor of Spice3f5. A small group of maintainers and the community of motivated users contribute to the NG Spice project by providing new features, enhancements and bug fixes. NG Spice is based on three free software packages: Spice, X Spice and Cider

Applications that are exclusively analog can make use of all analysis modes with the exception of Code Model subsystem that do not implements Pole-Zero, Distortion, and sensitivity and Noise analyses. Event-driven applications that include digital and User-Defined Node types may make use of DC (operating point and DC sweep) and Transient only. In order to understand the relationship between the different analyses and the two underlying simulation algorithms of NG Spice, it is important to understand what is meant by each analysis type.

4.1. Voltage Transfer Curve Simulations

The simulation results of voltage transfer characteristic (VTC) for conventional, proposed circuit-1and circuit-2 are first analyzed. The shape of VTC in proposed circuits is comparable to that happens in conventional one. It is also found that reduction in power dissipation as obtained with the leakage current of an NMOS device such as in proposedcircuit-1 is lower than proposed circuit-2.

Fig.6 shows simulation results of voltage transfer characteristic (VTC) for conventional, proposed circuit-1 and circuit-2. The circuits were simulated using NG spice tool.

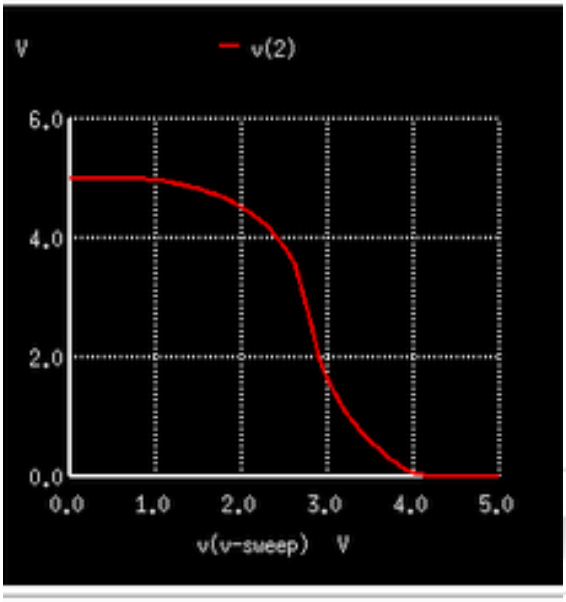

Figure 6(a): VTC of Conventional CMOS inverter

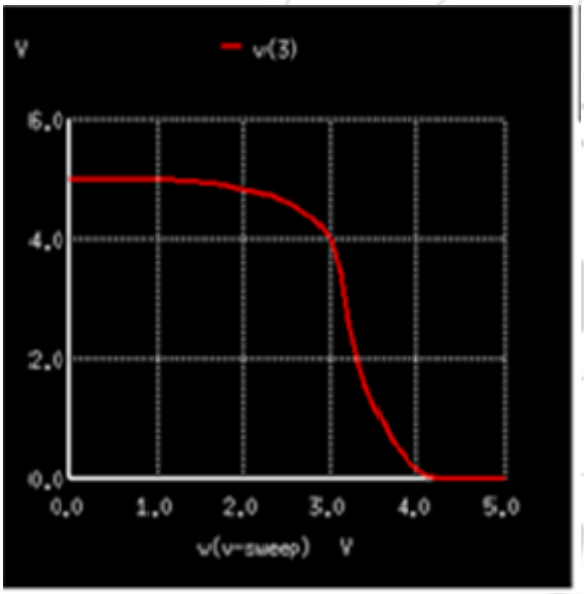

Figure 6(b): VTC of proposed circuit – 1

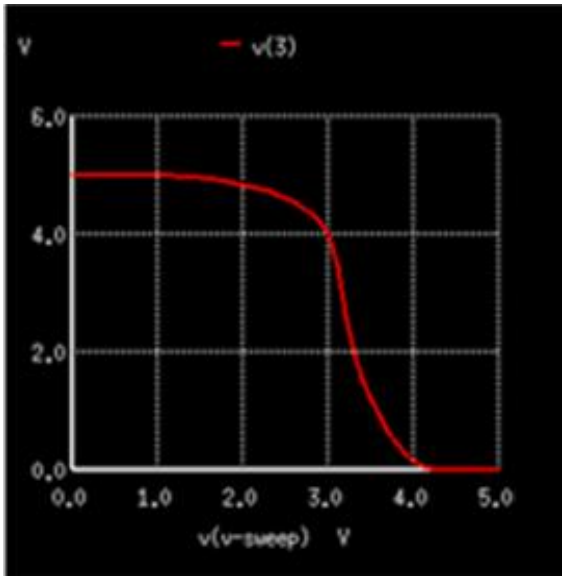

Figure 6(c): VTC of proposed circuit – 2

The Fig 6 shows simulations of Voltage transfer curve for conventional and proposed CMOS inverter circuits. From those simulation results, it's clear that the voltage transfer curves for all the three circuits are similar. It means that when the proposed technique is used, it does not make much difference to the voltage transfer characteristic of the inverter. It also indicates that there is not much change in noise margin irrespective of a slight increase in noise margin in the case of proposed techniques. The voltage transfer characteristics show that the introduction of extra node and device is a better method since there is not much change.

4.2 Substrate Current Simulations

The substrate current of the conventional and proposed inverters is shown in Fig 5 which is used to estimate the power dissipation. Since substrate current is one of the important factor for power dissipation in the dynamic circuits, the simulations of the substrate currents are done and power dissipation is analyzed of the basis of these simulations.

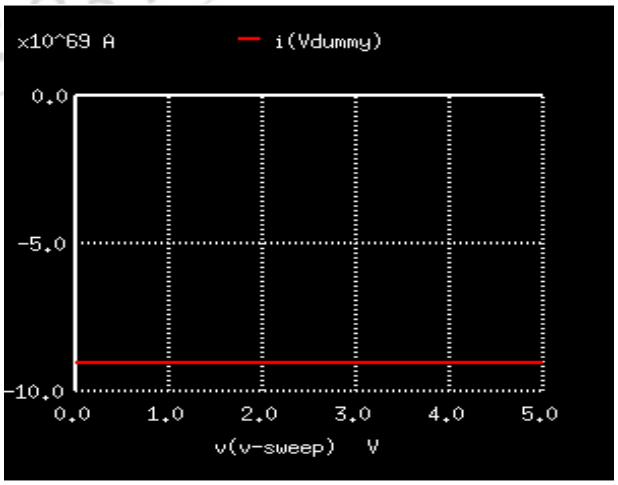

Figure 7(a): Substrate current of Conventional CMOS inverter

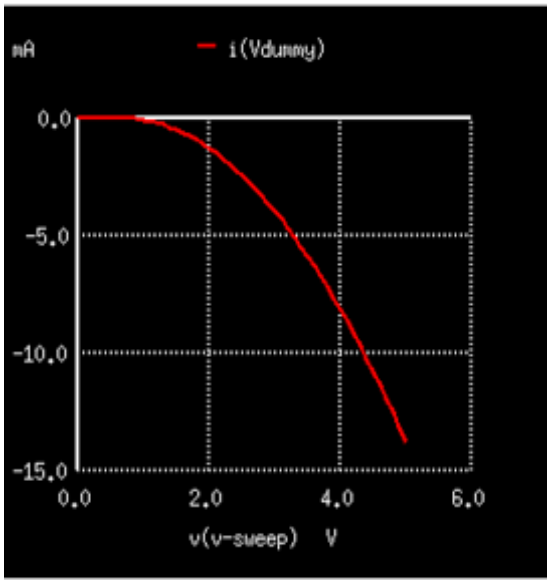

Figure 7(b): Substrate current of proposed circuit – 1

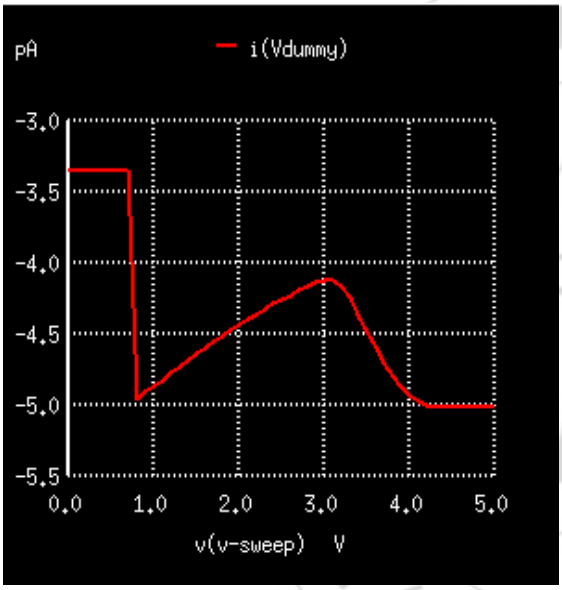

Figure 7(c): Substrate current of proposed circuit – 2

The Fig 7 shows simulations of the Substrate current or leakage current in the case of conventional and proposed inverter circuits. The Fig 7(a) shows the substrate current of conventional inverter which is in the ampere range. The Fig 7(b) shows the substrate current in case of proposed circuit-1 using NMOS where the substrate current is only a few milliampere. This shows that there is significant reduction in substrate current which implies that the proposed technique is capable of reducing the power dissipation. The Fig 7(b) shows the substrate current in case of proposed circuit-2 using PMOS where the substrate current is only a few picoampere. This method reduces the substrate current in picoampere which indicates that the most effective reduction in power dissipation takes place when the PMOS is connected in parallel.

5. Conclusion

Addition of nodes to the circuit and leakage current ofsub-100nm device, although result in larger power dissipation but these can also be integrated in a useful manner in the circuits leading to huge reduction in power dissipation. There is an optimum value of leakage current to be applied at the node, at which power reduction of the circuits becomes maximum. For example, in CMOS inverter, for minimum area, leakage current of single PMOS device results in maximum reduction in power dissipation than leakage current of either an NMOS, or multiple such devices. In addition, with channel length scaling, proposed methodology results in an eligible increase in static power dissipation. All these benefits of the proposed methodology can be attained with much less penalty in speed of operation. In view of the benefits of the proposed methodology as illustrated in this work, it can gain more privileged in low power circuit design for applications especially those operated using power from batteries, and require costly sophisticated cooling mechanism as a means of removing heat from the system.

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Author Profile

Harigovind received the B.Tech degree in Electronics And Communication Engineering from Mahatma Gandhi University, Kerala at Mar Baselios Christian College Of Engineering And Technology 2013 and now he is pursuing his M.Tech degree in VLSI and Embedded systems under the same university in SCMS School of Engineering and Technology, Cochin.

Sarath Mohan KP received the B.Tech degree in Electronics And Communication Engineering from Anna University, Tamil Nadu at Nehru Institute of Technology 2013 and now he is pursuing his M.Tech degree in VLSI and Embedded systems under the Mahatma Gandhi University in SCMS School of Engineering and Technology, Cochin.

Mariya Stephen received the B.Tech degree in Electronics And Communication Engineering from Mahatma Gandhi University, Kerala at Federal Institute of Science and Technology 2013 and now she is pursuing her M.Tech degree in VLSI and Embedded systems under the same university in SCMS School of Engineering and Technology, Cochin.