# Reduction of Static Power Dissipation in CMOS Inverter using Extra Nodes and Substrate Current

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**Abstract:** *High performance VLSI circuit design can be done by miniaturization of device channel length to sub-100nm dimension. But it may result in significantly higher leakage current. The increase in leakage current leads to significant increase in its power dissipation. For the past few years, various methods and device structures are proposed to solve this issue. In this work, we have tried to reduce the static power dissipation by either raising source or falling drain voltage since both lead to a reduction in VDS. CMOS inverter while designed with our proposed technique shows voltage transfer characteristics comparable to the conventional CMOS inverter and results in large reduction in substrate current and thereby reducing static power dissipation.*

**Keywords:** Extra nodes, static power dissipation (PS), substrate current (Isub), voltage transfer characteristic (VTC)

## 1. Introduction

One of the common methods to improve the operational speed of IC is down scaling the channel length of MOSFET. But this method has the drawback that it may result in large power dissipation, mostly because of the high leakage current due to short channel effects. Some of the common methods used to overcome this drawback are to use devices like Silicon-on-Insulator MOSFET (SOI MOSFET) and FinFET. But all these alternative devices require a relatively complex processing and thus circuit fabrication. Use of extra circuit elements to change the critical parameters can lead to a significant reduction in power dissipation at circuit level. But this technique has a drawback of area overhead. Moreover, the circuit technique requires peripherals of extra devices, complex voltage reference circuit, extra-long wire interconnections and also multiple supply voltage which themselves consumes much power and thus need optimizations. Such techniques would be beneficial only if these peripherals can be economical both in terms of their design and fabrication.

The proposed method integrates only few or one extra node with mother circuit. Here, to test the proposed methodology, we have used conventional CMOS inverter. We know that CMOS technology is popular for zero or negligible static power dissipation, but when designed with sub-100nmchannel length devices, its static power dissipation increases. However, with proposed methodology, the rate of increase in static power dissipation becomes negligible and the modified circuit works like the conventional one with reduced power dissipation.

## 2. Proposed Technique

Large static power dissipation in short channel devices is due to huge sub threshold leakage current of such devices due to severe SCEs. The leakage current in long channel device can be expressed as

$$I_{sub} = I_{D0} \times e^{\frac{V_G}{mV_T}} \times \left(e^{-\frac{V_S}{V_T}} - e^{-\frac{V_D}{V_T}}\right)$$

Sub threshold leakage current increases significantly in sub-100nm devices due to SCEs such as DIBL effects. It is well known that Isub and thus static power dissipation can be reduced through minimization of DIBL effects by either raising source or falling drain voltage since both lead to a reduction in VDS. For this purpose, we add an extra node of non-zero voltage at source of the device(s) and joined the node with GND by an NMOS device such that the complementary action in CMOS technology is retained. This is shown inFig.1
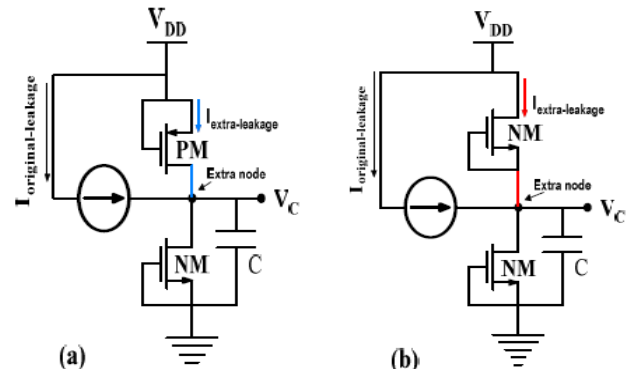


**Figure 1:** Circuit Schematic of controller circuit using leakage current of (a) PMOS, (b) NMOS
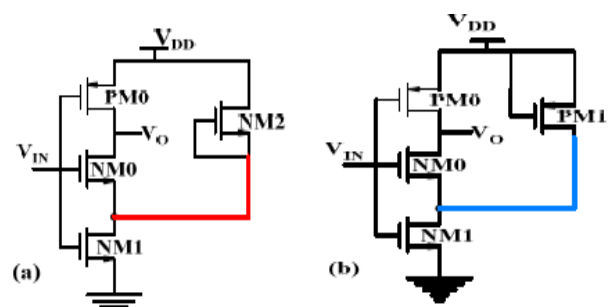


**Figure 2:** Circuit schematic of inverter (a) proposed circuit-1, (b) proposed circuit-2

Fig 2 shows the circuits based on proposed concept. The first circuit shows the proposed circuit using NMOS as the extra device and the second circuit shows the proposed circuit using PMOS as the extra device.

## 3. Circuit Implementation

It is found that hold power dissipation is considerable lower in both the cases compared to their conventional counterpart. It is also found that reduction in power dissipation as obtained with the leakage current of an NMOS device such as in proposedcircuit-1 is lower than proposed circuit-2. In case of proposed inverters, it is observed that reduction in static power dissipation is not proportionally transferred to total power reduction. This is understandable from the fact that dynamic power dissipation becomes relatively larger compared to conventional design due to extra node in the proposed technique. Nevertheless, simulation results show that a decrease in static power dissipation is more than an offset created by dynamic power dissipation due to extra node. It is justified from the fact that switching voltage (VC) of extra node is only a little fraction of VDD and thus dynamic power dissipation is inherently lower in the proposed methodology.

The proposed CMOS inverter circuits are similar to that of the conventional inverter; the only difference being the proposed circuits uses two more extra transistors. The proposed circuit–1 uses two extra NMOS transistors in which one of the NMOS is connected in parallel to the inverter configuration and the other transistor is used to connect the node to the ground. The drain of NMOS which is in parallel is connected to Vdd and source to the node Vc. The gate and drain are shorted for this transistor. The proposed circuit – 2 uses an extra NMOS as well as a PMOS transistor which is connected in parallel to the inverter configuration. The drain of PMOS in parallel is connected to the node and the gate and source are shorted and connected to Vdd. The NMOS is used to connect the node to the ground.
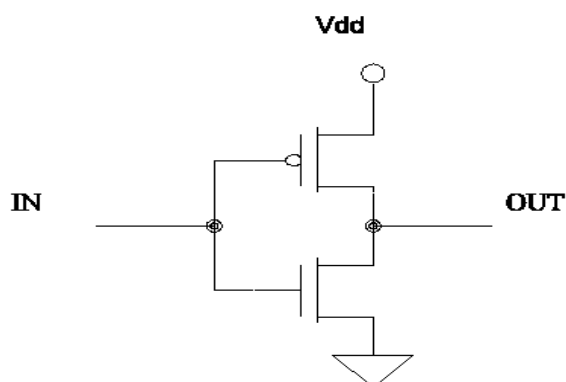


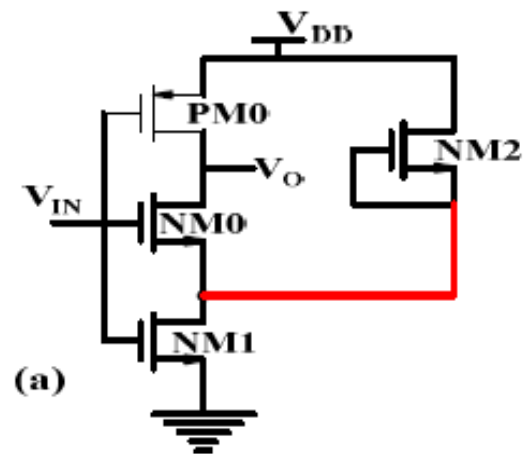**Figure 3:** Circuit Schematic of Conventional CMOS inverter



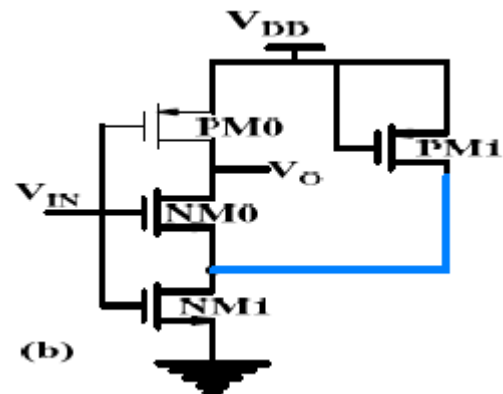**Figure 4:** Circuit Schematic of proposed circuit - 1



**Figure 5:** Circuit Schematic of proposed circuit - II

## 4. Simulation Results

The circuits were simulated using NG spice tool. NG Spice is a mixed-level/mixed-signal circuit simulator. It is the Open Source successor of Spice3f5. A small group of maintainers and the community of motivated users contribute to the NG Spice project by providing new features, enhancements and bug fixes. NG Spice is based on three free software packages: Spice, X Spice and Cider

Applications that are exclusively analog can make use of all analysis modes with the exception of Code Model subsystem that do not implements Pole-Zero, Distortion, and sensitivity and Noise analyses. Event-driven applications that include digital and User-Defined Node types may make use of DC (operating point and DC sweep) and Transient only. In order to understand the relationship between the different analyses and the two underlying simulation algorithms of NG Spice, it is important to understand what is meant by each analysis type.

### 4.1. Voltage Transfer Curve Simulations

The simulation results of voltage transfer characteristic (VTC) for conventional, proposed circuit-1and circuit-2 are first analyzed. The shape of VTC in proposed circuits is comparable to that happens in conventional one. It is also found that reduction in power dissipation as obtained with the leakage current of an NMOS device such as in proposedcircuit-1 is lower than proposed circuit-2.

Fig.6 shows simulation results of voltage transfer characteristic (VTC) for conventional, proposed circuit-1 and circuit-2. The circuits were simulated using NG spice tool.
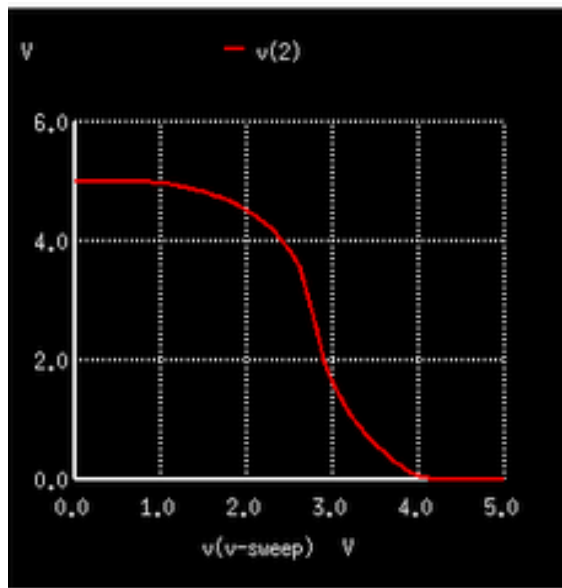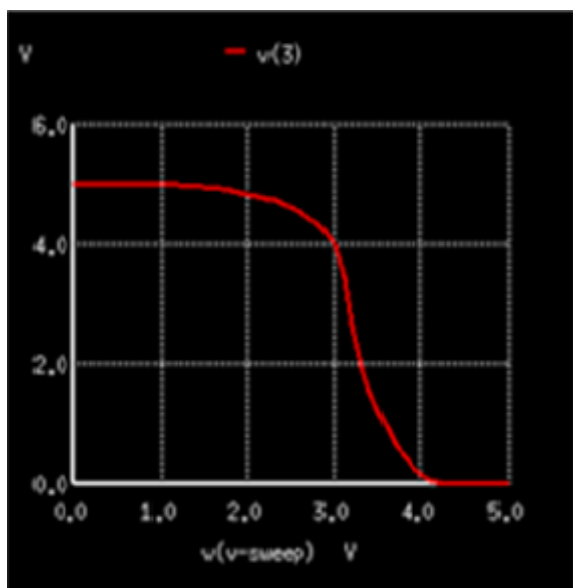


**Figure 6(a):** VTC of Conventional CMOS inverter



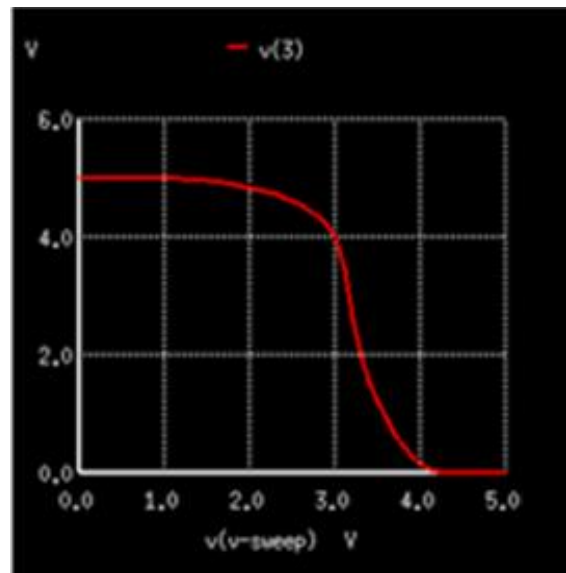**Figure 6(b):** VTC of proposed circuit – 1



**Figure 6(c):** VTC of proposed circuit – 2

The Fig 6 shows simulations of Voltage transfer curve for conventional and proposed CMOS inverter circuits. From those simulation results, it's clear that the voltage transfer curves for all the three circuits are similar. It means that when the proposed technique is used, it does not make much difference to the voltage transfer characteristic of the inverter. It also indicates that there is not much change in noise margin irrespective of a slight increase in noise margin in the case of proposed techniques. The voltage transfer characteristics show that the introduction of extra node and device is a better method since there is not much change.

### 4.2 Substrate Current Simulations

The substrate current of the conventional and proposed inverters is shown in Fig 5 which is used to estimate the power dissipation. Since substrate current is one of the important factor for power dissipation in the dynamic circuits, the simulations of the substrate currents are done and power dissipation is analyzed of the basis of these simulations.
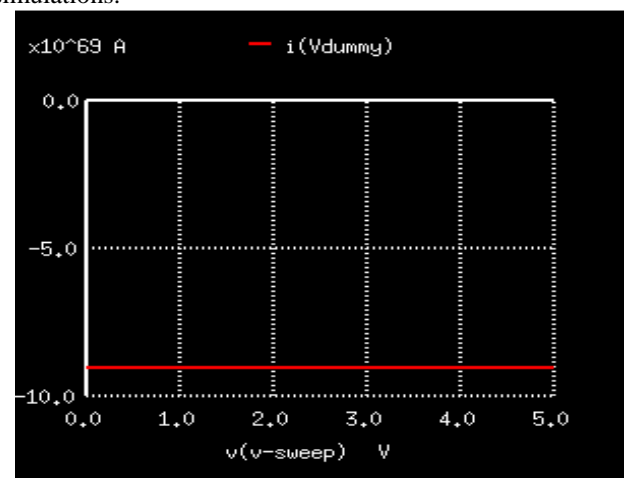


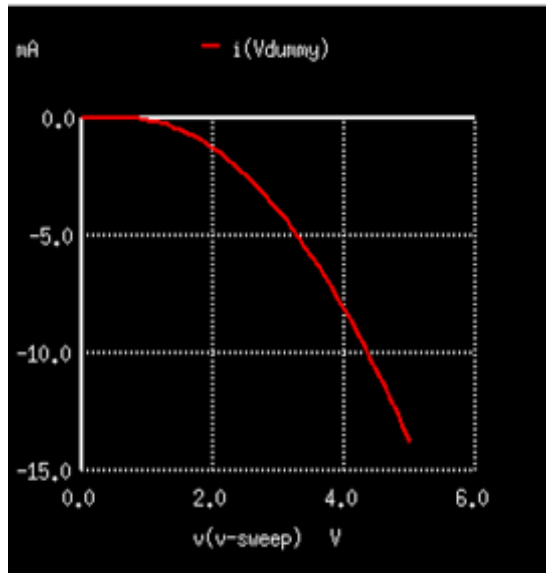**Figure 7(a): Substrate current of Conventional CMOS inverter**

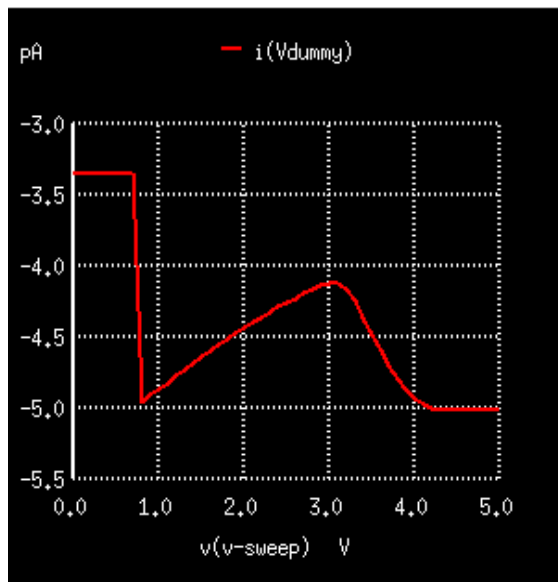**Figure 7(b):** Substrate current of proposed circuit – 1



**Figure 7(c):** Substrate current of proposed circuit – 2

The Fig 7 shows simulations of the Substrate current or leakage current in the case of conventional and proposed inverter circuits. The Fig 7(a) shows the substrate current of conventional inverter which is in the ampere range. The Fig 7(b) shows the substrate current in case of proposed circuit-1 using NMOS where the substrate current is only a few milliampere. This shows that there is significant reduction in substrate current which implies that the proposed technique is capable of reducing the power dissipation. The Fig 7(b) shows the substrate current in case of proposed circuit-2 using PMOS where the substrate current is only a few picoampere. This method reduces the substrate current in picoampere which indicates that the most effective reduction in power dissipation takes place when the PMOS is connected in parallel.

## 5. Conclusion

Addition of nodes to the circuit and leakage current ofsub-100nm device, although result in larger power dissipation but

these can also be integrated in a useful manner in the circuits leading to huge reduction in power dissipation. There is an optimum value of leakage current to be applied at the node, at which power reduction of the circuits becomes maximum. For example, in CMOS inverter, for minimum area, leakage current of single PMOS device results in maximum reduction in power dissipation than leakage current of either an NMOS, or multiple such devices. In addition, with channel length scaling, proposed methodology results in an eligible increase in static power dissipation. All these benefits of the proposed methodology can be attained with much less penalty in speed of operation. In view of the benefits of the proposed methodology as illustrated in this work, it can gain more privileged in low power circuit design for applications especially those operated using power from batteries, and require costly sophisticated cooling mechanism as a means of removing heat from the system.

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