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Design of 7T SRAM Cell Using Self-Controllable Voltage Level Circuit to Achieve Low Power

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Abstract: ***Modern ICs are enormously complicated due to decrease in device size and increase in chip density involving several millions of transistors per chip. The rules for what can and cannot be manufactured leads to a tremendous increase in complexity due to the amount of power dissipation is increased. Power dissipation can be in various forms as dynamic, subthreshold, etc. In this project first, a low power 7T SRAM Cell is designed and later it is build with "Self-controllable Voltage level" circuit for maintaining low power consumption and high performance. A Self-Controllable Voltage Level (SVL) Circuit can supply a maximum dc voltage when the load circuits are in active mode or it can also decrease the dc voltage supplied to a load circuit which is said to be in standby mode. This SVL circuit can reduce standby leakage power of CMOS logic circuits drastically with minimum chip size and speed by considering 7T as load circuit. Furthermore, it can also be applied to memories and registers, because such circuits using SVL technique can retain data even in the standby mode. The entire simulations have been done on 180nm single n-well CMOS bulk technology, in virtuoso platform of cadence tool with the supply voltage 0.7V and frequency of 25MHz.***

Keywords: Low Power, Leakage current, Static Random Access Memory (SRAM), Self Controllable Voltage Level (SVL).

1. Introduction

Low power design has emerged as a principal theme in today's electronics industry. As million of transistor is fabricating on single chip failure rate also increase and degradation of performance takes place so, the major concerns of the designer were area, performance, cost and reliability. In recent years, this has begun to change and increasingly power is being given comparable weight to area and speed considerations [1]. As modern technology is spreading fast, it is very important to design low power, high performance, and fast responding SRAM (Static Random Access Memory) [2]. This is especially true for microprocessors where the on-chip cache sizes are growing with each generation to bridge the increasing divergence in speed of the processors and main memory [3]. Hence the demand for static random-access memory (SRAM) is increasing with large use of SRAM in System-On-Chip and high performance VLSI circuits [4].Due to the increased integration and operating speeds power dissipation has become an important consideration for the need of battery operated devices where the scaling is continued in CMOS technology [5].SRAM cell design depend upon the speed and size of the cell, SRAM cell should be sized as small as possible so large number of transistors can be fabricated on single chip, and we achieve high density in memory design. Typical SRAM cell consists of six MOSFETS. It consists of two invertors connected in back to back followed by the access transistors. Each bit in an SRAM is stored on four transistors that form two cross-coupled inverters. Apart from this the storage cell has two stable states which are used to denote **0** and **1.**Two additional transistors called as access transistors serve to control the access to a storage cell during read and write operations [4].The organization of the paper is as follows: The section 2,3 describes previous work which consists of 6T,7T SRAM cells. Section 4, presents the proposed method of 7T SRAM cell using SVL to reduce leakage current using cadence virtuoso. Section 5 presents simulation result of proposed method. Finally the conclusion is presented in section 6.

2. Conventional 6T SRAM Cell

Operation of SRAM cell can be categorized into three different states: *standby mode* circuit is in ideal mode, *write mode* when mode data has to be updated and *read mode* when data has to be extracted.

In standby mode if the word line is not asserted, the access transistors M5 and M6 disconnect the cell from the bit lines.The two cross coupled inverters formed by M1-M4 will continue to reinforce each other as long as they are connected to the supply.

In write mode, information data is imposed on the bit line and the inverse data on the inverse BLB. Then the access transistors are turned on by setting the word line to high. As the driver of the bit lines is much stronger it can assert the inverter transistors. As soon as the information is stored in the inverters, the access transistors can be turned off and the information in the inverter is preserved [6].Note that the reason this works is that the bit line input-drivers are designed to be much stronger than the relatively weak transistors in the cell itself, so that they can easily override the previous state of the cross-coupled inverters Schematic and waveforms are shown in fig 1 & fig 2 respectively.

In read mode if Q contains 1 the bit lines are first precharged to logical 1 then asserting the word line WL, enables both the access transistors. The second step occurs when the values stored in Q and QB are transferred to the bit lines by leaving BL at its precharged value and discharging BLB through M1 and M5 to a logical 0 .On the BL side, the transistors M4 and M6 pull the bit line toward VDD [6]. The schematic and waveforms are shown respectively in fig3 & fig4 respectively.

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