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Design of 7T SRAM Cell Using Self-Controllable Voltage Level Circuit to Achieve Low Power

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Abstract: ***Modern ICs are enormously complicated due to decrease in device size and increase in chip density involving several millions of transistors per chip. The rules for what can and cannot be manufactured leads to a tremendous increase in complexity due to the amount of power dissipation is increased. Power dissipation can be in various forms as dynamic, subthreshold, etc. In this project first, a low power 7T SRAM Cell is designed and later it is build with "Self-controllable Voltage level" circuit for maintaining low power consumption and high performance. A Self-Controllable Voltage Level (SVL) Circuit can supply a maximum dc voltage when the load circuits are in active mode or it can also decrease the dc voltage supplied to a load circuit which is said to be in standby mode. This SVL circuit can reduce standby leakage power of CMOS logic circuits drastically with minimum chip size and speed by considering 7T as load circuit. Furthermore, it can also be applied to memories and registers, because such circuits using SVL technique can retain data even in the standby mode. The entire simulations have been done on 180nm single n-well CMOS bulk technology, in virtuoso platform of cadence tool with the supply voltage 0.7V and frequency of 25MHz.***

Keywords: Low Power, Leakage current, Static Random Access Memory (SRAM), Self Controllable Voltage Level (SVL).

1. Introduction

Low power design has emerged as a principal theme in today's electronics industry. As million of transistor is fabricating on single chip failure rate also increase and degradation of performance takes place so, the major concerns of the designer were area, performance, cost and reliability. In recent years, this has begun to change and increasingly power is being given comparable weight to area and speed considerations [1]. As modern technology is spreading fast, it is very important to design low power, high performance, and fast responding SRAM (Static Random Access Memory) [2]. This is especially true for microprocessors where the on-chip cache sizes are growing with each generation to bridge the increasing divergence in speed of the processors and main memory [3]. Hence the demand for static random-access memory (SRAM) is increasing with large use of SRAM in System-On-Chip and high performance VLSI circuits [4].Due to the increased integration and operating speeds power dissipation has become an important consideration for the need of battery operated devices where the scaling is continued in CMOS technology [5].SRAM cell design depend upon the speed and size of the cell, SRAM cell should be sized as small as possible so large number of transistors can be fabricated on single chip, and we achieve high density in memory design. Typical SRAM cell consists of six MOSFETS. It consists of two invertors connected in back to back followed by the access transistors. Each bit in an SRAM is stored on four transistors that form two cross-coupled inverters. Apart from this the storage cell has two stable states which are used to denote **0** and **1.**Two additional transistors called as access transistors serve to control the access to a storage cell during read and write operations [4].The organization of the paper is as follows: The section 2,3 describes previous work which consists of 6T,7T SRAM cells. Section 4, presents the proposed method of 7T SRAM cell using SVL to reduce leakage current using cadence virtuoso. Section 5 presents simulation result of proposed method. Finally the conclusion is presented in section 6.

2. Conventional 6T SRAM Cell

Operation of SRAM cell can be categorized into three different states: *standby mode* circuit is in ideal mode, *write mode* when mode data has to be updated and *read mode* when data has to be extracted.

In standby mode if the word line is not asserted, the access transistors M5 and M6 disconnect the cell from the bit lines.The two cross coupled inverters formed by M1-M4 will continue to reinforce each other as long as they are connected to the supply.

In write mode, information data is imposed on the bit line and the inverse data on the inverse BLB. Then the access transistors are turned on by setting the word line to high. As the driver of the bit lines is much stronger it can assert the inverter transistors. As soon as the information is stored in the inverters, the access transistors can be turned off and the information in the inverter is preserved [6].Note that the reason this works is that the bit line input-drivers are designed to be much stronger than the relatively weak transistors in the cell itself, so that they can easily override the previous state of the cross-coupled inverters Schematic and waveforms are shown in fig 1 & fig 2 respectively.

In read mode if Q contains 1 the bit lines are first precharged to logical 1 then asserting the word line WL, enables both the access transistors. The second step occurs when the values stored in Q and QB are transferred to the bit lines by leaving BL at its precharged value and discharging BLB through M1 and M5 to a logical 0 .On the BL side, the transistors M4 and M6 pull the bit line toward VDD [6]. The schematic and waveforms are shown respectively in fig3 & fig4 respectively.

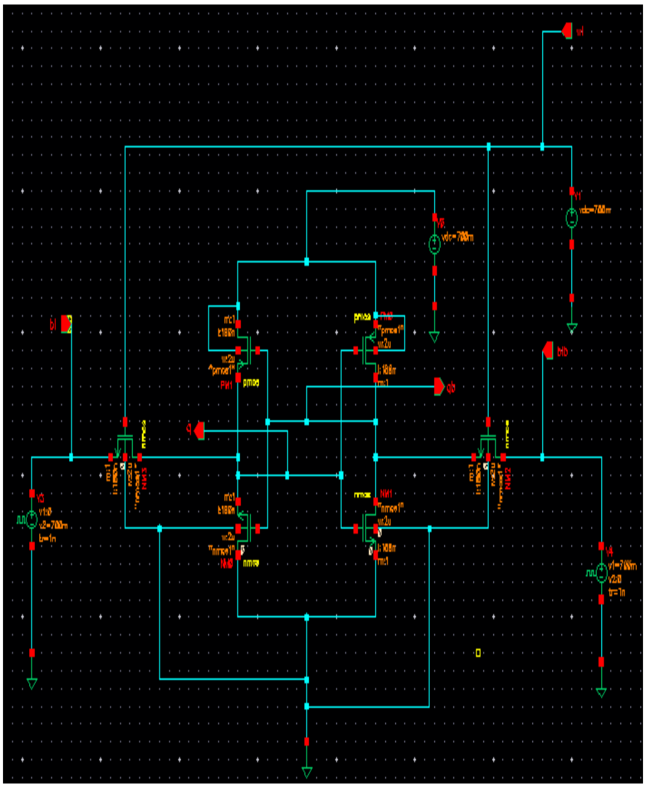

Figure 1: Schematic of 6T SRAM Cell during write mode

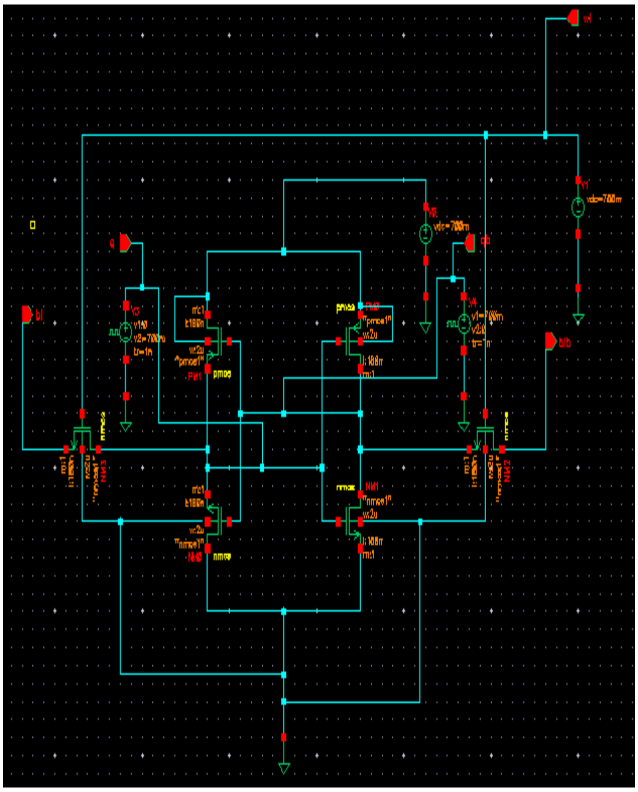

Figure 3: Schematic of 6T SRAM Cell during read mode

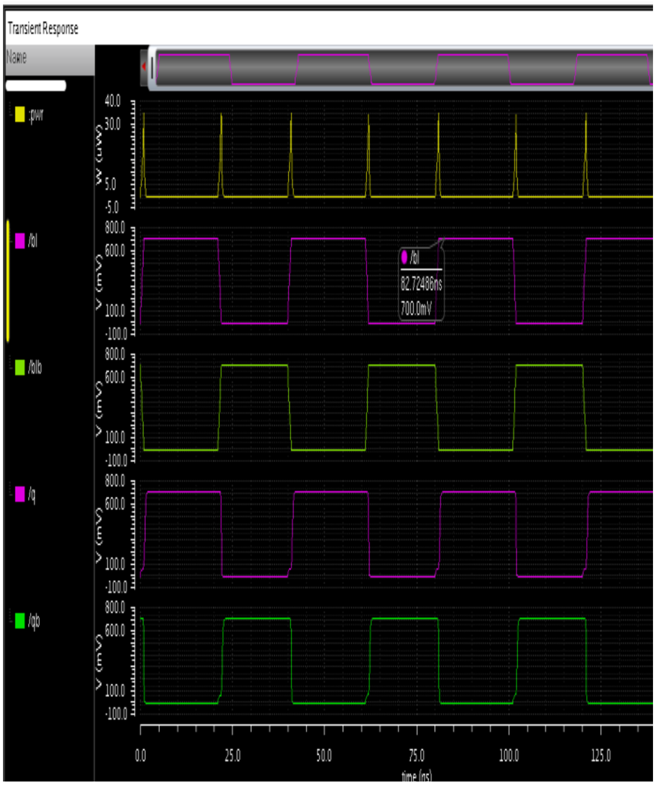

Figure 2: Waveform of 6T SRAM Cell during write mode

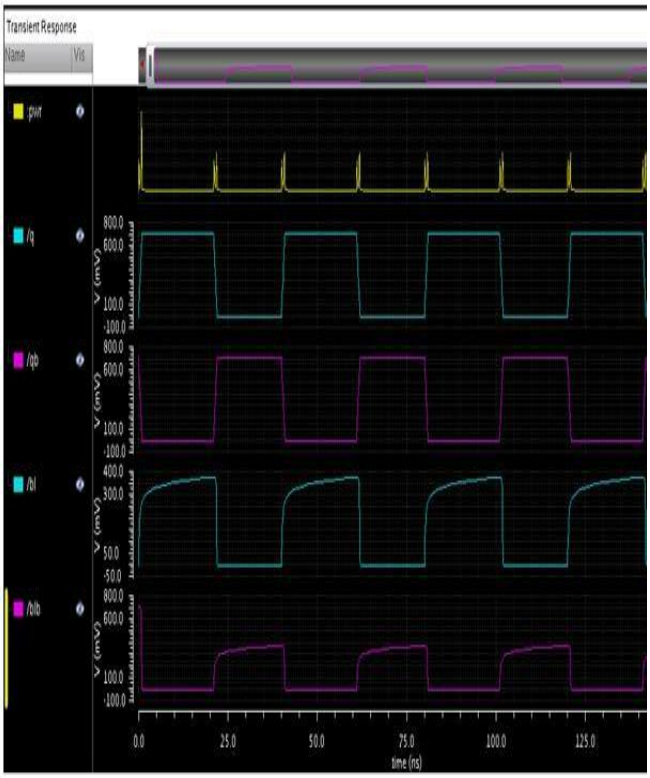

Figure 4: Waveform of 6T SRAM Cell during read mode

The disadvantage of 6T SRAM cell is it consumes more power when compare to 7T SRAM cell and it has poor static noise margin (The static noise margin is the maximum amount of noise voltage that can be introduced at the output of the two inverters, such that the cell retains its data. Static noise margin quantifies the amount of noise voltage required at the internal nodes of a bit-cell to flip the cell's content.

3. Design of 7T SRAM Cell

The 7T SRAM cell consists of a 6T SRAM cell and an additional NMOS transistor Cell. This additional transistor is placed in the ground path in order to reduce the leakage while the cell is in standby mode [9]. For writing 1 to the storage node output Q , BLB and BL should be charged and discharged and word line across the

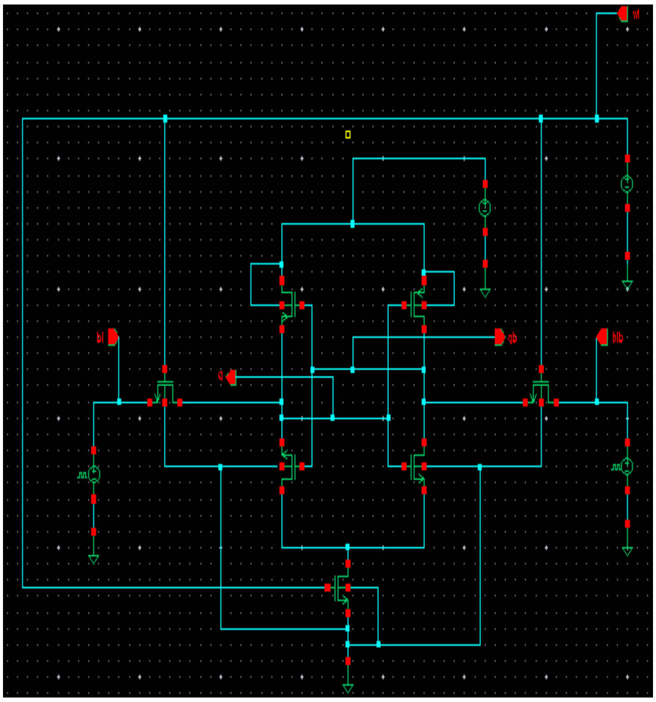

Figure 5: Schematic of 7T STAM Cell during write mode

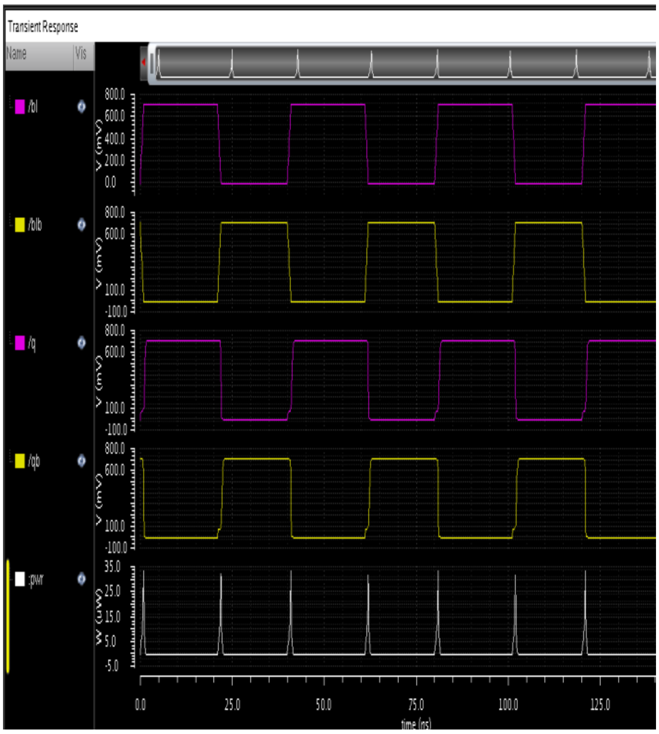

Figure 6: Waveform of 7T SRAM Cell during write mode

additional transistor should be discharged. Then one PMOS transistor will be on giving 1 at QB and through the NMOS transistor Q will be charged to 0 [10] [11]. Similarly for the case of Q to be 1 and QB to be 0.The schematic and waveforms are shown in fig 5 & fig 6 respectively.

For reading if Q is at 1 and QB is at 0 then keep WL to be high and then through BL and BLB we will get the outputs in the complementary form. The storage nodes Q and QB completely decouple datum from the BL during read operation [10] [11]. The schematic and waveforms are shown in fig 7& fig 8 respectively.

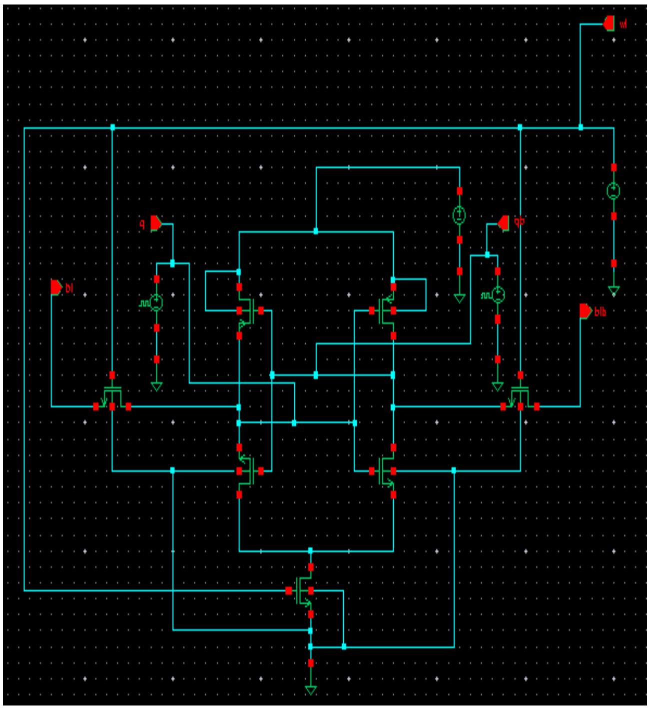

Figure 7: Schematic of 7T SRAM Cell during read mode

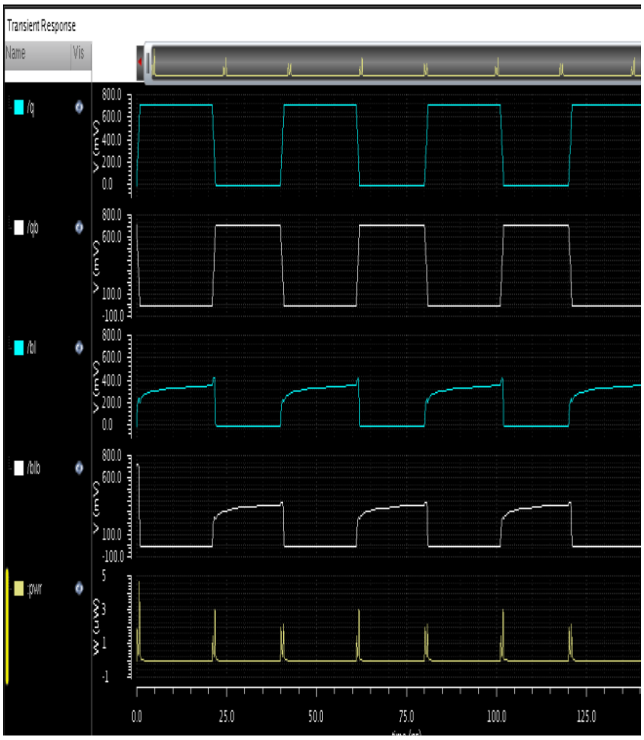

Figure 8: Waveform of 7T SRAM Cell during read mode

The read operation of both 6T and 7T SRAM cell is similar and in order to reduce the leakage current in 7T SRAM a new method is proposed 7T SRAM using SVL which drastically reduces the amount of leakage current.

4. Self Controllable Voltage Level Circuit

For the portable systems which are driven by battery there are many power reduction techniques such as multi threshold voltage CMOS (MTCMOS) and variable threshold CMOS (VTCMOS). In the first technique power has been reduced. Effectively by use of high *Vt* MOSFET switches which disconnects the power supply. If this is applied with memories and flip- flops it has a drawback of not retaining data. In the other technique variable thresh old-voltage CMOS (VTCMOS) is used that reduces Power by increasing the substrate-biases. The drawbacks for this technique is large area problem as well as power dissipation. So a self-controllable voltage level (SVL) technique is proposed where the load circuits in active mode allows full supply voltage and decreased supply voltage appears to be proficient for reducing gate leakage currents as well [13].When the load circuits are in standby mode, it supplies slightly lower voltage and relatively higher voltage to them through "ON" switch, so the drain-source voltages of the "OFF MOSFETs" decreases Vsub. So Vth increases consequently when sub threshold current decreases. Three types of self-controllable voltage level (SVL) circuits are there. Type 1 stands for upper SVL circuit, Type 2 stands for lower SVL circuit, and Type 3 stands for both combined. This technique is well suited for circuit in standby mode as leakage power is reduced more as compared to other techniques [12][13].

In upper SVL a single NMOS and PMOS are connected in series in which "ON" PMOS transistor connects VDD to load circuit in active mode and "ON" NMOS transistor connects VDD to load circuit in standby mode as shown in fig 9. If gate voltage (VG) of the inverter is kept at "0", the PMOS is turned on while the NMOS is turned off. In standby mode due to connection between gate to the VDD. NMOS will be turned on and PMOS switch will be turned off. Thus VDD is supplied to the inverter using NMOS. So there will be a flow of drain voltage across the NMOS transistor giving an expression as

Vdsn= VDD-mv ---equ (1)

Where v is the voltage drop across NMOS transistor and according to the equation Vdsn depends on m and v which means if we want are increasing m or v drain voltage will be decreased which in turn will increase the barrier height. So according to the second order effect threshold voltage will increase which will decrease the sub threshold current of NMOS and leakage current through inverter.

The lower SVL circuit, a single NMOS and PMOS are connected in series, and located between a ground-level power supplies (VSS) and the load circuit. In lower SVL "ON" NMOS transistor connects VSS to load circuit in active mode and "ON" PMOS transistor connects VSS to load circuit in standby mode as shown in fig10.

In this case of lower SVL circuit, gate voltage for PMOS will turn it on and for applied in NMOS will turn it off so that VSS is supplied to the stand-by inverter with VG of "0" through PMOS. Thus, according to the previous equation, reduction in drain voltage reduces the subthreshold current.

Vsub= -mv ---equ (2)

Now due to two effects drain induced lowering and back gate bias there will be further decrease in leakage current thereby reducing power.

In type3 both upper and lower SVL is combined which in turn reduces leakage current. Moreover source voltage(Vs) is increased by mv, so the substrate bias (i.e., back - gate bias) (Vsub) increase which is expressed by

Vdsn= VDD-2mv ---equ (3)

This in turn increases the threshold voltage and thus decreases the leakage current. The schematic and waveform of 7T SRAM Cell using proposed SVL technique for write and read operations are shown in simulation results.

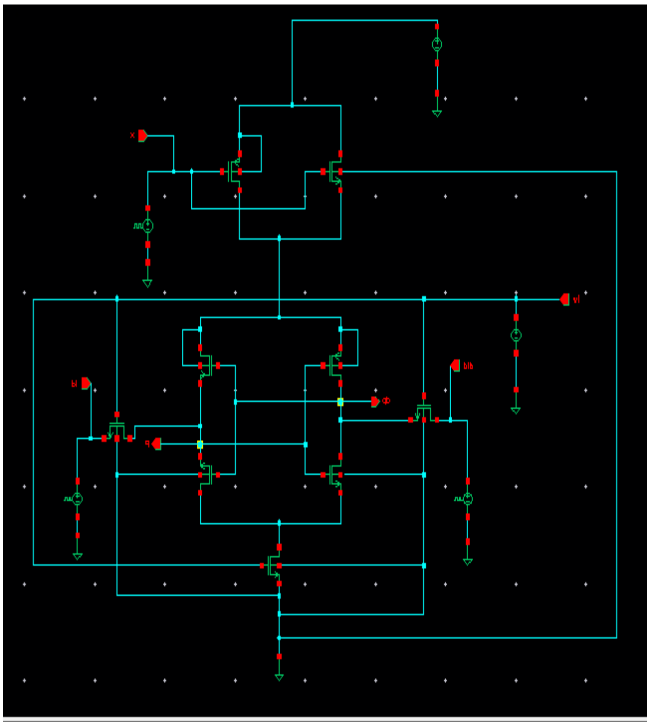

Figure 9: Schematic of 7T SRAM using USVL

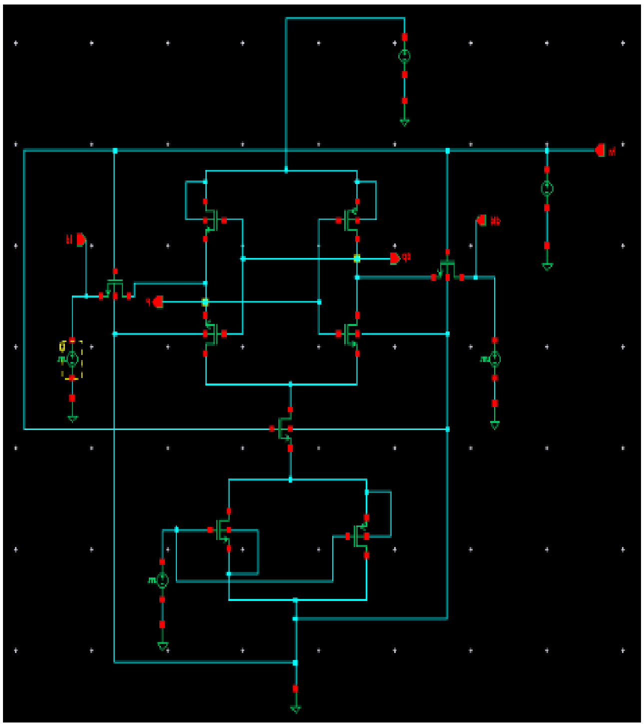

Figure 10: Schematic of 7TSRAM using LSVL

5. Simulation Results

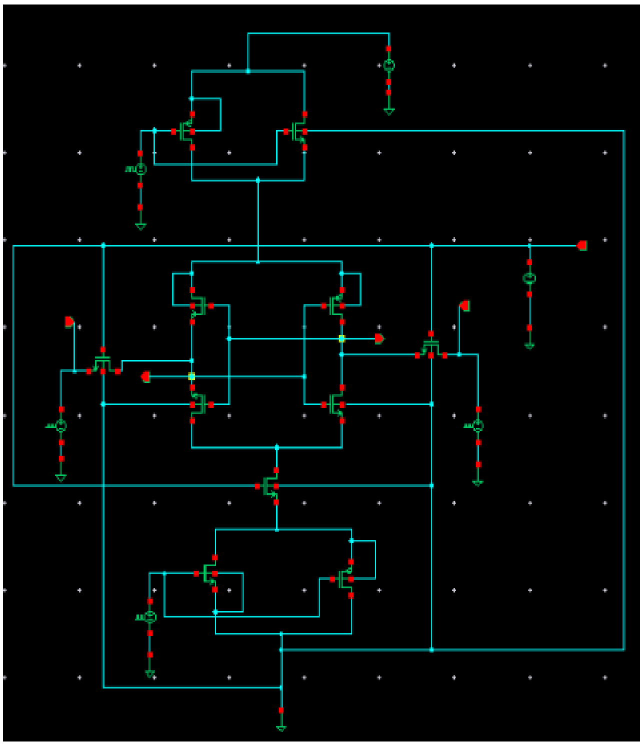

Figure 11: Schematic of 7T SRAM Cell using SVL during write mode

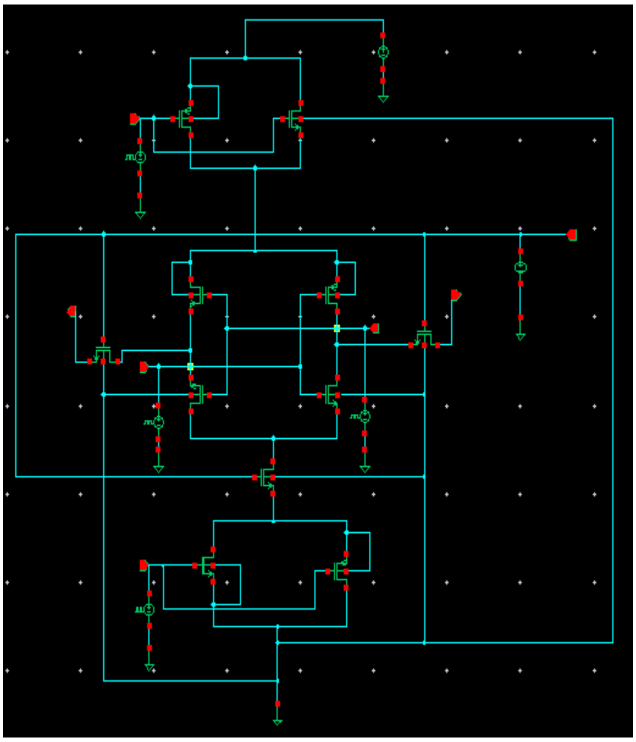

Figure 13: Schematic of 7T SRAM Cell using SVL during read mode

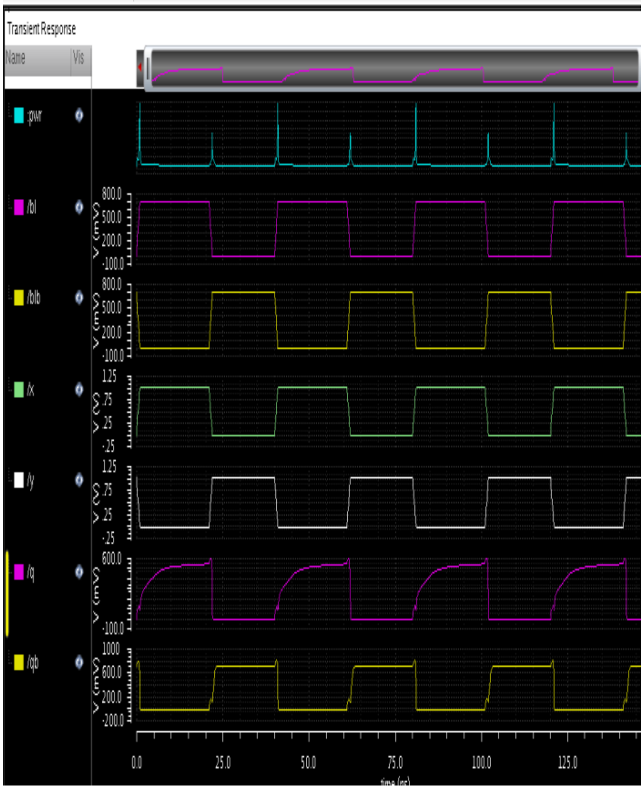

Figure 12: Waveform of 7T SRAM Cell using SVL during write mode

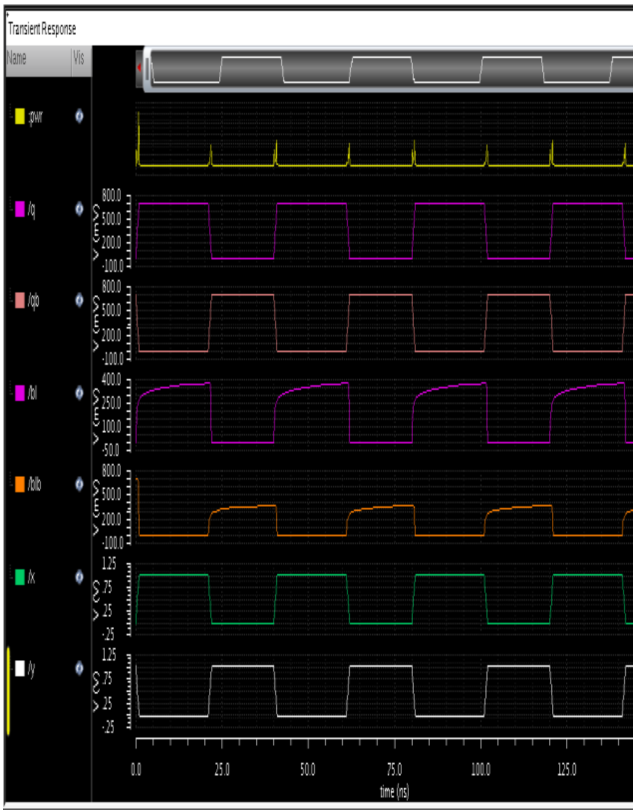

Figure 14: Waveform of 7T SRAM Cell using SVL during read mode

Table 1: Average Power and Current Analysis of SRAM Cells

Cell	Modes of operation	Power	Current
6T SRAM Cell	Write	0.948uW	0.534uA
	Read	0.068uW	0.108uA
7T SRAM Cell	Write	0.771uW	0.514uA
	Read	0.063uW	0.107uA
7T SRAM Cell using SVL	Write	0.435uW	0.311uA
	Read	0.049uW	0.0375uA

6. Conclusion

In this paper we have simulated and analyzed the performance of 6T,7T and 7T using SVL circuit SRAM cells at 180 nm technology using cadence tool[6]. This paper describes the comparison between conventional 6T and 7T SRAM cell and simulation results prove the better stability of 7TSRAM cell with respect to average power [15] and Signal to Noise Margin. Moreover after applying Upper Self Controllable Voltage Level technique nearly 10% power reductions, Lower Self Controllable Voltage Level around 23.4% power reduction and using both SVL techniques around 35%. Power reduction has been found in terms of leakage current. This technique can further be used with registers and other flip flops and arrays for low power in terms of leakage current [13].

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