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Performance Enhancement of Voltage-Source-Converter Using Vector Control Under Load Disturbance

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Abstract: ***Voltage-source converter (VSC)-based transmission systems have attractive potential features in terms of power flow control and stability of the network.The increasing emergence of VSC-based transmission is the result of development in semiconductor devices, power electronic circuits, control, and executive engineering, The most important limiting factor of power semiconductors is their switching properties since they are usually optimized for the conduction intervals. This concept specifically proposes a control structure to improve the performance of high-power vector-controlled back-to-back VSC systems . The main improvement is to suppress the possible dc-link voltage fluctuations under power line faults and unbalanced conditions. The proposed controller structure is designed based on regulating the converter system's states locally in d-q synchronous reference frame without sequence components extraction or resonant notch compensator. The mat lab results verify the validity of the proposed control architecture during normal and unbalanced power system conditions.***

Keywords: High-voltage direct current (HVDC), Lyapunov, methods, power systems faults, pulsewidth modulation (PWM), voltage source converter(VSC).

1. Introduction

It is desirable to have high-power high voltage converter based systems available during power system faults when they may be needed the most. If the protection measures trip the converter system, it can take several fractions of an hour, depending on the size of the converter, to discharge the dc link and check the healthiness of the whole system. Hence, several practical methods have been proposed and implemented to keep a system operating under power system faults and disturbances [1], [2]. Today, the most promising market for HVDC technology is interconnection of the networks where the centers of the loads are located far from the points of connection. The problem of ac systems arises as the phase angle drifts and varies over a wide range with daily load changes [3]. This phenomenon especially in a weak ac network along with the power line faults exacerbates the operation of HVDC systems.

A voltage-source converter (VSC) is the main building block for flexible ac transmission systems (FACTS) devices and, as of today HVDC technology up to several hundred megawatts.The increasing emergence of VSC-based transmission is the result of development in semiconductor devices, power electronic circuits, control, and executive engineering, [4]–[6]. Previously, the lack of these developments had prohibited the VSC-based technology from being the first choice. While each development is moving forward individually, the result of each one influences the design criteria and application requirements of the overall system.

However, generally, less dependence on power semiconductor characteristics amounts to having more supplier possibilities for the VSC-based transmission. The most important limiting factor of power semiconductors is their switching properties since they are usually optimized for the conduction intervals. Hence, high-power electronic converters are desired to operate with relatively lowswitching frequencies (maximum 9–15 times the line frequency, and even lower for multilevel converters). The low switching frequency operation of VSC systems imposes control limitations in case of power system faults and disturbances when they may be needed the most. To the best of the authors' knowledge, in the installed operating FACTS and HVDC systems, the ride-through capability is obtained either by proper passive element design [7], [8] or a change in the control mode [1]. On the other hand, with emerging high-power applications such as 10-MW wind generation turbines [9] or transportable recovery transformers [10], the dynamic operation of the VSC under power system disturbances must be revisited. This paper proposes an alternative control framework to obtain robust dc-link voltage with specific attention to design the VSC controller in the back-to-back (BTB) configuration, as shown in Fig. 1. The proposed controller is implemented in the *dq* (rotating) synchronous reference frame without sequence extraction.

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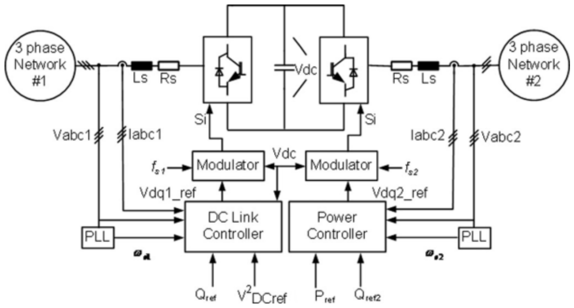


Figure 1: Simplified schematic of closed-loop BTB VSC systems.

reviews research and advances to control the VSC under unbalanced conditions. This section also provides the backgrounds and advantages of the proposed methods and their applicability for high-power high-voltage VSCs. Section III describes the modeling approach for the VSC. In this section, general closedloop functions and control constraints of the BTB VSC systems will be discussed briefly. In Section IV, the proposed control architecture and its implementation will be presented. RTDS verification of the proposed control method be presented in Section V. Finally, Section VI presents the conclusion of the research.

2. Backgrounds On Controlling the VSC Under Unbalanced Conditions

A. Single VSC Control Under Unbalanced Conditions

The VSC is the main building block for FACTS devices and many other converter-based utility interfaces. Therefore, the study on the methods to improve the converter performance as a single system under network unbalanced conditions is unavoidable. The theory of instantaneous active and reactive powers for three-phase switching converter control was proposed by Akagi*et al.* [11]. It has been shown that the power quality in terms of current harmonics and reactive power can be improved using the instantaneous reactive power definition. The work in [12]and [13] showed that network voltage unbalances cause input current distortions which can be transferred to the dc side due to the negative-sequence component of the voltage.

Rioual *et al.* [14] probably proposed the very first control scheme for the VSC that regulate the instantaneous power generated under network voltage dips. Their work mainly generated current references in both positive and negative synchronous references to regulate the power at the point of common coupling (PCC). Since then, researchers have been developing “enhanced” control schemes mostly to minimize input harmonics which are coupled to dc-link voltage ripples. For instance, Stankovic and Lipo [15] presented a model that can eliminate the harmonics for generalized unbalanced conditions. However, this method needs a great deal of computation steps for DSP-based control. In [16] and [17], the authors consider the instantaneous power at the converter poles, not the PCC, and consequently obtain better harmonic responses. Although these methods are more effective than the work in [14] and relatively simpler than that in [15], the proposed methods suffer from solving nonlinear equations in real time and low bandwidth of the current regulator due to the extraction of the current sequence components. Suh and Lipo continued their work [18], which resulted in a hybrid synchronous stationary frame with oscillating reference currents. Consequently, the bandwidth-diminishing functions are avoided. They also proposed a simplified current reference generator that can be implemented more easily than that in [16] and [17]. It might be of reader’s interest that in [16]–[18], the instantaneous reactive power definition is different from the“classical” notion of outer products of vectors presented in [11].Instead, these authors mainly employed the work in [19] in which the authors developed the so-called extension PQ theory to resolve the singularity issues existing in the work of Akagi *et al.* [11] for the generalized unbalanced condition. Accordingly,the instantaneous reactive power is redefined on the basis of a set of voltages that lag the pole voltages by 90◦ and is not the imaginary part of the complex power. Despite satisfactory operation of a three-phase rectifier under unbalanced conditions,the proposed scheme in [18] requires several feedback and feedforward compensators. A simplified controller is proposed in [20] which uses stationary current controller (resonant compensator) that considers both positive and negative sequences simultaneously. Notch filters tuned at 120◦ [21] are nonetheless used to extract the bus voltage sequences for current reference generation. In [22], the authors also consider notch filters but to separate the positive- and negative-sequence current controllers. One potential constraint of these methods is the emergence of third harmonic in the input current that is proportional with the voltage dip, and in [23], the authors analyzed the effects of several methods to estimate the proper sequence components. Most recent work is reported in [24] which implemented the whole control frame in the stationary frame resulting in a new current reference generator. Fast dynamic performance with small dc-link voltage ripple in a 20-kVA/10-kHz pulsewidth modulation (PWM) prototype converter under a 30% supply voltage dip is reported. A desirable feature of the scheme is that no phase-locked loop (PLL) strategies are needed but constant line frequency is assumed and sinusoidal compensators as in [18] are deployed due to the control logic of the oscillating references.

B. BTB VSC Control Under Unbalanced Conditions

The transmission-level multi-VSC option requires a careful consideration of system interactions, while switching frequency is kept relatively low (9–15 times the line frequency). An example of this theme is investigated for a unified power flow controller (UPFC) in [25] where additional compensating terms are added to reduce or remove the interactions of rectifier and potential issues of BTB VSC system operation with conventional controllers applied to single VSCs [26]. This fact is more critical under power system faults since the controllers introduced previously should take these interactions into account. Therefore, simply separating sequence controllers may not achieve the desired performance due to the system coupling, filtering delays, etc. To solve these problems, Xu *et al.* [26] introduced a framework which mainly used the results of [14] and [27]. Xu *et al.* [26] proposed to nullify the oscillating power as in [14] by generating a current reference. In addition, Xu *et al.* [26] considered the improved “cross-coupling control” mentioned for UPFC in [27]. This control scheme was first proposed for UPFC applications in [28] where authors showed that the crossing gain of a transmission line is much larger than its direct gain. The cross-coupling controller uses the *q*-axis voltage vector, to control the *d*-axis current and the *d*-axis voltage vector to control the *q*-axis current. Numerical results in [26] illustrate the satisfactory performance under a single-line-to-ground fault but with more than double the rated current. The latter result is important in VSC HVDC transient dynamics. It has been pointed out in [29] that increase of the current limit significantly improves the power quality of the system. Yazdani and Iravani mention in [30] that it is possible to suppress the dc-link voltage oscillations by using the notch filter approach; therefore, the same issues exist as for a single VSC. For a specific VSC BTB HVDC system, Hagiwara and Akagi [31] proposed a unique dclink control structure that has the load feedforward term. With the proposed structure, a robust dc-link voltage is achieved if the fault occurs in the inverter side. It has been shown that load estimation can improve the converter performance. In fact,Winkelnkemper [32] had shown that adding the load estimation into the main controller better attunes the dc-link voltage to load power change. Parkhideh *et al.* [33] also showed how it is possible to remove the varying load effect from the closed-loop large mining converter control systems (1.5–24 MW) which are basically BTB VSC systems.

On the other hand, there are emerging interests to have medium voltage interfaces for renewable integration such as wind generations currently up to 10MVAwith direct-drive technologies (BTB VSC) [9]. In [34], the authors have presented a unique controller in the stationary frame for direct-drive wind generation systems that is based on reactive power compensation. Applying the proposed method ensures balanced grid currents even under power system faults. Nonetheless, due to possible low-speed operation of wind turbines, dc-link dynamics have been addressed as one of the key factors which affect the operation of the turbine [35]. Therefore, more investigations are essential to determine the proper control strategy: balanced currents or a stiff dc-link voltage.

This paper proposes a control structure specifically for the dc-link controller converter in the BTB VSC system which is implemented in a single synchronous reference frame without any sequence component extraction or resonant compensator. It will be shown that dc-link dynamics are coupled to the interaction imposed by the inverter performance. On the other hand, there is no direct control input that can remove this interaction or disturbance with conventional frequency-oriented controller design. This study introduces a *dq* (rotating) synchronous-based framework to design a more robust controller for relatively low switching frequency (9–15 times) PWM or vector-controlled BTB VSC systems.

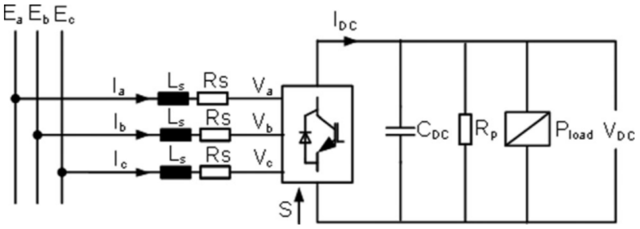


Figure 2: Schematic of a VSC

3. Modeling And Control Of VSC

A. Modeling of VSC

The modeling of VSC, the building block of the BTB system, is based on the state-space average modeling approach [36]. This modeling is based on the principal circuit analysis and voltage and current equations for storage elements known as state equations. The general schematic of a three-phase VSC circuit is shown in Fig. 2, and the state equations of a VSC in the three-phase stationary coordinates are as follows:

$$\frac{dI_{abc}}{dt} = -\frac{R_s}{L_s} I_{abc} + \frac{E_{abc}}{L_s} - \frac{V_{abc}}{L_s} \qquad (1)$$

$$\frac{dV_{DC}}{dt} = \frac{I_{DC}}{C_{DC}} - \frac{V_{DC}}{R_p C_{DC}} - \frac{P_{load}}{C_{DC} V_{DC}} \qquad (2)$$

In order to benefit from all decoupling and constant properties of a two-phase system instead of a three-phase one, *dq* transformation is considered to convert all quantities in the *abc* stationary coordinate frame to the synchronously rotating reference frame, i.e., d_e–q_e

$$\frac{dI_d}{dt} = -\frac{R_s}{L_s} I_d - \omega_s I_q + \frac{E_d}{L_s} - \frac{V_d}{L_s} \qquad (3)$$

$$\frac{dI_q}{dt} = -\frac{R_s}{L_s} I_q + \omega_s I_d + \frac{E_q}{L_s} - \frac{V_q}{L_s} \qquad (4)$$

In (3) and (4), V_d and V_q are the converter output voltages in the synchronous reference frame. The modulation index can also be written in this frame as (5) where k depends on the modulation technique. In this study, we use the vector control method or type-I control denoted by Schauder and Mehta [7]

$$m_d = \frac{V_d}{kV_{DC}} \quad , \quad m_q = \frac{V_q}{kV_{DC}} \qquad (5)$$

In many literature works especially for dc/dc converters, the modulation index is used as the control input; therefore, (3) and (4) present the nonlinear system. DC-link dynamics are also nonlinear by introducing the definition for I_{DC} as (6). However, by considering V_d and V_q as the control inputs, (3) and (4) can be treated as linear ones. Also, power balance is used to derive the equation for the dc-link voltage neglecting the interface losses as in (7) [22], [37], [38]. E_a (the PCC phaseAvoltage) is aligned with the *d*-axis in the synchronously rotating reference frame. The result of dc-link dynamics shown in (7) is linear as long as E_d and E_q are constant. Consequently, no linearization around specific operating points is needed and the small-signal VSC model looks similar to the large-signal model. The state-space representation of the VSC can be obtained from (3), (4), and (7). State variable vector $x(t)$ is the state variable vector, $u(t)$ is the input vector, and $e(t)$ is considered as the disturbance vector, (8):

$$I_{DC} = \frac{3}{2}\left(m_d I_d + m_q I_q\right) \qquad (6)$$

$$\frac{dV^2{}_{DC}}{dt} = \frac{3E_q I_d}{C_{DC}} + \frac{3E_q I_q}{C_{DC}} - \frac{2V^2{}_{DC}}{R_p C_{DC}} - \frac{2P_{load}}{C_{DC}} \qquad (7)$$

$$x(t) = \begin{pmatrix} I_d \\ I_q \\ V^2{}_{DC} \end{pmatrix},$$

$$u(t) = \begin{pmatrix} V_d \\ V_q \end{pmatrix}, e(t) = \begin{pmatrix} E_d \\ E_q \\ P_{load} \end{pmatrix} \qquad (8)$$

Although there is a possibility of using the so-called instantaneous PLL presented in [39] to discard the effect of the *q*-component of the voltage vector even under unbalanced conditions (at least in the model), this study considers common PLL structures in order to unify the problem.

B. Closed Loop of BTB VSC Systems

In the vector-controlled BTB VSC systems regardless of the topology, one converter typically controls the dc-link voltage and supports its reactive power. This converter can be operated as rectifier in HVDC applications or as an inverter in directdriven wind turbines. The other converter is operated in *PQ* or *V*/*f* (voltage/frequency) mode controlling the active and reactive powers. A simplified schematic of the BTB VSC system with its control functions is depicted in Fig. 1.

To design a closed-loop system, the eigenstructure assignment or any linear feedback design method can be used to place the poles at the desired locations. Eigenstructure assignment is explained for STATCOM in [40] and we use it to develop the general controller and as the baseline for the VSC in the BTB configuration as presented in [38].

According to the system equations, the mode associated with the *q*-component of the current (typically for reactive power control) can be adjusted based on the ac-side interface parameters and required response time. On the other hand, dc-link voltage closed-loop dynamics consist of the modes associated with two eigen values. One of the system poles affects the charging and discharging of the capacitor which is called λ_c. This eigen value should be placed near to the origin to avoid either high charging or discharging current. The other pole can be placed at the same location the reactive current control mode is, which we call it λ_i. It should be noted that the poles associated with the current mode can be placed as far as the inherent delay of the converter modeling allows; current regulators often present a fast firstorder behavior. To achieve a nonoscillatory output response, itis sufficient to place the poles at the real axis. Consequently,the dc-link voltage regulator can be designed based on the system specifications and requirements. The performance of the BTB system under balanced conditions through the proposed modeling and control has already been presented in [38].

Table 1: VSC BTB System Parameters

Base Power	S	10 MVA
Line-to-line voltage (converter side)	E	1 pu = 13.8 kV
Line-to-line voltage for drive app.	E_w	1 pu = 3.3 kV
Line frequency (grid)	f	60 Hz
Leakage inductance	L_s	15% pu
Interface resistance	R_s	0.4% pu
DC link voltage	V_{DC}	1 pu = 1.65 V_{AC}
DC link capacitance	C_{DC}	0.66 pu
Unit capacitance constant	H	4.16 ms
Switching frequency	f_s	900 Hz (15xf)
Converter loss resistor (estimated)	R_p	1% pu
Continuous overcurrent capability	I	1.5 pu
Absolute overcurrent capability	I_{max}	2 pu
Current controller pole location	λ_i	-1000
Voltage controller pole location	λ_c	-250
Communication delay	T_d	10 ms
Time delay of the derivatives	T_{iF}	0.1 ms
Controller sampling time	t_s	50 us

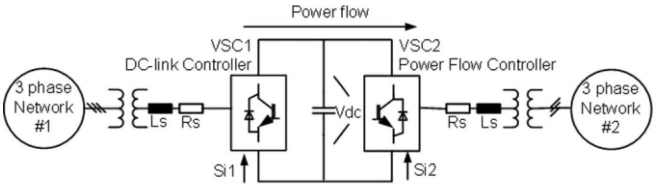


Figure 3: BTB VSC system for HVDC applications.

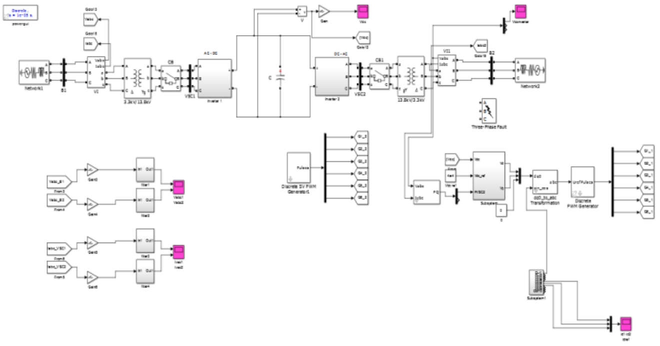
4. Dynamic Performance of BTB VSC Systems with the Proposed Control Architecture

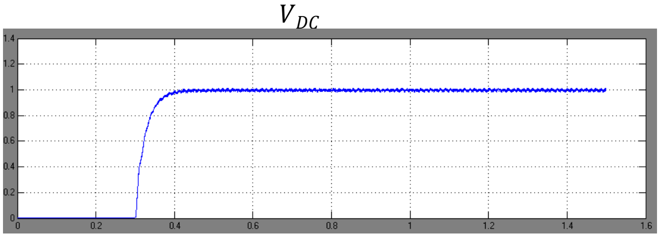
This section presents and evaluates the dynamic performance of BTB VSC systems in different applications. Applications are categorized as HVDC, drive (wind), and hybrid power system applications. The proposed controller has been implemented in RTDS and compiled on a GPC processor card with a controller sampling time of 50 μs and key circuit parameters as tabulated in Table I. For reference, the performance comparison of the BTB VSC system (based on the average model) with the proposed control scheme and commonly used controller structures has been presented in the Appendix. In order to analyze the performance of the system, the following assumptions have been made.

1) The system references are controlled based on the currents for the case studies under faults.
2) There is no change in control mode of the system pre-during, and post-fault. Under unbalanced grid voltages, reactive power demand can dominate the available converter capacity. This demand imposes some limitations in regulating the dc-link voltage.
3) Power systems have same short-circuit capacity.

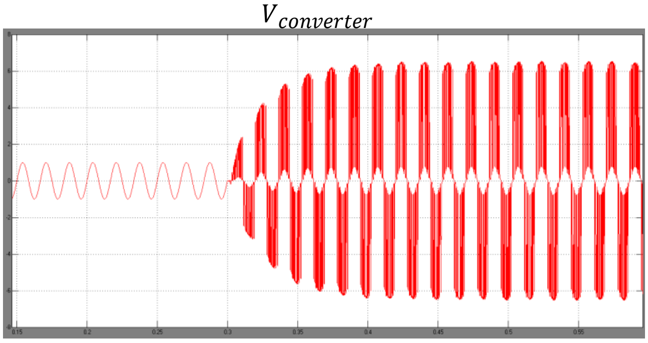
5. Simulation Results

Simulation Result of BTB VSC system for HVDC application without fault.

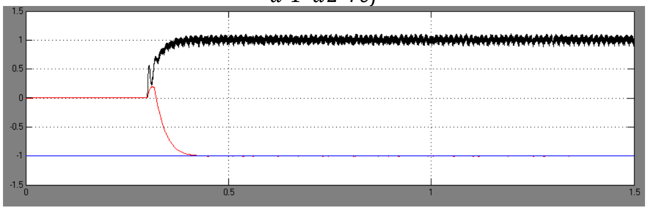




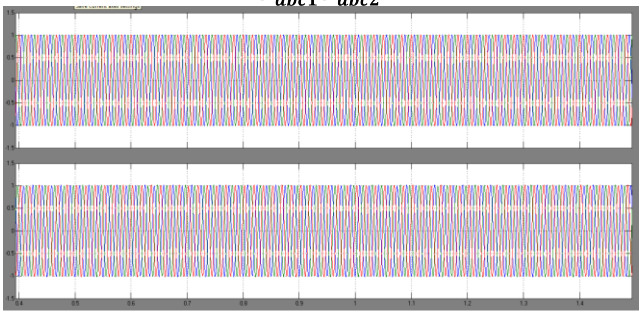
V_{DC}



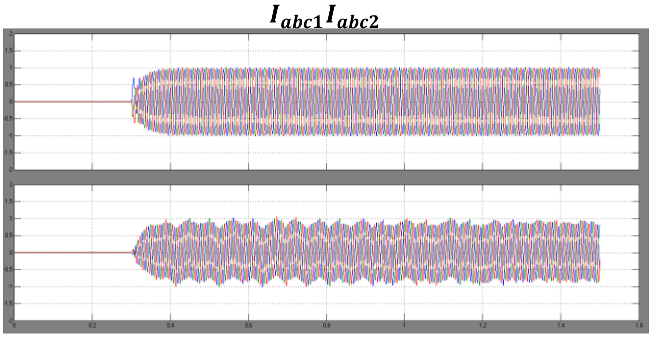
$V_{converter}$



$I_{d\ 1}I_{d2}I_{ref}$

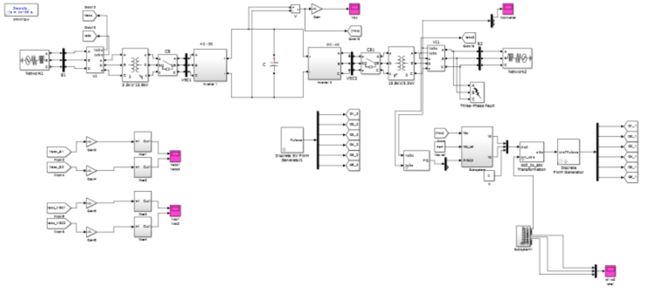


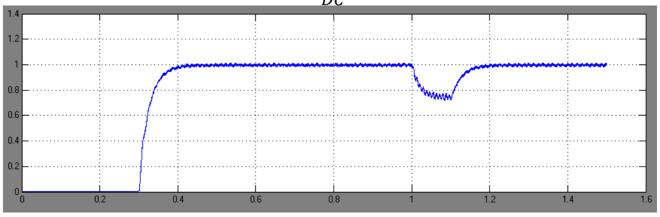
$V_{abc1}V_{abc2}$



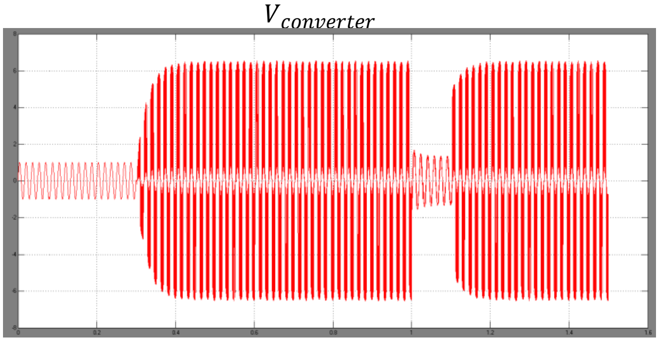
$I_{abc1}I_{abc2}$

Simulation Result of BTB VSC system for HVDC application with fault

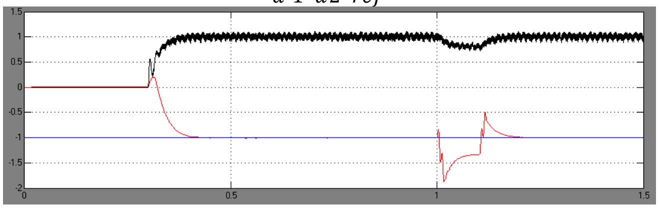




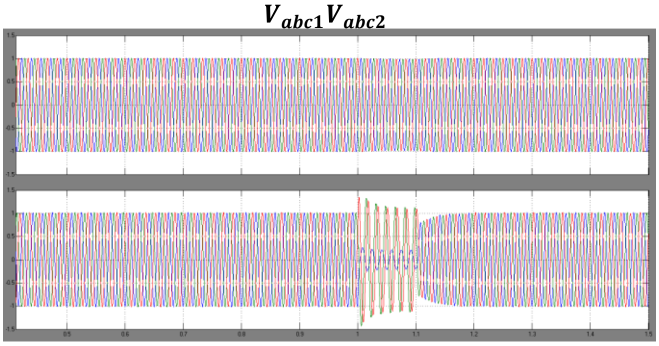
V_{DC}



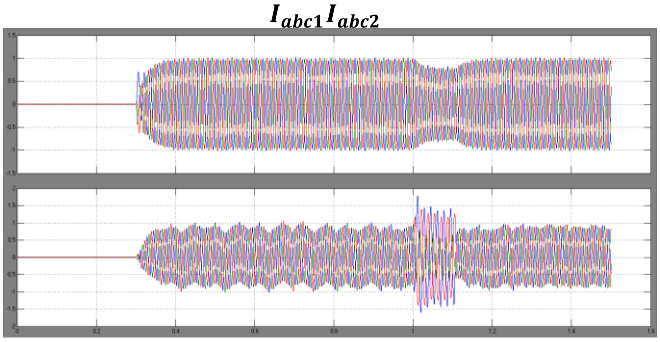
$V_{converter}$



$I_{d\ 1}I_{d2}I_{ref}$



$V_{abc1}V_{abc2}$



$I_{abc1}I_{abc2}$

FFT Analysis of BTB VSC system for HVDC application of Iabc1 Before Fault ,Fault at the Moment,After Fault

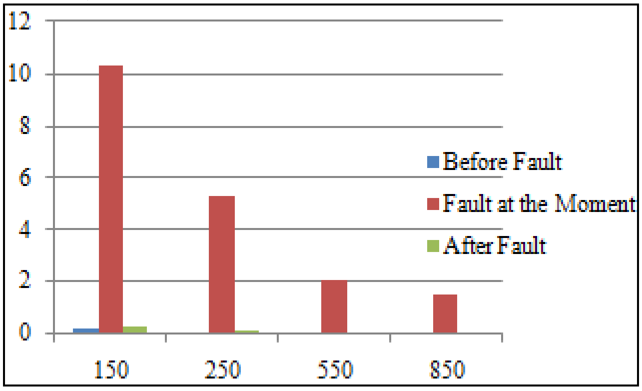


Figure: BarChart of Ia1 before ,at the moment &after fault

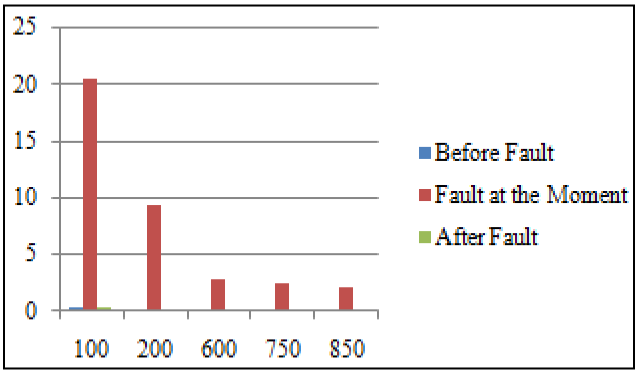


Figure: BarChart of Ib1 Before Fault,Fault at the Moment & After Fault

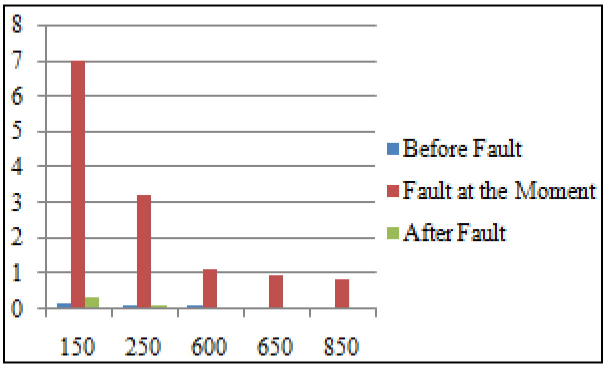


Figure: BarChart of Ic1 Before Fault,Fault at the Moment & After Fault

FFT Analysis of BTB VSC system for HVDC application for Iabc2 Before Fault, Fault at the Moment,After Fault

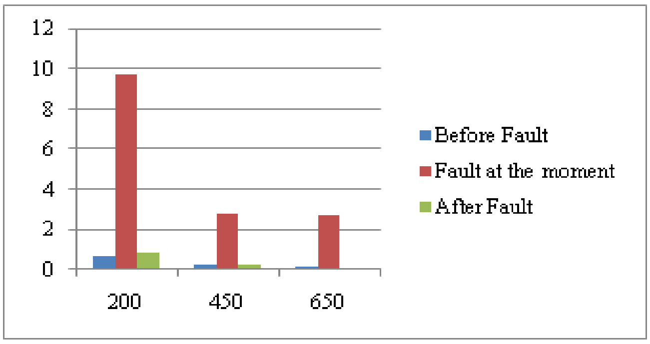


Figure: BarChart of Ia2 Before fault,fault a the moment & After fault

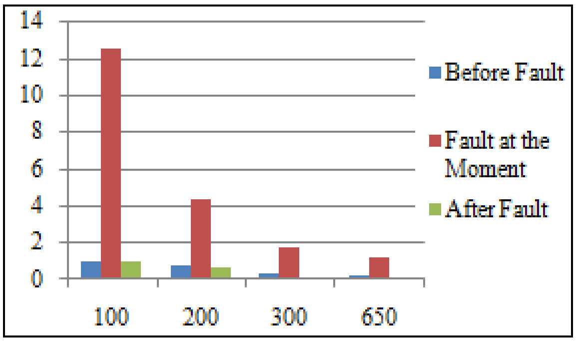


Figure: BarChart of Ib2 Before fault ,Fault at the moment & After fault

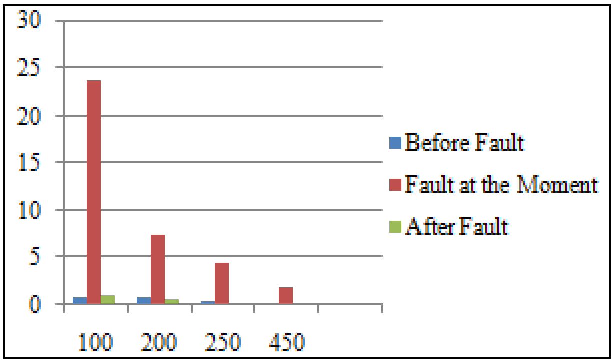


Figure: BarChart of Ic2 Before fault ,Fault at the moment & After fault

FFT Analysis of BTB VSC system for HVDC application for Vabc1 Before Fault ,Fault at the Moment,After Fault

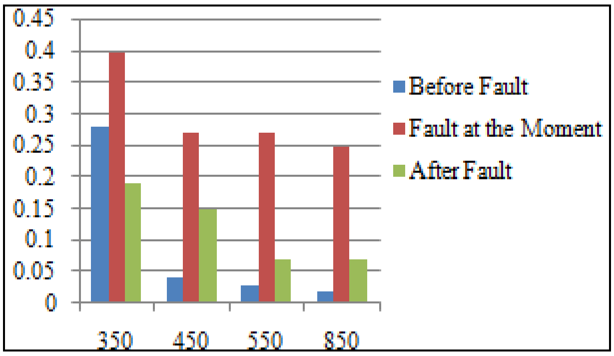


Figure: BarChart of Va1 Before fault ,Fault at the moment & After fault

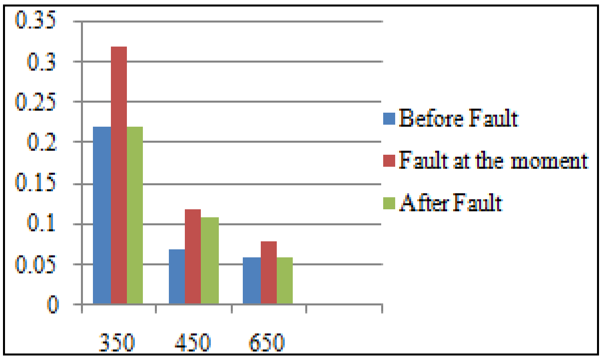


Figure: BarChart of Vb1 Before fault ,Fault at the moment & After fault

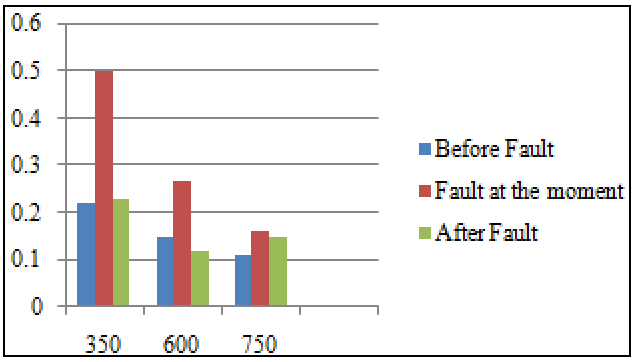


Figure: BarChart of Vc1 Before fault, Fault at the moment & After fault

FFT Anlysis of BTB VSC system for HVDC application for Vabc2 Before Fault ,Fault at the Moment,After Fault

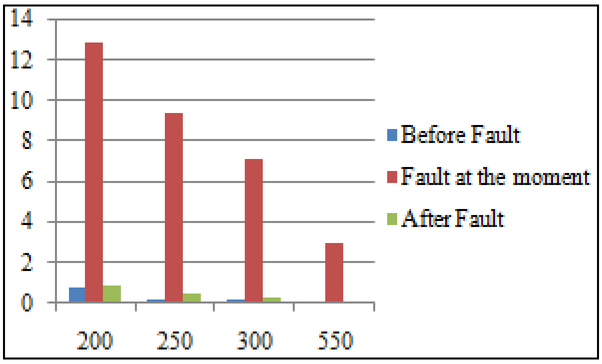


Figure: BarChart of Va2 Before fault ,Fault at the moment & After fault

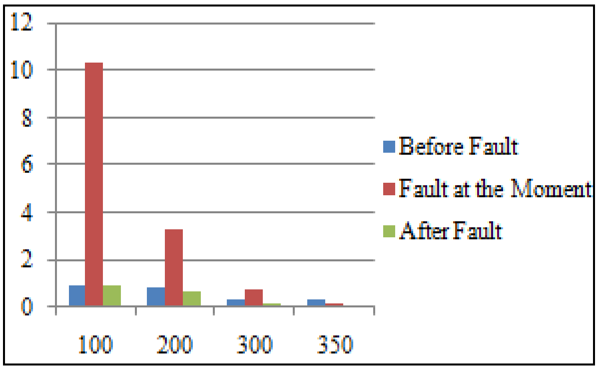


Figure: BarChart of Vb2 Before fault ,Fault at the moment & After fault

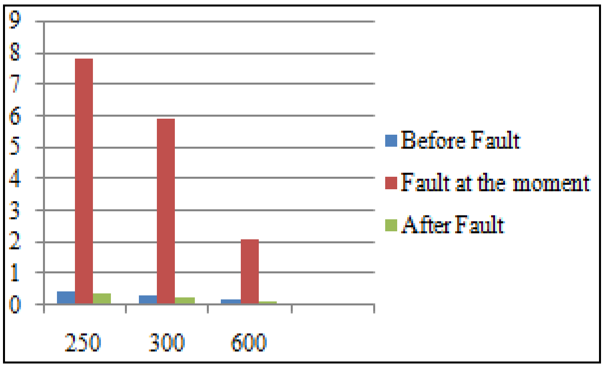


Figure: BarChart of Vc2 Before fault ,Fault at the moment & After fault

6. Conclusion

In this paper, recent advances of the VSC-based HVdc technology are presented. Having analyzed the current state-of-the-art methods of mitigating the dc-link voltage fluctuations under grid faults and disturbances, we have proposed reference frame.. The scheme, however, utilizes the interaction of the converters, the load, bus voltage, and their derivatives to compensate for the phase delay in the current regulator. The proposed scheme was explained through a back stepping control method in which its Lyapunov-based structure ensures the stability of the system. From FFT Analysis it is observed that harmonic distortion is more at the moment of fault and is less before and after the fault.

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