

8Kb Logic Compatible DRAM based Memory Design for Low Power Systems

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Abstract: 8Kb DRAM based memory is implemented for low power systems. 3T DRAM gain cell utilizing preferential boosting is used to achieve large data retention time and low leakage current which contributes to low power consumption. Current mode sense amplifier is designed for read operation to achieve high speed which gives output in voltage mode. There are two 4Kb sections in memory architecture which are controlled by internal control circuitry. This architecture has simplest write back circuitry. This Design performs all specific memory functions. This test memory has 20 pins. This design is done in 180nm CMOS technology

Keywords: DRAM, Decoder, Sense amplifier, Control circuit, Logic gates.

1. Introduction

Modern VLSI systems demands on chip memory. For better performance of system these memories should offer small size, fast operation and low power consumption. Random Access Memories are used as cash memories in systems, 6T Static Random Access Memories offer fast operation and are widely used for the same. As the increasing need of large memories 6T SRAM occupy large area as they use 6 MOS transistors to store one bit data, as an alternative Dynamic Random Access Memories are used to store data for large memories, which take lesser area and allows higher cell density. Along with less area DRAM cells offer low cost per bit.

At the same time DRAM based memories have their drawback, these memories suffer poor data retention time due to leakage currents. Which results in loss of data. These leakage currents also contribute to high static power consumption. If data retention time is increased, by decreasing leakage current we can achieve less static power consumption. To overcome this problem of leakage current Luk et al. proposed a 3T1D gain cell where a gated-diode is used to preferentially boost the cell voltage via capacitive coupling [2]. But this approach uses an additional device and occupy large area another solution to achieve high data retention time was proposed by Ki Chul Chun[1] Which is used in this design.

Memory architecture contributes to device performance and power consumption of the system[6]-[8]. This paper shows a controlling circuitry which is design to achieve low power consumption.

This paper contains six sections. Section II explains basic DRAM structure and DRAM structure which is used in this paper. Sections III explains about sense amplifier and write back circuitry, section IV explains architecture and controlling circuitry. In section V Designed memory and Simulation results are discussed, and section VI gives conclusion.

2. Basic and Low Power Dram Cell

Basic 3T DRAM structure is shown in Fig.1 (a) which has a write access transistor, read access transistor and a storage transistor. PMOS devices are chosen over NMOS devices because they have significantly less gate tunneling leakage current, which extends the data retention time [1].

When WWL signal switches to low logic level, WBL signal is transferred to storage node, when WWL signal again switches to high logic level, transferred WBL signal remains as stored data on gate capacitance of storage transistor. For read operation RBL is either pre-charged or pre-discharged based on the design of sense amplifier which gives the cell data by comparing the RBL with a reference read bit line. This basic 3T DRAM cell has its data retention time in the range of microseconds, and data is lost due to leakage currents flowing through transistors, to compensate this data loss DRAMs require time to time refreshing memory.

This leakage current and refresh current contributes to large power consumption. Ki Chul Chun, Pulkit Jain and Chris H. Kim proposed a DRAM structure to increase data retention time without the need of any additional device [1]. which is shown in Fig.1(b) it has same working and storage mechanism as that of basic 3T DRAM cell here the source of storage transistor is connected to RWL which provides a stronger coupling effect. Hence improves data retention time and reduces the amount of leakage current thus it achieves low power consumption.

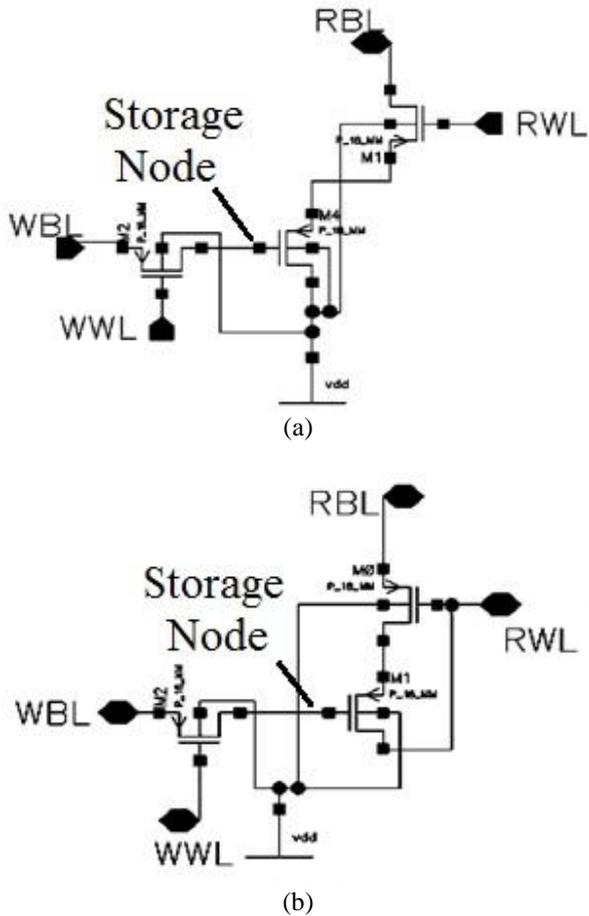


Figure 1: (a) basic DRAM cell (b) Low power DRAM cell

3. Sense amplifier and write back circuit

Sense amplifier design defines the performance of memory. Here current mode sensing is preferred over voltage mode sensing to achieve high speed operation as current mode sense amplifiers offer small input impedance [3],[4]. Fig2 (a) shows the diagram of sense amplifier used in this design. It has two stages first stage detects the data and next stage is buffer which gives full swing data, sensing is being done in two stages because there is a limited area for sense amplifiers as they have to match pitch size of storage cell. RBLP and RBLQ pins are connected to the read bit lines of the arrays at both the sides which are always pre-charged at VDD by a pair of PMOS transistors which have their gate terminals always grounded.

When RWL signal is enabled in a particular memory cell, current flowing through one of the branch of sense amplifier changes based on the location of cell being read, and a little fluctuation will be shown at node A and

B, when signal RE is enabled sense amplifier will go on and node A and node B will give complimented outputs which are then passed through buffers, Hence read_outP and read_outQ will also be complemented to each other, If arrayP is being read read_outP will hold the datum and for arrayQ read_outQ will hold datum. These read_out pins are passed through a controlling circuit which gives the stored data. This control circuit is explained in section IV.

As DRAM memories need to be refreshed periodically a write back circuit is needed, followed by sense amplifier, A simplest write back circuit can be created using D-Latches.

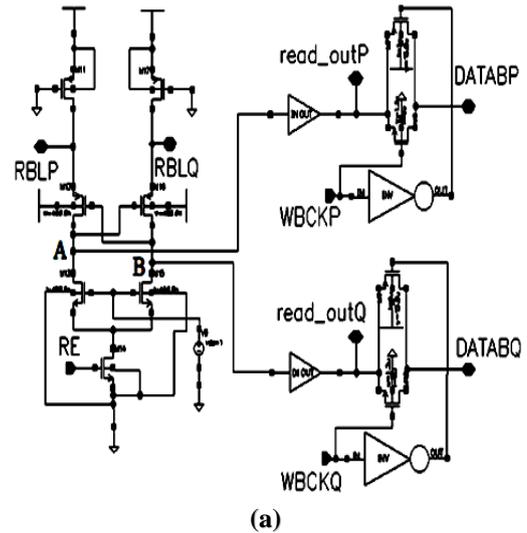
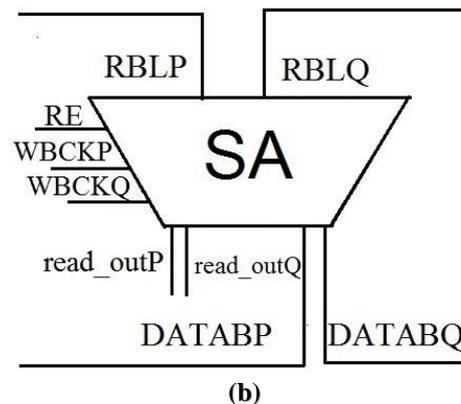


Figure 2: (a) Sense amplifier circuit (b) Symbolic view of sense amplifier



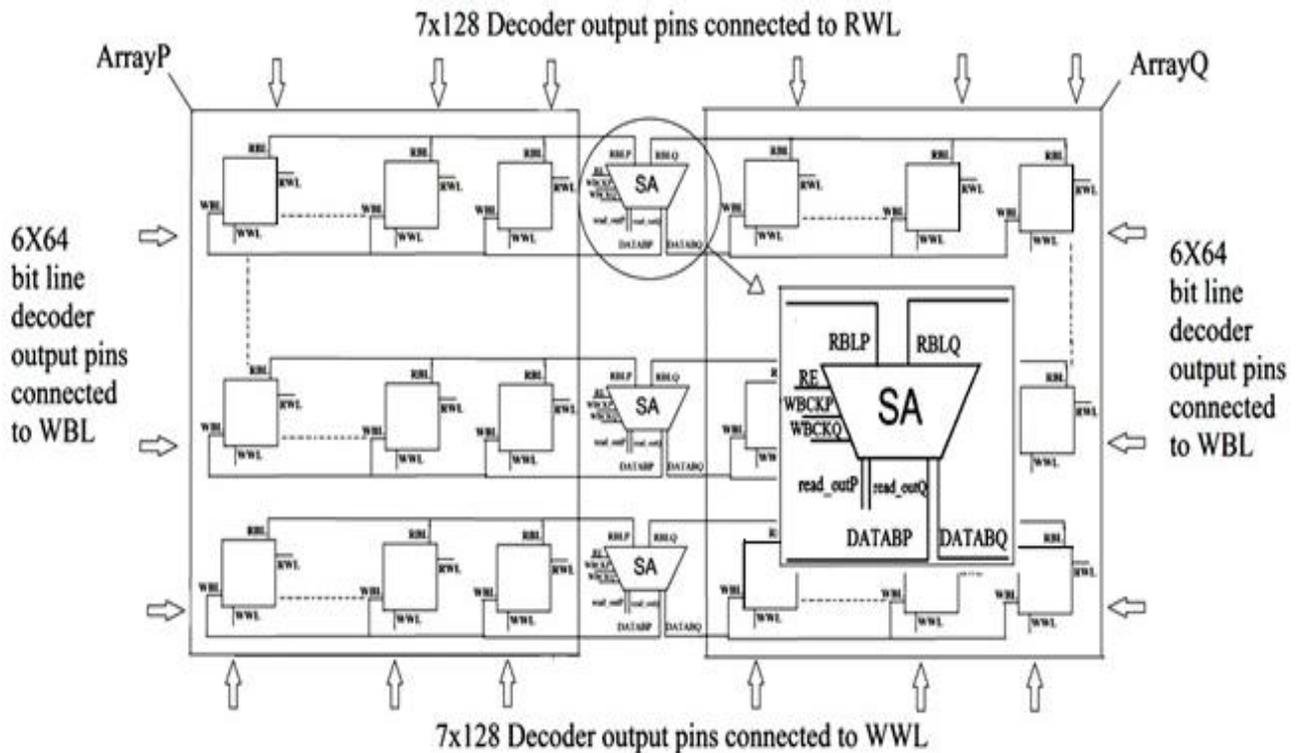


Figure 3: Architecture of 8Kb DRAM based memory

As shown in Fig.2(a) Both buffers outputs are connected to D-Latch, When WBCKP/WBCKQ goes high write back operation will be performed for respective bit line. This write back operation is also controlled by external control circuit explained in section IV. Fig.2 (b) shows the symbolic representation of sense amplifier.

4. Architecture and Control Circuitry

Memory architecture plays an important role in overall device functioning, read/write access time and overall power consumption, by developing a control circuitry extra power consumption can be reduced.[5] Section A explains architectural considerations and section B explains designed control circuitry.

A. Architecture and operation of 8Kb array:

architecture of 8kb memory array is shown in fig.3 this 8Kb memory block has two 4Kb sections arrayP and arrayQ, each have 64 rows and columns. Sense amplifiers are located at the centre of both arrays for each bit line Thus there are 64 bit lines and 128 word lines including both arrays. A 7x128 decoder is used to access word lines and 6x64 pass transistor based column decoder is used to access bit lines and write data. Pin diagram of this memory is shown in Fig.4.

Write operation: Address pins A0-A6 are used to access one of 128 word lines, and address pins A7-A12 will access a particular bit line through column decoder in both arrays and when WE signal is enabled data DI will be allowed to be written in the accessed cell, write control circuitry is shown in Fig.5(a).bit lines are pre-charged to a moderate voltage level before write

operation by keeping precharge value to a moderate level delay is reduced.

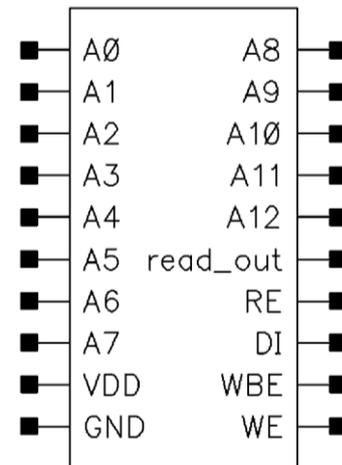
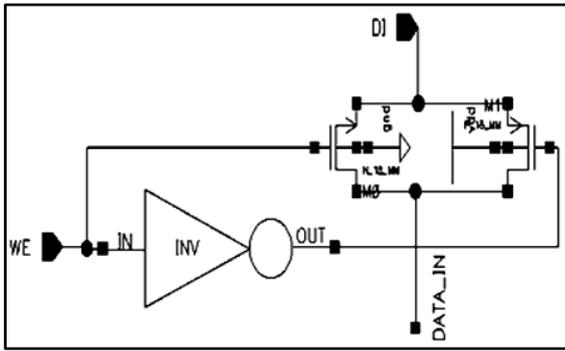
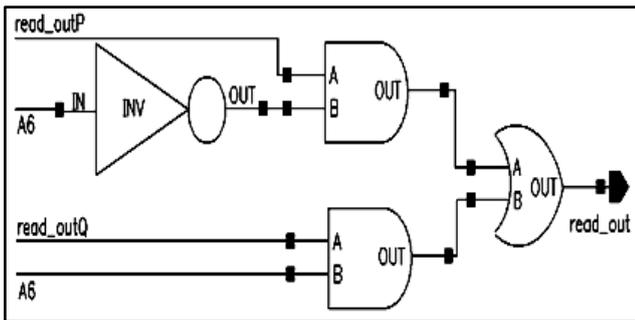


Figure 4: Pin diagram of 8Kb Memory

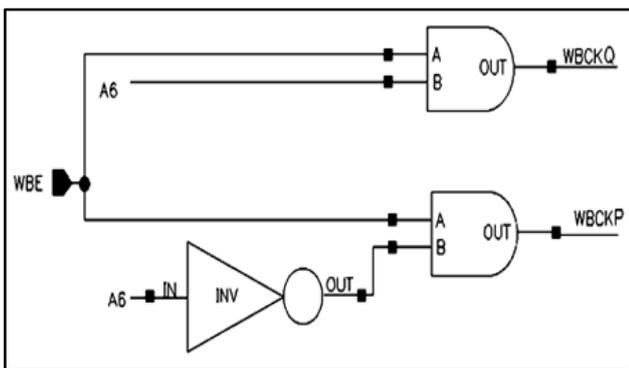
Read operation: Read operation in memories is done using a sense amplifier Current mode sense amplifier is connected at the centre of both the arrays which is explained in section III. This sense amplifier will keep Read bit lines of both the arrays pre-charged at VDD level. when RE is enabled datum of accessed cell is fetched on read_outP if cell of array P is being read or it will appear on read_outQ if cell of array Q is being read. These read_out pins of sense amplifier are followed by a control circuit to get the actual read data. which is shown in Fig5(b).



(a)



(b)



(c)

Figure 5: (a) write control circuit (b)read control circuit (c)write-back control circuit.

B. Controlling Circuitry: for this memory three control circuits are made one to control write operation, second to control read operation and, third to control write back operation. As discussed in section A ,this memory is divided in two arrays : arrayP and arrayQ both have 64 word lines each when pin A6 is 0 arrayP is accessed and when A6 is 1 array Q is accessed, maximum controlling is done by pin A6.

Write Control: write control circuit used in this design is shown in fig.5(a), here DI is the external data input which is given to a D-latch which is controlled by WE pin, when WE is logic high D-Latch will allow DI to be transferred to data input pin of column decoder, this column decoder will transfer data to bit lines.

Read Control: When pin A6 is logic 0 arrayP will be read whose output will appear on read_outP and when pin A6 is logic 1 arrayQ will be read and its output will appear

on read_outQ. The actual output data will go on pin read_out depending on logic level of pin A6. This control circuit is shown in Fig 5(b).

Write Back Control: After reading the datum from cell, write back operation can be performed using the concept of read control, using pin A6, i.e. when A6 is 0 WBCKP will be active and data will be written back on bit line of array P, and when A6 is 1 WBCKQ will be active and data will be written back to arrayQ. This control circuit is shown in Fig 5(c) .

5. Designed memory and Simulation Results

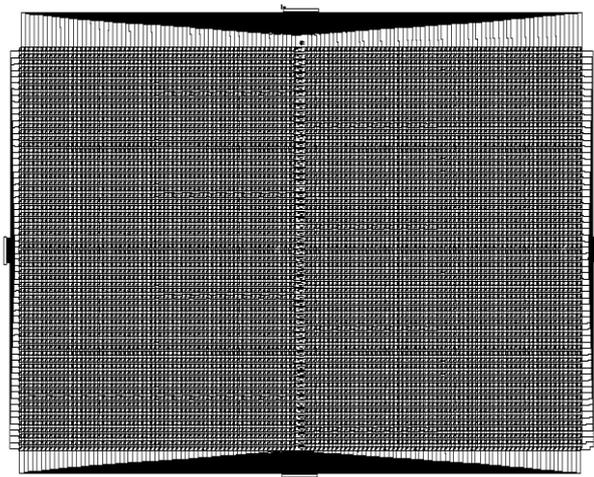
This 8 Kb memory was implemented on 180nm CMOS technology using Cadence EDA tool in 1.8 supply voltage architecture of this memory is explained in section VI . Since this design uses PMOS 3T gain cell hence when it transfers logic 0 data from bit line to word line there is a threshold voltage gap and full swing data is not transferred for full swing data a negative stimulus is applied to gate terminal which is below threshold voltage of PMOS i.e. – 600mV [1].

Simulation waveforms of 8Kb memory array which is shown in Fig 6(a), are given in Fig. 6(b), Simulation results of this memory are given in table1. In the first waveform data 0 is to be written on storage node, when the signal WE goes logic high i.e. when WE is enabled after that data on the storage node changes. The second waveform is for read operation which is reading stored data 0 from cell, waveform shows that, when RE signal goes high i.e. when RE signal is enabled read_out pin shows the stored data and at the same time stored node voltage is also amplified.

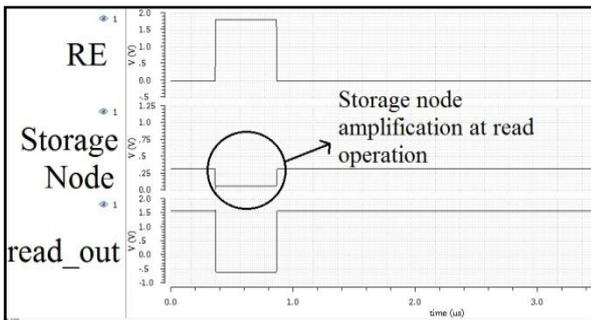
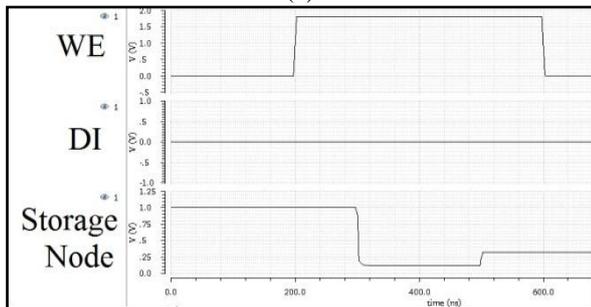
Write access time of memory is considered to be the delay between WE (write enable) signal and storage node voltage, And read access time is considered as delay between RE (read enable) signal and read_out pin, all enable signals in this design are active high logic pins.

Table1: Simulation results of 8Kb test memory

Cell area for 180nm CMOS technology	.59uM x .59uM
Write access time	667pS
Read access time	1nS
Average power consumption	14mW



(a)



(b)

Figure 6: (a) 8Kb test memory (b) Simulation results of 8Kb memory

6. Conclusion

In this paper implementation of a 8Kb memory was shown which includes a control circuitry whole design is done by keeping the requirement of low power consumption in mind. By increasing data retention time, time gap for refreshing memory would increase and leakage current of memory cell decreases. While designing sub circuitries for low power consumption there was tradeoff between speed and power consumption.

References

- [1] Ki Chul Chun, Pulkit Jain, Jung Hwa Lee, and Chris H. Kim, "A 3T Gain Cell Embedded DRAM Utilizing Preferential Boosting for High Density and Low Power On-Die Caches" *IEEE J. SOLID-STATE CIRCUITS*, VOL. 46, NO. 6, JUNE 2011.

- [2] W. K. Luk, J. Cai, R. H. Dennard, M. J. Immediato, and S. V. Kosonocky, "A 3-transistor DRAM cell with gated diode for enhanced speed and retention time," in *Proc. VLSI Circuits Symp.*, 2006, pp.184–185.
- [3] E. Seevinck, P. J. van Beers, and H. Ontrop, "Current-mode techniques for high-speed VLSI circuits with application to current sense amplifier for CMOS SRAM's," *IEEE J. Solid-State Circuits*, vol. 26, no. 4, pp.525–536, Apr. 1991
- [4] J. Sim, H. Yoon, K. Chun, H. Lee, and S. Hong *et al.*, "A 1.8-V 128-Mb mobile DRAM with double boosting pump, hybrid current sense amplifier, and dual-referenced adjustment scheme for temperature sensor,"
- [5] Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic, "Digital Integrated Circuits a Design.
- [6] Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic, "Digital Integrated Circuits a Design.
- [7] Tegze P. Haraszti, "CMOS Memory Circuits".
- [8] Neil H. E. Weste, Kamran Eshraghian Principles of CMOS VLSI Design .