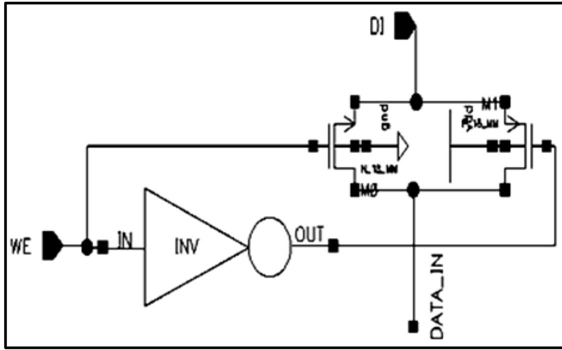
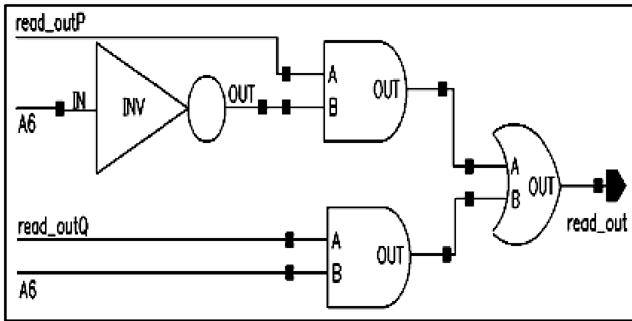
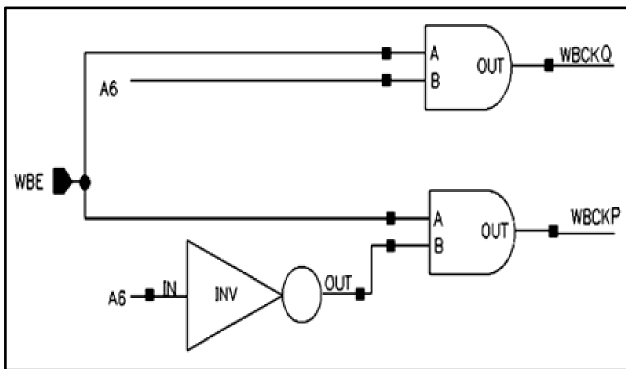


(a)



(b)



(c)

Figure 5: (a) write control circuit (b)read control circuit (c)write-back control circuit.

B. Controlling Circuitry**:** for this memory three control circuits are made one to control write operation, second to control read operation and, third to control write back operation. As discussed in section A ,this memory is divided in two arrays : arrayP and arrayQ both have 64 word lines each when pin A6 is 0 arrayP is accessed and when A6 is 1 array Q is accessed, maximum controlling is done by pin A6.

Write Control: write control circuit used in this design is shown in fig.5(a), here DI is the external data input which is given to a D-latch which is controlled by WE pin, when WE is logic high D-Latch will allow DI to be transferred to data input pin of column decoder, this column decoder will transfer data to bit lines.

Read Control: When pin A6 is logic 0 arrayP will be read whose output will appear on read_outP and when pin A6 is logic 1 arrayQ will be read and its output will appear on read_outQ. The actual output data will go on pin read_out
depending on logic level of pin A6. This control circuit is shown in Fig 5(b).

Write Back Control: After reading the datum from cell, write back operation can be performed using the concept of read control, using pin A6, i.e. when A6 is 0 WBCKP will be active and data will be written back on bit line of array P, and when A6 is 1 WBCKQ will be active and data will be written back to arrayQ. This control circuit is shown in Fig 5(c) .

5. Designed memory and Simulation Results

This 8 Kb memory was implemented on 180nm CMOS technology using Cadence EDA tool in 1.8 supply voltage architecture of this memory is explained in section VI . Since this design uses PMOS 3T gain cell hence when it transfers logic 0 data from bit line to word line there is a threshold voltage gap and full swing data is not transferred for full swing data a negative stimulus is applied to gate terminal which is below threshold voltage of PMOS i.e. – 600mV [1].

Simulation waveforms of 8Kb memory array which is shown in Fig 6(a), are given in Fig. 6(b), Simulation results of this memory are given in table1. In the first waveform data 0 is to be written on storage node, when the signal WE goes logic high i.e. when WE is enabled after that data on the storage node changes. The second waveform is for read operation which is reading stored data 0 from cell, waveform shows that, when RE signal goes high i.e. when RE signal is enabled read_out pin shows the stored data and at the same time stored node voltage is also amplified.

Write access time of memory is considered to be the delay between WE (write enable) signal and storage node voltage, And read access time is considered as delay between RE (read enable) signal and read_out pin, all enable signals in this design are active high logic pins.

Table1: Simulation results of 8Kb test memory

Cell area for 180nm CMOS technology	.59uM x .59uM
Write access time	667pS
Read access time	1nS
Average power consumption	14mW

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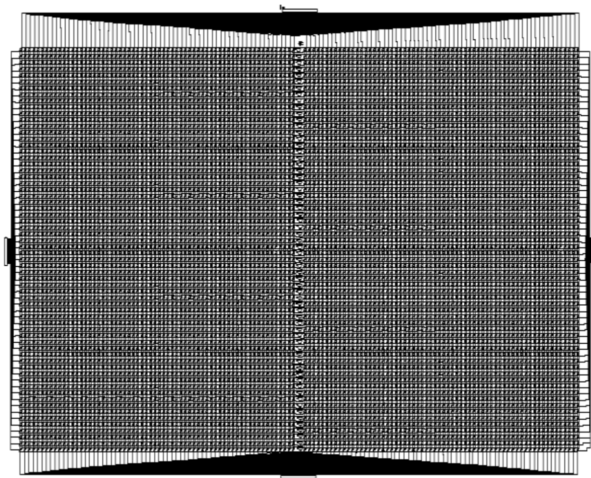
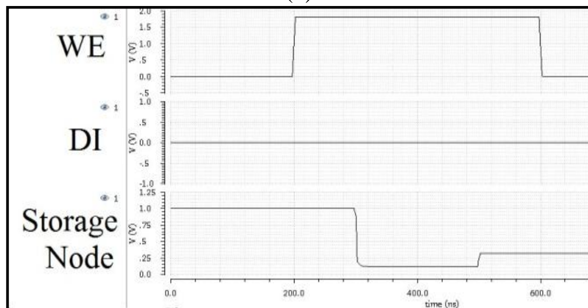
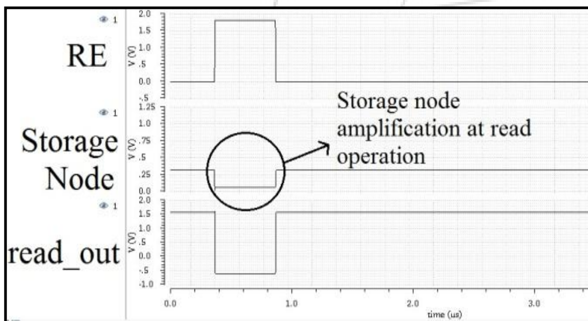


(a)





(b)

Figure 6: (a) 8Kb test memory (b) Simulation results of 8Kb memory

6. Conclusion

In this paper implementation of a 8Kb memory was shown which includes a control circuitry whole design is done by keeping the requirement of low power consumption in mind. By increasing data retention time, time gap for refreshing memory would increase and leakage current of memory cell decreases. While designing sub circuitries for low power consumption there was tradeoff between speed and power consumption.

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