inputs are used for charging and discharging of load capacitance. When the input signal In1 is low, the bit line capacitance 'C_{bl}' charges to the peak voltage of the power clock voltage through diode D1. When the input signal in1 is high, the bit line capacitance 'C_{bl}' discharges to the power clock through diode D2. Complimentary action takes place in the other bit line 'C_{blb}'.

4. Simulation Results And Layout Design

Comparison of performance of 1 bit conventional asymmetric 6T SRAM cell and adiabatic asymmetrical 6T SRAM cell

The performance of the adiabatic SRAM cell was compared with the non adiabatic Asymmetric SRAM cell. The performance parameters considered are total energy, power dissipation, write delay, read delay and static noise margin [6,9].

1. Energy

The energy relations in the conventional 6T SRAM are as follows

Energy during read time

$= \int f \times (C_{bl} + C_{dl}) \times \Delta V_{bl} \times V_{dd}\, dt$

Energy during write time

$= \int f \times (C_{bl} + C_{dl}) \times V_{dd}^2\, dt$

Where f is the clock frequency and C_{bl} and C_{dl} are the capacitances of a bit line and a Data line.

In the same way the energy relations in the Adiabatic 6T SRAM are as follows

Energy during read time

$= \int f \times (C_{bl} + C_{dl}) \times \Delta V_{bl} \times VPC\, dt$

Energy during write time

$= \int f \times (C_{bl} + C_{write} + C_{dl}) \times VPC^2\, dt$

Where f is the clock frequency, C_{bl} bit line capacitance, C_{write} and C_{dl} are the capacitances of a bit line, write driver and a Data line. VPC is time varying power clock voltage.

Energy during hold time

$= \int I_{leak} \times V_{dd}\, dt$

$I_{leak} = I_{subthreshold} + I_{gate\ leak}$

Where I_{leak} is total leakage current, $I_{sub\ threshold}$ is sub threshold leakage current and $I_{gate\ leak}$ is gate leakage current

2. Read Delay

The read delay is the time delay between 50% level change in the word line signal to 50% level change in the output of the sense amplifier. The read delay is found to be reduced in case of adiabatic SRAM as compared to conventional SRAM.

3. Write Delay

The write delay is defined as the difference in time between 50% level change in the word line signal and the 90% level of the storage node signal. Due to increased resistance of the write driver circuit the write delay is increased in the Adiabatic SRAM when compared to the non adiabatic SRAM

4. Static Noise Margin (SNM)

SRAM bit cell immunity to the failure is measured by SNM. It is defined as the maximum noise that can be tolerated at the input of the SRAM without changing its status. The size of the smallest square in the butter fly curve of the SRAM gives SNM. The SNM of both SRAMs is 455.75mV.

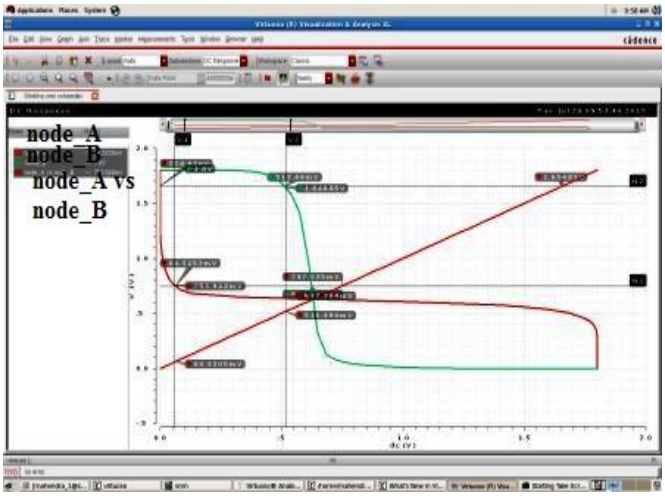

Figure 1.4: SNM of SRAM cell

Table 1.1: Performance parameters of both conventional and adiabatic SRAM cells

S.No.	*Performance Parameters*	*Conventional SRAM*	*Proposed Adiabatic SRAM cell*
1.	Technology	180nm	180nm
2.	Power Dissipation	52.84uW	34.39uW
3.	Energy Consumption	1.23nJ	1.07nJ
4.	SNM	455.75mV	455.75mV
5.	Write Delay	0.35ns	8.44ns
6.	Read Delay	92.32ps	0.29ps

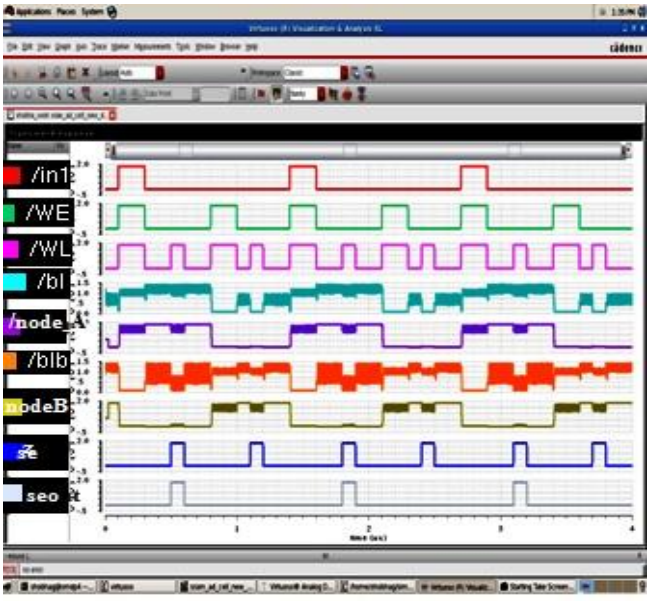

Figure 1.5: Waveforms of Asymmetrical 1 bit Adiabatic SRAM cell

Where;

In1 input to write diver connected to bitline bl and its inverted input to write driver connected to bitline blb.

WE= Write enable, WL= Word line for access transistor, Node_A, Node_B are the storage pin of SRAM,

Se, Seout are the sense amplifier input and output port for read operatipon.

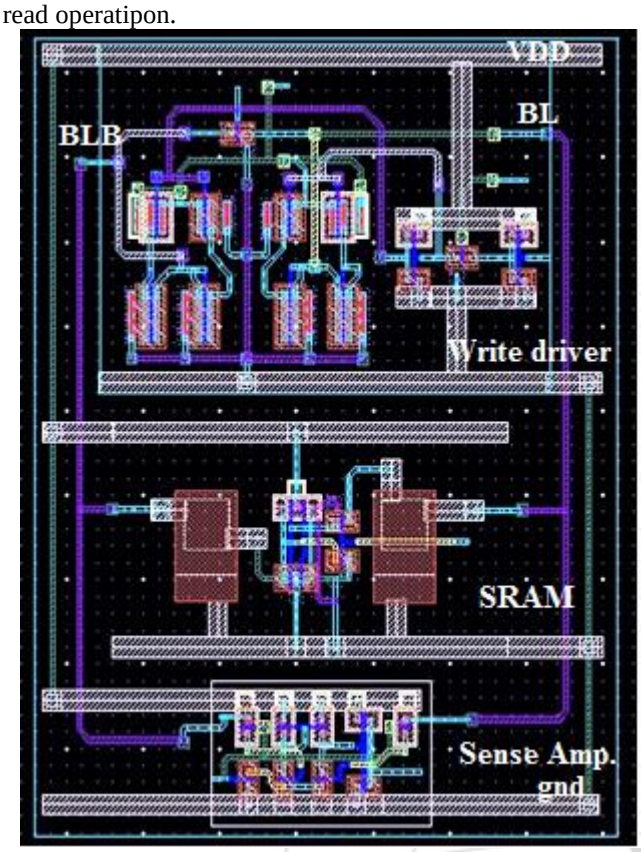

Figure 1.6: Layout of Asymmetrical 1 bit Adiabatic SRAM cell

5. Conclusion

In this work adiabatic technique is used for reduction of power dissipation with no performance degradation. The 35% reduction in power in SRAM cell is achieved as compared to conventional one. In future, this technique can be used in large array of memory design.

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