10. Conclusion

A new low power and area efficient 4x4 array multiplier had been successfully designed and simulated. Results are compared with the conventional CMOS design. The new improved designs of gates and Adder cells have been implemented which shows better result. The methodology used here shows full swing outputs unlike the basic GDI technology.

In future perspective, higher order multiplier can be implemented using the same methodology, pipelining of the circuit can be done to increase the throughput. Other digital circuits can also be implemented using the GDI technique and they can be put in together to make a complete IC or an ASIC.

References

[1] A. Morgenshtein, A. Fish, I.A. Wagner,(2002) "Gate-Diffusion Input (GDI) – A Power Efficient Method for Digital Combinational Circuits," IEEE Trans. VLSI, vol.10, no.5,566-581.
[2] Z. Abid, H. El-Razouk, D.A. El-Dib,(2008) "Low Power Multipliers based on new Hybrid Full Adders" Microelectronics Journal, Volume 39, Issue 12, 1509–1515.
[3] V. Foroutan, M. Taheri, K. Navi, A.a. Mazreah, (2014)"Design of two Low-Power Full Adder cells using GDI structure and Hybrid CMOS logic style", Integration, the VLSI journal, Volume 47, Issue 1,48-61.
[4] A. Morgenshtein, V. Yuzhaninov, A. Kovshilovsky, A. Fish,(2014) "Full-Swing Gate Diffusion Input logic-Case-study of low-power CLA adder design," Integration, the VLSI journal, Volume 47, Issue 1, 62-70.
[5] N. Ravi, Y. Subbaiah, Dr. T. J. Prasad, Dr. T. S. Rao,(2011)"A Novel Low Power, Low Area Array Multiplier Design for DSP Applications," International Conference on Signal Processing, Communication, Computing and Networking Technologies,254-257.
[6] J. Gupta, A. Grover, G. K. Wadhwa, N. Grover,(2013) "Multipliers using low power adder cells using 180nm Technology", International Symposium on Computational and Business Intelligence.
[7] N. Weste and K. Eshraghian, Principles of CMOS Digital Design MA: Addison-Wesley

Licensed Under Creative Commons Attribution CC BY