$$V_{in} = I_s R e^{(V_d/V_t)} \quad (8)$$

Considering that the negative of the voltage across diode is the output voltage V_{out} (see the circuit diagram (figure1)), we can rearrange the equation (6) to get

$$V_{out} = V_t I_{in}(V_{in} / I_s R)$$

The output of the logarithmic amplifier is found to be a symmetric square wave in addition with a negative going waveform of diode drop 0.7V.In order to discard this portion of the waveform the voltage level shifter using opamp circuit has been designed in order to obtain the symmetric clock pulse fed as input to digital CMOS inverter to determine its switching characteristics.

2.1. Performance Of CMOS Inverter: The Dynamic Behavior

The qualitative analysis presented earlier concluded that the propagation delay of the CMOS inverter is determined by the time it takes to charge and discharge the load capacitor CL through the pull-up and pull-down networks, respectively. This observation provides innovative information that getting CL as small as possible is crucial to the realization of high-performance CMOS inverter circuits. Before that we first acquire a knowledge of the major components of the load capacitance before embarking onto an in-depth analysis of the propagation delay of the gate. In addition to this complete analysis, the section also provides a summary of techniques that a designer might use to optimize the performance of the inverter. Since it can be observed that we produce input V_{in} is driven by opamp circuits with zero rise and fall times instead of giving vpulse with certain specifications and taking into account of rise and fall time of capacitor. A symmetric clock pulse with zero rise and fall times will be able to minimize the propagation delay which inturn minimal the delay power product.

With the growing demand of handheld devices like cellular phones, multimedia devices, personal note books etc., low power consumption has become one of the major design metric consideration for VLSI circuits and system with increase in power consumption, reliability problem also increases and cost of packaging goes high. Power consumption in VLSI circuit consists of dynamic and static power consumption. Dynamic power has two terms i.e. switching power due to the charging and removing of the load capacitance and the short circuit power due to the non-zero rise and fall time of the input waveforms [5].

3. Simulation Results & Discussions

Transient analysis is used for circuits with time variant sources (e.g. ac sources and switched dc sources). It calculates all the node voltages and branch currents over a time interval, and their instantaneous values at the out ends. Hence Fig shows the Transient analysis of the digital CMOS inverter. The proposed circuit design is as shown in Figure 3.

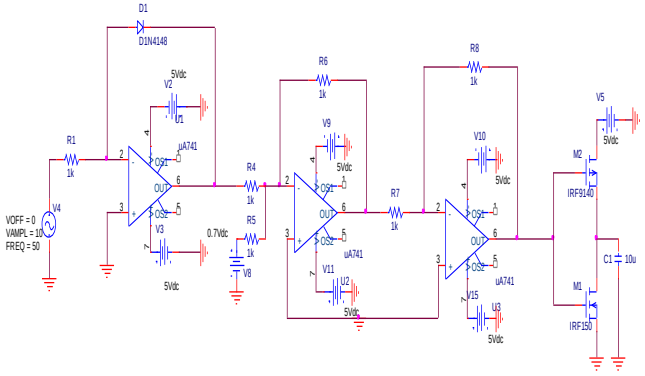

Figure 3: Proposed circuit diagram

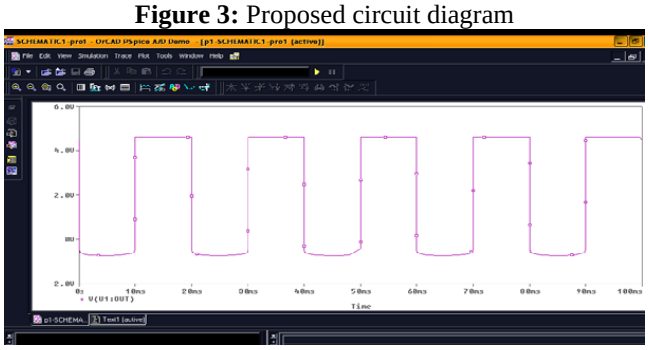

Figure 4: simulation result of log amplifier

The output of logarithmic amplifier is as shown in figure 4 with square wave of voltage range -0.7V to 4.613V.

Figure 5: simulation of voltage shifter of first opamp A1

The simulation of first opamp A1 of voltage level shifter is as shown in figure 5 where votage swings between 0V to -4.613V. The simulated result of second opamp A2 of voltage level shifter is as shown in figure 6 where voltage swings between 0V to + 4.5757V.

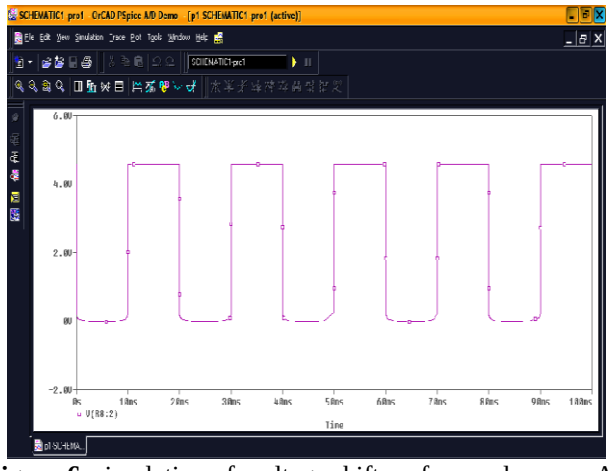

Figure 6: simulation of voltage shifter of second opamp A2

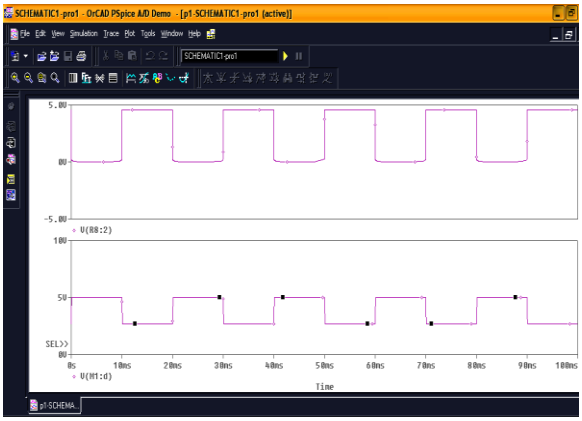

Figure 7: Transient analysis of the digital CMOS inverter.

The clock pulse generated above in figure 6 is fed as an input to the digital CMOS inverter to determine its switching characteristics acts as an inverter shown in figure 7.From figure 7 indicates instead of reducing load capacitor and providing vpulse as an input to the digital CMOS inverter ,the symmetric square wave characterized by zero rise and fall time results with optimized CMOS inverter which will be a basic building block of IC design characterized by minimum propagation delay and delay power product also the overall cost.

4. Conclusion and Future Aspects

The application of logarithmic opamp is proposed in this paper. The proposed circuit is simulated by SPICE. Simulation Results shows the TRANSIENT (switching) Analysis of digital CMOS inverter with zero rise and fall times will be able to minimize the propagation delay which inturn yield minimal delay power product. We can also implement the application of log opamp in future by the consideration of its feature size to analyse the complex digital circuits for lowering the voltage or power which will help to create effective product demanded in market.

References

[1] Mayank Kumar, etal Int. Journal of Engineering Research and Applications www.ijera.com ISSN : 2248-9622, Vol. 4, Issue 5(Version 4), May 2014, pp.133-136
[2] Thomas Kugelstadt (Email: tk@ti.com)Senior Systems Engineer, Industrial Systems.Integrated logarithmic amplifiers for industrial applications.
[3] Shin'ichiro Mutoh ,Takakuni Douseki, Yasuyuki Matsuya Member, Takahko Aoki, Satoshi Shigematsu and Junzo Yamada, Member,1 -V Power Supply High-speed Digital Circuit Technology with Multithreshold-Voltage CMOS, IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 30, NO. 8, AUGUST 1995.
[4] Joyjit Mukhopadhyay and Soumya Pandit, Modeling and Design of a Nano Scale CMOS Inverter for Symmetric Switching Characteristics, Research Article.
[5] Manoj Kumar, Sandeep K. Arya, Sujata Pandey, LEVEL SHIFTER DESIGN FOR LOW POWER APPLICATIONS, International journal of computer science & information Technology (IJCSIT) Vol.2, No.5, October 2010.