the storage elements because unnecessary transitions are not loaded when the clock is not active. CG is illustrated in figure 1 block CG, which inhibits the clock signal when the idle condition is true, is associated with each sequential functional unit. The clock signal is computed by function fcg. CLK is the system clock and CLKG the gated clock of the functional unit.

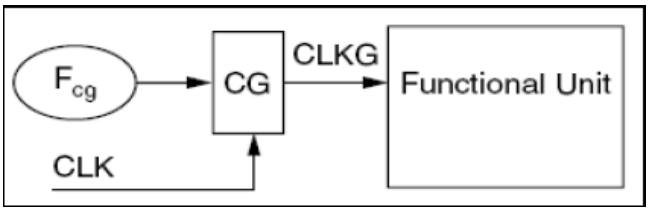

Figure 1: Clock gating principle

It is good design idea to turn off the clock when it is not needed. Automatic clock gating is support by modern EDA tools. They identify the circuits where clock gating can be inserted. The RTL stage is the best point in the design process to optimize dynamic power. At this point, the system architecture is defined, the design is clock cycle accurate, and there is accurate power information available from lower design stages. The only thing left is for hardware designers to have a RTL metric to evaluate and identify candidate logic within a design for optimization of clock gating.

4. How To Implement Clock Gating

There are many clock gating styles available to optimize power in VLSI circuits. They can be:

1) Latch-free based design.
2) Latch-based design.

Latch-Free Based Clock Gating Design

The latch-free clock gating style uses a simple AND or OR gate (depending on the edge on which flip-flops are triggered). Here if enable signal goes inactive in between the clock pulse or if it multiple times then gated clock output either can terminate prematurely or generate multiple clock pulses.

Clock Gate = Clock + Gate (either AND or OR)

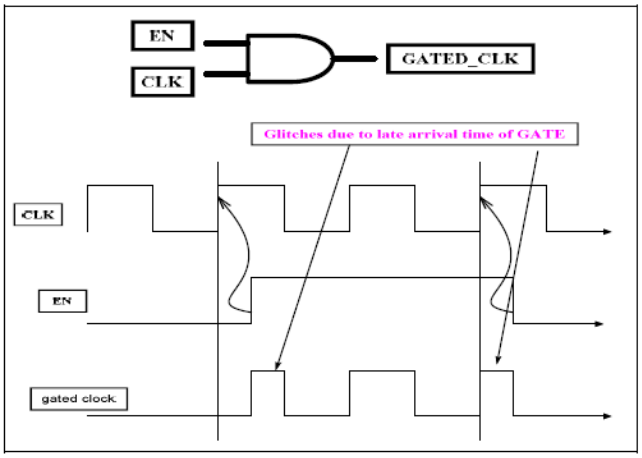

Figure 2: Latch Free Clock Gating

Latch-Based Clock Gating Design

The latch-based clock gating style adds a level-sensitive latch to the design to hold the enable signal from the active edge of the clock until the inactive edge of the clock. Since the latch captures the state of the enable signal and holds it until the complete clock pulse has been generated, the enable signal need only be stable around the rising edge of the clock, just as in the traditional ungated design style.

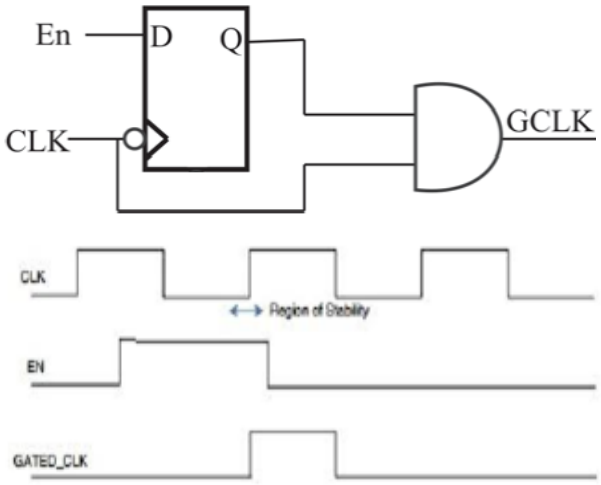

Figure 3: Latch Based Clock Gating

Arithmetic Logic Unit

B. Top Level Schematic Of ALU

There are four inputs ALU as shown in Figure.4. There are A, B, Sel and clock. Out returns the result of the ALU operation. Input Sel3-0 determines which operation is performed. The ALU generates four flags-Zero (Z), Carry (C), Sign (S), and Parity (P) . In all unary function, only the C flag is affected by the Shift function. All flags are affected by the other ALU functions. There are sixty functions depending on 4-bit opcode. There are 8 unary functions. Whose opcode range is 0-7. There are 4 arithmetic operations.

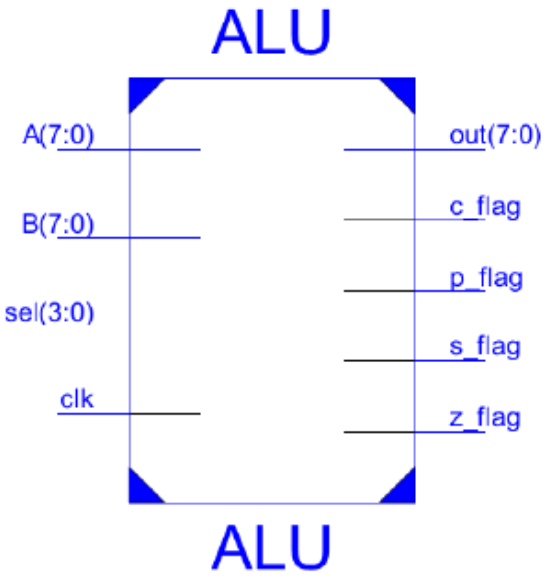

Figure 4: Top Level Schematic of ALU

Whose opcode range is 8-B. There are 4 Logic functions. Whose opcode range is C-F.

C. RTL Schematic Of 8 bit ALU

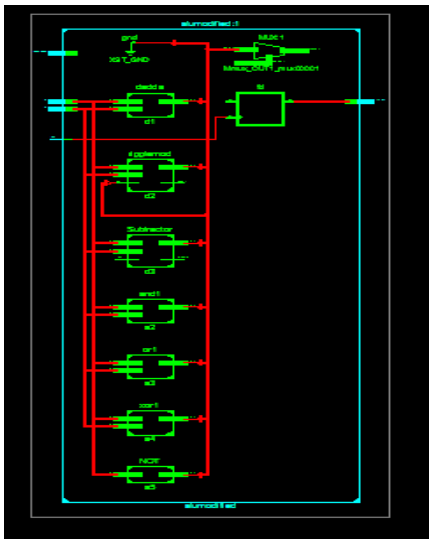

Figure 5: RTL Schematic of ALU

D. Power Consumption Of ALU Without Clock Gate

Table 1: Power Consumption of ALU without Clock Gate

	Clocks	Logic	Signals	IOs	Dynamic	Total
10ns	0.002	0.001	0.001	0.000	0.004	0.057
1ns	0.017	0.009	0.010	0.004	0.041	0.094
0.1ns	0.168	0.048	0.088	0.041	0.345	0.403
0.01ns	1.679	0.153	0.802	0.410	3.044	3.123
1ps	16.795	1.198	7.983	4.099	30.025	30.10

Clock power is 50%, 41.46%, 51.30%, 55.15% and 55.78% of total dynamic power when device operating frequency is 100MHz, 1GHz, 10GHz, 100GHz and 1 THz as listed in Table.1.

ALU With Clock Gate

E. Top Level Schematic Of Latch-Free Clock Gated ALU

Here en is extra output for generation of clock gate as shown in Figure.6. When clock is high, then clock and en fed to AND gate and when clock is low, then clock and en is fed to OR gate. The output of AND/OR gate is gated clock. There is 5 input and output as shown in Figure.6.

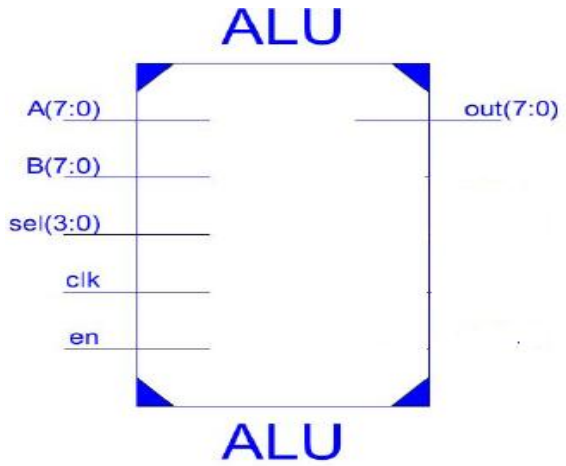

Figure 6: Top Level Schematic of Latch-free Clock Gated ALU

F. RTL Schematic of 8 bit Latch-Free Clock Gated ALU

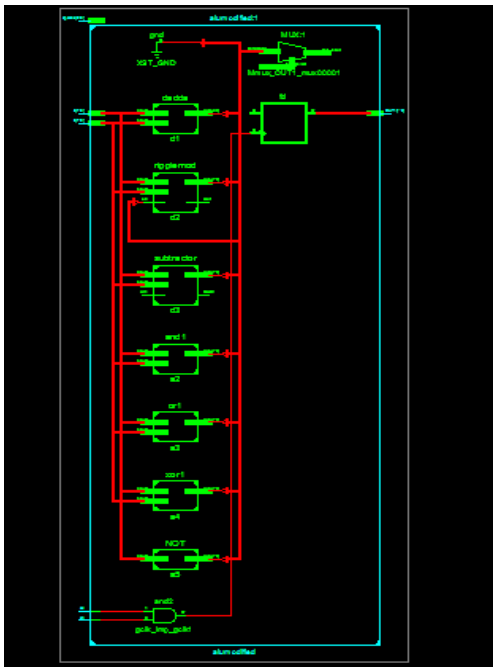

Figure 7: RTL Schematic of Latch-Free Clock Gated ALU

G. Power Consumption Of Latch-Free Clock Gated ALU

Table 2: Power Consumption of Latch-Free Clock Gated ALU

	Clocks	Logic	Signals	IOs	Dynamic	Total
10ns	0.000	0.001	0.001	0.000	0.003	0.055
1ns	0.055	0.009	0.011	0.003	0.028	0.080
0.1ns	0.046	0.048	0.096	0.025	0.215	0.271
0.01ns	0.457	0.153	0.864	0.251	1.725	1.804
1ps	4.572	1.198	8.537	2.505	16.812	16.89

After implementation of Latch-Free clock gating techniques in ALU, Clock power reduces to 17.85%, 23.39%, 26.49% and 27.19% of total dynamic power when device operating frequency is 1GHz, 10GHz, 100GHz and 1 THz as listed in Table.2.

H. Top Level Schematic of Latch-Based Clock Gated ALU

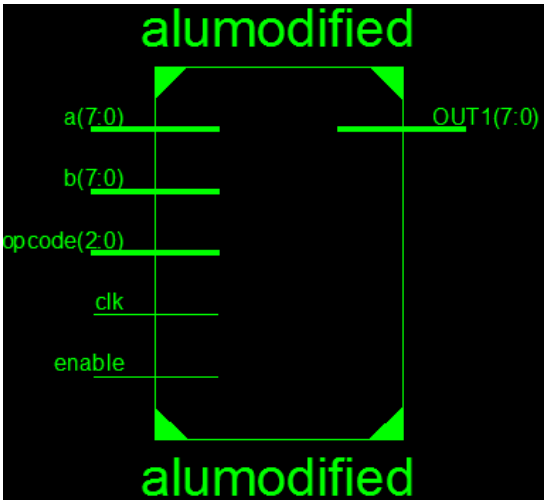

Figure 8: Top Level Schematic of Latch-Based Clock Gated ALU

This design adds a level sensitive latch to the design to hold the enable signal from the active edge of the clock until the inactive edge of the clock. So to removes drawbacks of latch free clock gating.

Here en is extra output for generation of clock gate as shown in Figure.7. When clock is high, then clock and en fed to AND gate clock gating and the output of AND gate is gated clock. There is 5 input and output as shown in Figure.7.

I. RTL Schematic of 8 bit Latch-Based Clock Gated ALU

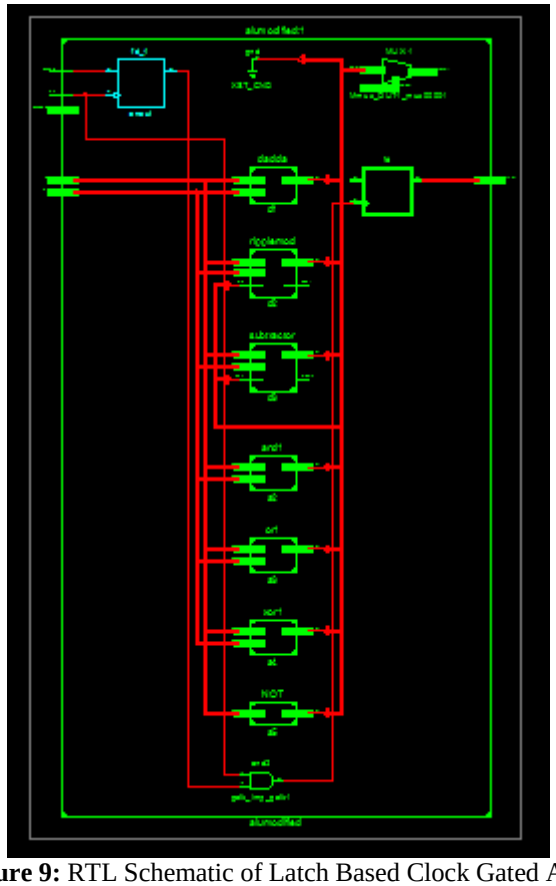

Figure 9: RTL Schematic of Latch Based Clock Gated ALU

J. Power Consumption Of Latch-Based Clock Gated ALU

Table 3: Power Consumption of Latch-Based Clock Gate ALU

	Clocks	Logic	Signals	IOs	Dynamic	Total
10ns	0.000	0.000	0.000	0.000	0.002	0.035
1ns	0.003	0.003	0.005	0.002	0.022	0.048
0.1ns	0.031	0.018	0.041	0.005	0.167	0.180
0.01ns	0.308	0.070	0.351	0.025	0.985	1.203
1ps	3.079	0.567	3.446	1.505	12.546	12.876

After implementation of Latch-Free clock gating techniques in ALU, Clock power reduces to 15%, 17.89%, 20% and 21.56% of total dynamic power when device operating frequency is 1GHz, 10GHz, 100GHz and 1 THz as listed in Table.3.

5. Power Analysis Of Clock Gate Effect

Dynamic Power consists of clock power, logic power, signal power, IO power. Clock power is major contributor in total dynamic power, IO power is the second highest contributor in dynamic power. Clock gating is applied mainly to reduce dynamic power consumption of any target design. We calculate power using XPower on difference device operating frequency 1MHz, 10MHz, 100MHz, 1GHz, 10GHz, 100GHz and 1 THz. Power is directly proportional to frequency and inversely proportional to clock period. 1GHz operating frequency is 1ns clock period and 1 THz operating frequency is 1ps clock period.

Table 4: Power with and without Clock Gate on 1 THz

1ps	Clock	IOs	Dynamic
Without Clock Gate	16795mW	4099mW	30025mW
Latch free Clock Gate	4572mW	2505mW	16812mW
Latch Based Clock Gate	2435mW	1205mW	9005mW

All reduction listed in Table. The power consumption listed in above table is calculated when device operate on 1 THz frequency. There is 72.77% reduction in clock power, 38.88% reduction in IOs power and 44% reduction in dynamic power in compare to power consumption without using clock gating techniques. With latch based clock gating there is 18.67% reduction in clock power, 15.89% reduction in IOs power and 22% reduction in dynamic power in compare to power consumption latch free clock gating technique.

Table 5: Power with and without Clock Gate on 100 GHz

0.01ns	Clock	IOs	Dynamic
Without Clock Gate	1679mW	410mW	3044mW
Latch free Clock Gate	457mW	251mW	1725mW
Latch Based Clock Gate	243mW	129mW	925mW

Latch Based Clock gating technique reduces 18.83% clock power. It also reduces 15.98% IOs power. There is 21.33% dynamic power reduction using clock gating techniques. All reduction listed in Table. The power consumption listed in above table is calculated when operate on 100 GHz frequency.

Table 6: Power with and without Clock Gate on 1 GHz

1ns	Clock	IOs	Dynamic
Without Clock Gate	17mW	4mW	41mW
Latch free Clock Gate	5mW	3mW	28mW
Latch Based Clock Gate	2mW	1mW	16mW

When operating frequency of Latch Based Clock Gated ALU is 1GHz and when we apply clock gating technique on target design, then there is 20%, 18.59% and 25.70% reduction in clock power, IOs power and dynamic power respectively.

Table 7: Power with and without Clock Gate on 100 MHz

10ns	Clock	IOs	Dynamic
Without Clock Gate	2mW	0mW	4mW
Latch free Clock Gate	0mW	0mW	3mW
Latch Based Clock Gate	0mW	0mW	1mW

When Latch Based clock gated ALU operating frequency is 100MHz and when we apply clock gating technique on ALU, then there is 100%, 0% and 15% reduction in clock power, IOs power and dynamic power respectively.

6. Conclusion

Power optimization, traditionally relegated to the synthesis, and placement and routing stages, has moved up to the System level and RTL stages. Hardware designers use clock gating to turn off inactive sections of the design and reduce overall dynamic power consumption. In this paper ,the proposed ALU design is implemented by using Latch based Clock gating .This technique consumes minimum clock power and reduces dynamic power consumption when compared to other clock gating techniques. Hence this Proposed ALU architecture has minimum power Consumption.

7. Future Scope

In this work, we implement our design on 90nm Spartan-3 FPGA. There is open scope to implement this design on 45nm Spartan-6, 40nm Virtex-6 FPGA and 28nm Artix -7 FPGA to achieve energy efficiency in our design on higher level. This target design is 8-bit ALU, so there is scope to design this ALU in form of 16-bit ALU or 32-bit ALU or even higher 64-bit ALU for 64-bit architecture.

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