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Design of E2 Framer and Deframer

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Abstract: ***This paper describes the design and implementation of E1 frame and generating E2 frame multiplexing of 4 E1 Frames, as well as degenerating E1 frame from E2 frame. The design is implemented using Verilog HDL, functionally validated by simulation, carried out RTL and synthesized to get resource utilization and implemented on an FPGA for functionality verification, using Quartus II and Cyclone IV E FPGA family. The designed framer can be used for generation and analysis of E1 frame that has a data rate of 2.048 Mbps and E2 frame that has a data rate of 8.448 Mbps.***

Keywords: E1 frame, CRC, clock divider, E2 frame, STM-1.

1. Introduction

E1 is the basic level of the Plesiochronous Digital Hierarchy (PDH) and is among the most common ways of transmitting voice & data over telephone and data networks. Physically E1 is transmitted as 32 timeslots, but in these one timeslot is used for frame synchronization and one timeslot allocated for signaling call setup and tear down. Unlike Internet data services, E-carrier systems permanently allocate capacity for a voice call for its entire duration.

E1 is one of the fundamental technologies used in telecommunication but there is insufficient provision for network management and in this method inability to identify individual channels in a higher-order bit stream. STM1 is a synchronous digital hierarchy (SDH) is standardized multiplexing protocols that transfer multiple digital bit streams over optical fiber using lasers or light-emitting diodes (LEDs). The method was developed to replace the PDH system for transporting larger amounts of telephone calls and data traffic over the same fiber without synchronization problems. STM-1 Data rate is 155.52 Mbps, 63 E1's are multiplexed in to this STM-1. For this method takes 63 copper lines for Multiplexing and demultiplexing. So this project is concentrated to reduce number of lines by using E2 frame,it reduces 63 lines to 16. E2 frame is generating by multiplexed 4 E1's and degenerating by demultiplexed.

2. Frame Structure

2.1 E1 Frame Structure

Each channel in a frame has 8 bits and is called a time slot, TS as shown in Figure 2.1. Thus, a frame contains a total of 256 bits. Time slots in a frame are numbered from 0 to 31. Each time slot corresponds to a 64Kbps channel carrying 8 bits of either data or an 8 kHz digitized voice sample. Bits in a time slot are numbered from 1 to 8. Time slots are combined using Timing Division Multiplexing (TDM) at 2,048MHz. Thus, a frame is transmitted each 125µs.

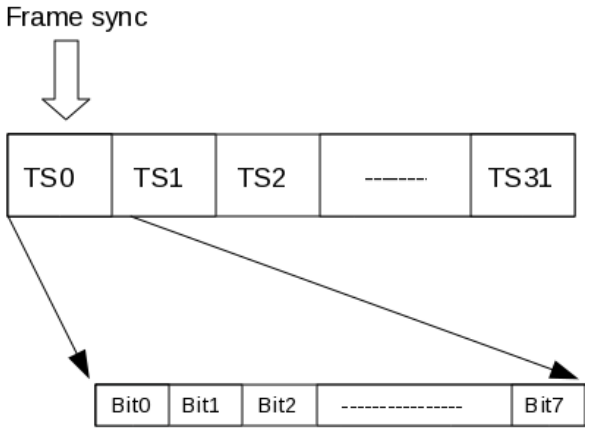

Figure 2.1: E1 frame structure

2.2 E2 Frame Structure

The E2 frame is capable of transporting four E1 signal (8.448 Mbit/s) using bit interleaving manner. The frame comprises of Frame alignment signal, control justification, justification bits and payload as shown in Figure**.**

FAS (1111010000)	RAI	NA	Data Bits (200)
Control Justification Bits	Data (208 Bits)		
Control Justification Bits	Data (208 Bits)		
Control Justification Bits	Justifiction Bits	Data (204 Bits)	

Figure 2.2: E2 frame structure

2.2 Specifications

Data rate for E1 frame
Frame length: 256 bits
Each slot capacity: 64 kbps
Frame repetition rate: 8000 frames/s
Transmission time: 125µs
Data rate: 2.048Mbps

Data rate for E2 Frame

Number of rows: 4 rows
Number of columns: 212 columns
Number of bits/frame: 848 bits
Each slot capacity: 8 kbps
Frame repetition rate: 9962.26 frames/s

Transmission time: 100.3 µs
Data rate: 8.448 Mbps

3. E2 Frame Formatter

3.1 E2 Frame Formatter

E2 is a scalable Frame Formatter, allowing 4 E1 channels [frame signal] to mapped/Demapped into/from E2 Frame.E1 to E2 multiplexing is a several step process of merging 4 E1 lines into a single E2 line, the several steps are illustrated in the below figure.

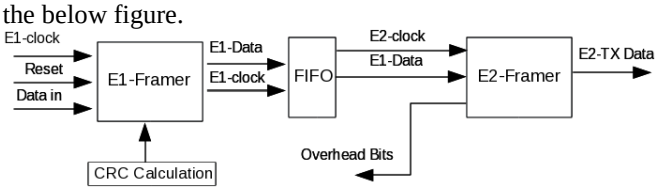

Figure 3.1: E1 to E2 frame generation

The first step is the container; Input signals are placed into the containers. The Second step is E1 framer, it defines E1 frame structure, and The E1 frame comprises FAS, NFAS, and Signaling bits. The last step is generating the E2 frame by multiplexing of 4 E1's using bit interleaving procedure, and it adds FAS for synchronization purpose and justification bits which compensates for the permitted data rate between the E2 signal and the E1 signal.

3.2. E1 Frame

The E1 framing is the first level in the digital hierarchy. The E1 frame carries 30 voice channels in a 256-bit frame. Since 30 channels only require 240 bits, 16 bits are available for framing, signaling, error checking and supervisory communications. These extra 16 bits are divided into two groups of 8 bits each.

3.3. FIFO

To attain synchronization between the lower rate signal [E1], FIFO are placed between the tributaries and the bit interleave [Multiplexer]. Synchronization is achieved by reading out bits from the FIFO with a higher bit rate [E2] when writing bits into it lower bit rate [E1].

3.4. Digital Multiplex

The principle for digital multiplexing is the bit interleaving process in which the tributaries are combined bit by bit to a bit flow. Four lower rate tributaries [E1] are combined by Time Division Multiplexing (TDM) to produce one higher rate signal [E2]. Similarly the demultiplexing process is used to transmit a small number of voice channels.

3.5. Frame Synchronous

Framing synchronous is necessary so that any equipment receiving the E2 signal can synchronize, identify, and extract the individual channels.

3.6. E2 Framer Formatter

The frame formatter is made up of four sets. The four sets are transmitted one after another to make up the complete E2 frame formatter. At each stage when the tributaries are combined, the resulting bit rate is slightly higher than the input bit rate that is, 4 x2048 kb/s = 8192 kb/s, but the actual rate is 8448 kb/s. These extra bits are used for synchronization and justification purpose.

3.7. Deframer

The figure 3.2 shows the block diagram of E2 Deframer. The E2 Frame signal is fed to the Frame Synchronization block which performs frame synchronization as per ITU-T G.703 [8].After the synchronization of transmitter and receiver degenerating E1's by using demultiplexing process, and clock is recovered based on the data rate(the output clock is differ because of justification).

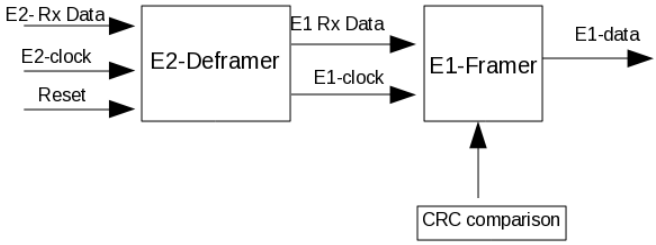

Figure 3.2: E2 Deframer

4. Design & Implementation

4.1 Frame

The Figure 4.1 shows the block diagram of how an E2 frame is generated. The serial E1's data is used to fill the payload section of the E2 frame. At every positive edge of the clock the data is fed into the Framer block. When the RESET signal is set the frame will be reset to the initial value.

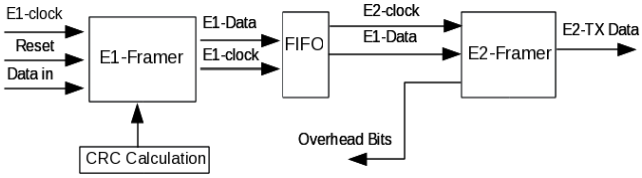

Figure 4.1: E1 to E2 frame generation

The Frame Alignment Signal bits, control justification bits and justification bits are also sent into the framer at appropriate positions to complete the frame.

4.2. Deframe

The figure 4.2 shows the overall block diagram of how an E1 frame is regenerated from the E2 frame. The E2 Frame signal is fed to the Frame Synchronization block which performs frame synchronization as per ITU-T G.703 [1].

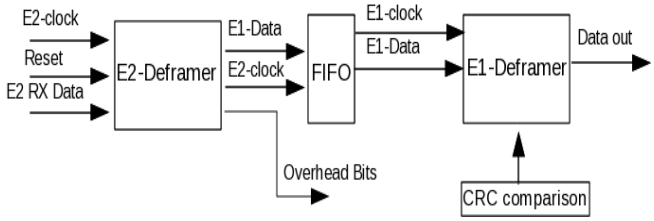

Figure 4.2: E2 frame degeneration

The other inputs to this block are clock and reset. When reset is made high, all the internal registers are set to predefined values. When reset goes low, this block takes the serial data from the receiver on negative edge of the clock.

Frame Alignment Signal block: The Frame Alignment Signal (FAS) block is used at the Receiving end to determine whether the frame has started or not. This is done by comparing the first ten bits with a fixed pattern which is the Frame Alignment Word and is used to recognize the beginning of an E2 frame. FAS has a default value of 1111010000.The Frame Alignment Signa1 block will wait for these values and whenever it encounters all the ten values the frame signal will be asserted to indicate the start of the frame. Once the head signal is asserted the E2 data will be extracted using demultiplexing technique.

5. Tests and Results

Figure depicts the simulation result of the E2 frame generator module. This figure illustrates the functional validation of E2 Frame FAS bits.

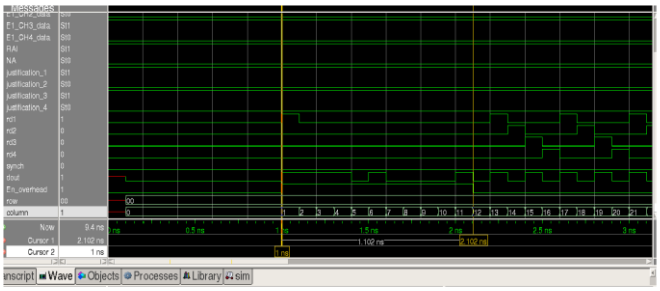

Figure 5.1: E2 overhead bits generation

Figure depicts the simulation result of the E2 frame generator module. This figure illustrates the functional validation of E2 frame data bits.

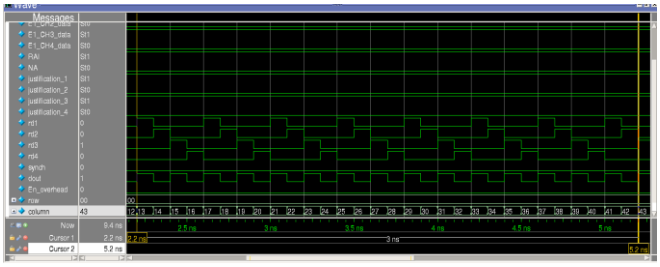

Figure 5.2: E2 data bits generation

Figure depicts the simulation result of the E2 frame generator module. This figure illustrates the functional validation of E2 frame justification bits.

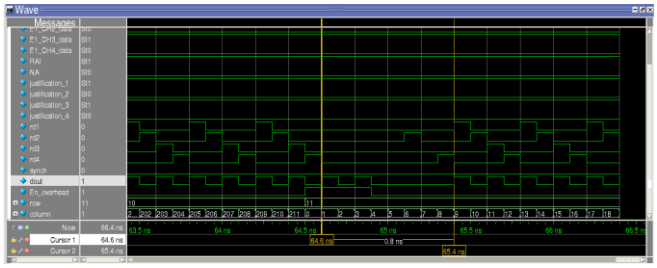

Figure 5.3: E2 justification bits generation

Figure depicts the simulation result of the E2 frame degenerator module. This figure illustrates the functional validation of E2 defame FAS detection.

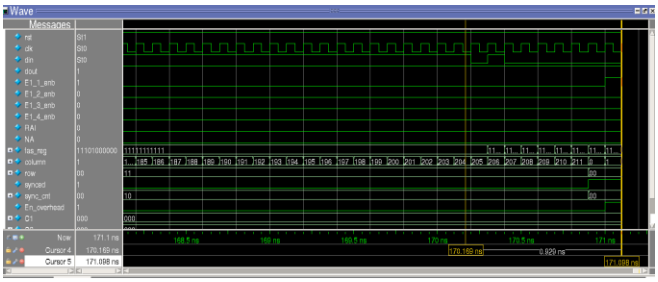

Figure 5.4: E2 deframe FAS bits generation

Figure depicts the simulation result of the E2 frame degenerator module. This figure illustrates the functional validation of E2 deframe sync generation.

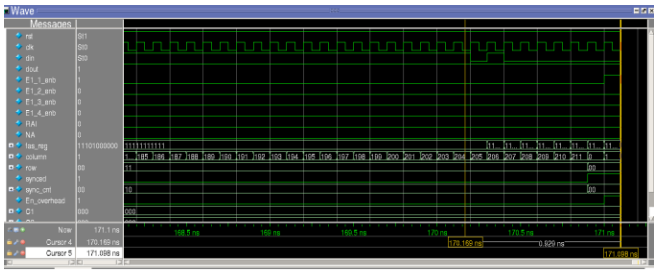

Figure 5.5: E2 deframe SYNC bit generation

Synthesis result of E2 Frame and Deframe

S.NO	Parameters	
1	FPGA Family	Cyclone IV E
2	Device	EP4CE22F17C8
3	Total Logic elements	668
4	Dedicated combinational elements	477
5	Dedicated combinational elements	485
6	Total Pins	21
7	Total memory bits	512
8	Total PLL's	1

Figure 5.6: synthesis report

6. Conclusions

This paper presents the E1 to E2 Framer and Deframer, with basic Frame length of 848 bits. Each Frame is transmitted at 100usec. The Frame is mapped in a bit interleaved fashion, into a higher rate signal and damped into a small rate signal. This soft core offers high data rate and also provides a faster and lower cost solution.

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