The design of Fig. 5 requires 16 transistors to implement the circuit (without considering the inverters which will be discussed later). Since complementary inputs are fed to the circuit of Fig. 5, it is better to follow the same strategy to implement the majority function; instead of using an inverter at the output node. Thus, the inverter can be omitted from the last stage of the circuit. The equation (6) and (7) Boolean expressions for *sum* may be rearranged as:

$$Sum = a.b.c + a.\bar{b}.\bar{c} + \bar{a}.b.\bar{c} + \bar{a}.\bar{b}.c \quad (15)$$

$$Carry = a.b.c + a.b.\bar{c} + a.\bar{b}.c + \bar{a}.b.c \quad (16)$$

Fig. 6 shows the implementation using the above idea. As seen, this circuit uses two bridge transistors like previous design. A complete fast full adder can be built by placing the sum circuit of Fig. 5 and the carry generator of Fig. 6 together as a whole circuit (according to the simulation results in section IV). The circuit requires 16 transistors to generate the sum signal, 10 transistors to produce the carry signal and 6 for complementary inputs, resulting in a device count of 32.

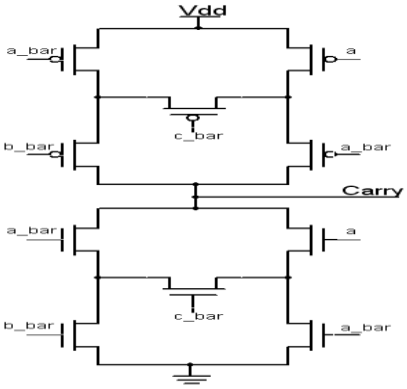

Figure 6: Carry generator circuits (Three Inputs Majority Function).

In consequence, it uses 4 transistors more than conventional CMOS adder. The increase in transistor count, in addition to some other reasons such as using more inverters, causes more power consumption of the considered design as compared to conventional CMOS adder (with respect to simulation results). However, the improvement in speed over conventional CMOS adder is eminent and drastically leads to a better power-delay product. The simulation results are presented in the next section. We have also considered some other adder cells either in voltage or current mode, but conventional CMOS adder is chosen for being analogous to our proposed adder.

6. Simulation Results

We have performed simulations using HSPICE in a 90 nanometer (*nm*) standard CMOS technology at room temperature; with supply voltage ranges from 0.65v to 1.5v with 0.05v steps. The simulation structure used is shown in Fig. 7. Data analysis of the carry and sum signals has been performed by Cosmos scope software. Also, the average power consumption of the simulated circuits is calculated by the expression (1).

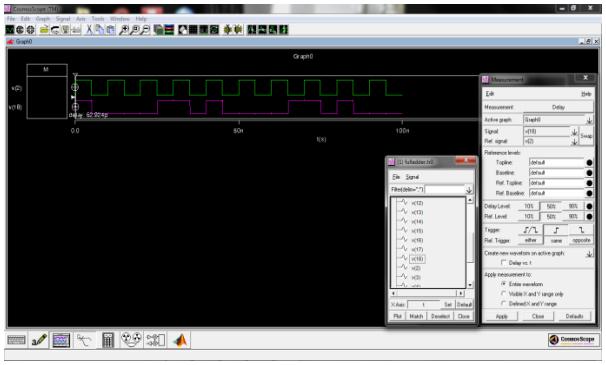

Figure 8: Delay calculation of Proposed Full adder design in 180nm technology.

Figure 9: Delay calculation of Proposed Full adder design in 90nm technology.

Power Consumption Results For Different Technologies

Figure Name	180nm	90nm
Conventional cmos full adder	4.9540uw	2.2242uw
Bridge implemention of majority function(fully symmetric style)	6.5150uw	2.8105uw
Bridge implemention of majority function(semi symmetric style)	2.0202uw	1.3987uw
Carry generator(majority function) circuit	2.7035uw	1.2072uw
Three inputs XOR(sum function)circuit	6.9344uw	3.002uw
Carry generator circuit(Three inputs majority function)	5.3267uw	2.3102uw

Power delay results for different technologies

Figure Name	180nm	90nm
Conventional cmos full adder	62.924ps	39.83ps
Bridge implemention of majority function(fully symmetric style)	102.71ps	57.989ps
Bridge implemention of majority function(semi symmetric style)	75.468ps	38.671ps
Carry generator(majority function) circuit	61.131ps	34.956ps
Three inputs XOR(sum function)circuit	123.09ps	68.697ps
Carry generator circuit(Three inputs majority function)	83.248ps	46.686ps

7. Conclusion

In this paper a novel design methodology, entitled bridge style, for CMOS full adder, is presented, and afterwards a new 1-bit adder is proposed based on the idea of bridge and compared to its conventional CMOS contender. Our new design style uses some transistors, called bridge transistors, sharing transistors of different paths to generate new paths from supply lines to circuit outputs. The suggested bridge adder shows better performance in delay as compared to conventional CMOS adder. According to HSPICE simulation in 90 *nm* and 180nm CMOS process technology at room temperature, and under given conditions, an improvement of 41.5% (@ Vdd=0.65 volt) to 0.37% (@ Vdd=1.5 volt) in speed over conventional CMOS adder is achieved. In addition, the suggested adder shows 13.8% (@ Vdd=0.65 volt) to 31.5% (@ Vdd=1.5 volt) degradation in terms of power consumption than conventional CMOS design.

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