













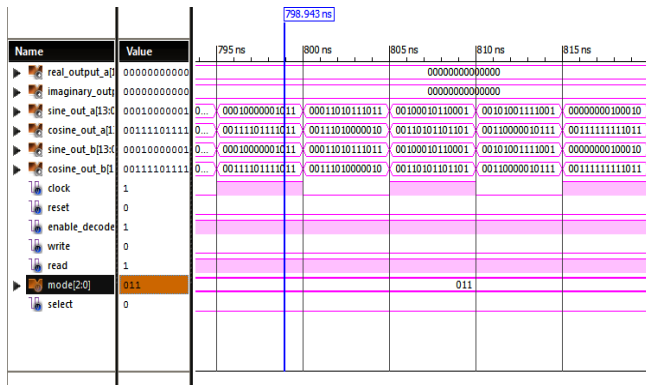




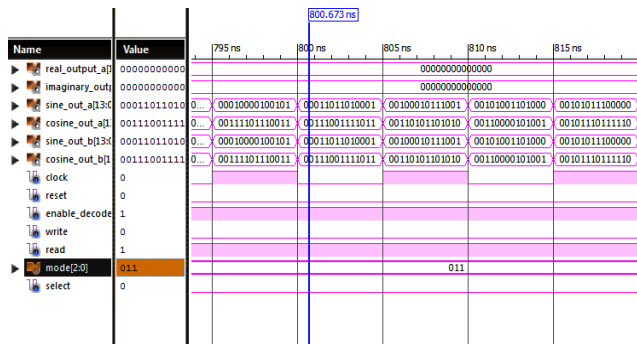


select input is used for selecting addition /subtract operation.

Simulation results of 8-microrotation CORDIC unit is shown in Figure 10 and corresponding optimized 4-microrotation CORDIC is shown in Figure 11.



**Figure 10:** Stimulation result of 8-microrotation CORDIC unit



**Figure 11:** Stimulation result of optimized 4-microrotation CORDIC unit

Comparison of Area utilization in terms of number of slice LUTs and total processing time of 8-microrotation CORDIC and optimized 4-microrotation CORDIC in programmable MIMO Decoder Architecture by synthesize the design in Virtex 5 xc5v1x110T is shown in TABLE IV.

**Table IV:** Comparison of 8-microrotation CORDIC unit and optimized 4-microrotation CORDIC in programmable MIMO Decoder Architecture

Architecture	Number of slices	Processing time (ns)
8-micro rotation CORDIC unit	2759	43.614
Optimized 4-micro rotation CORDIC unit	1389	33.947

## 7. Conclusion

MIMO OFDM plays an important role in most of the emerging wireless communication technologies. This work proposes a programmable MIMO decoder architecture with reduced area and processing time by reducing the micro rotation of the CORDIC rotation unit in existing MIMO decoder architecture. Here an optimization scheme has been used for micro rotation and scaling in to the CORDIC unit in the programmable MIMO decoder architecture. The proposed method adaptively select the appropriate iteration steps and converges to the final results by executing only four micro rotation as compared with increased number of rotations in the conventional CORDIC. The proposed algorithm perform all the angle of rotation within the range of  $0^0$  to  $45^0$  by angle folding method and which results in a pre-computation of micro rotations for all the rotation angles in the range  $0^0$  to  $45^0$ . This has eliminated the need for micro rotation calculation steps in the conventional CORDIC and thus entire processing time for rotation operation is reduced. Also, optimization scheme used in this work has reduced chip area requirement for the MIMO decoder, which in turn results in the reduction of power consumption.

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