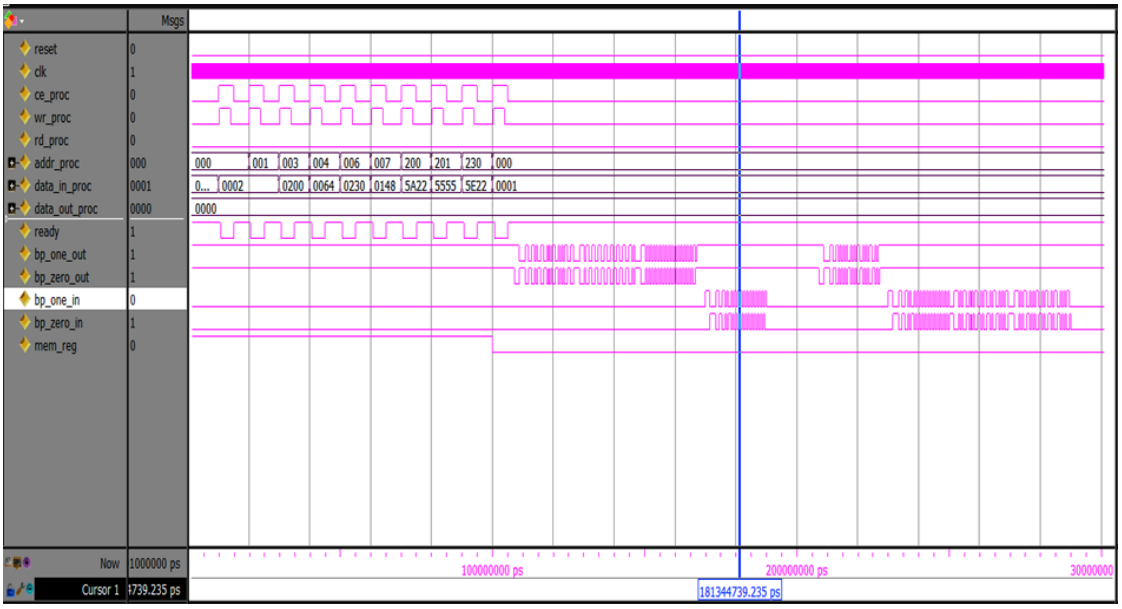

Figure 8: Simulated waveform of 1553B bus controller

5. Results

A finite state machine which designed the enhanced throughput message activity in a 1553B based bus controller have been presented. The designed state machine has been simulated using ModelSim and obtained waveform is shown in Figure 8 below.

The proposed system works as a bus controller which controls the data transfer through the bus. For BC to RT transfer a command word followed by data word is send by the BC. Upon receiving this, RT sends SW indicating an error free reception. The RT to BC transfer includes a command word which is send by the BC and upon receiving this CW, RT sends status word followed by the data word. The designed system is implemented on an Spartan 3 FPGA kit. From the device utilization obtained, it is clear that the area of utilization for the entire system is less.

Logic Utilization	Used	Available	Utilization
Total number of slice registers	16,621	66,560	24%
Number of 4 input LUTs	11,273	66,560	16%
Logic Distribution			
Number of coupled slices	13,928	33,280	41%
Total number of 4 input LUTs	11,281	66,560	16%
Number of bonded IOBs	53	633	8%
Number of GCLKs	2	8	25%

Figure 9: Device Utilization of proposed 1553B bus controller

6. Conclusion & Future Works

This thesis describes a MIL-STD-1553B serial data bus interface and the bus protocol controller VHDL simulation. The 1553B bus protocol controller which helps in controlling the data transmission through the bus. In the proposed system, 1553B bus controller is modelled as a finite state machine in VHDL. With the addition of an arbitrator, processor interface, memory block and protocol controller, the performance of the entire system was improved. The proposed system is implemented on an FPGA kit. For future work its data transferring rate could be improved to a great extent.

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