2.2 MSIC-TPG for Test per Scan schemes

The MSIC-TPG for test-per-scan schemes is illustrated in Figure 4. Tests per scan scheme consist of scan chains, test pattern generator, CUT, Look Up Table (LUT) block. The seed generator circuit produces unique seed vector by clocking the circuit. The reconfigurable Johnson counter is operated in all the three modes to generate every possible unique Johnson codeword. After XOR operation between seed vector and Johnson codeword, single bit change vectors are generated. These test vectors are given to CUT which should produce the expected outcome, which is stored in the LUT and to the scan chain blocks. The output of circuit under test is given to the look up table which compact the expected output of the circuit under test. The LUT makes a comparison of test response of CUT with the stored responses and decides whether the circuit is faulty or not.

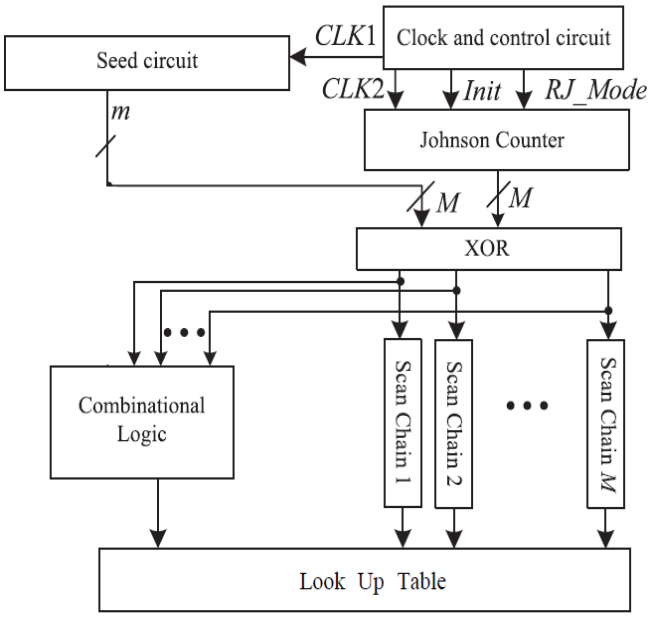


Figure 4: MSIC-TPGs for test-per-scan scheme

The test procedure for the test per scan scheme is as follows:

1) The seed circuit generates a new seed by clocking CLK1 one time.
2) *RJ_Mode* is set to "0". The reconfigurable Johnson counter will operate in the Johnson counter mode and generate a Johnson vector by clocking CLK2 one time.
3) After a new Johnson vector is generated, *Init* and *RJ_Mode* are set to 1. Now the reconfigurable Johnson counter operates as a circular shift register, and generates l codewords by clocking CLK2 l times. Then, a capture operation is inserted.
4) Repeat above two steps until $2l$ Johnson vectors are generated.
5) Repeat the above steps until the expected fault coverage or test length is achieved.

The main objective of the test pattern generator designed to produce single input change vector is to reduce the switching activity. Another requirement is that the MSIC sequence should not contain any repeated test patterns, because repeated patterns could prolong the test time and reduce test efficiency [8].

3. Verification of Circuit under Test

The verification of the circuit under test is done with the test per scan technique. From the scan chains produced from the test per scan method, one of the scan chain is considered as the input to the circuit under test. For testing the circuit, the test patterns generated from the Multiple single input change test pattern generator is applied as the input to the CUT. The MSIC sequence generated have the favorable features of uniform distribution and low input transition density. If the produced test patterns of MSIC TPG gives the expected output of the circuit under test without any error, a conclusion can be made that the test pattern generation in Built In Self Testing is sound. Reducing the switching activity between the test patterns can reduce the faults in the circuit under test to a great extend by eliminating errors like stuck at faults. MSIC test patterns are single input change vectors that have only single bit transition between test patterns.

A combinational circuit is used as the circuit under test. After applying the test patterns from the Multiple Single Input Change to the circuit under test (CUT), the verification of the CUT can be done in two ways. First is by using a reversible technique in the circuit under test. Another method is by using a Look Up Table (LUT) method. A typical LUT works as a comparator with stored responses and analyses the test responses to determine the correctness of the CUT.

3.1 Reversible Technique

To validate the CUT, the test patterns generated by MSIC test pattern generator is applied to the circuit under test. The circuit under test can be either combinational, sequential or a combination of both. A combinational circuit is used in this work. XOR gates are used in the combinational circuit because XOR gates possess reversible property. The XOR gate produces the same input as output, if the output of an XOR operation is XORed with any one of the input applied.

The circuit under test (CUT) considered must be reversible in nature for the verification of the CUT using reversible technique. The test patterns applied to the CUT produces corresponding test responses. The response of the reverse circuit of CUT obtained by inputting the test response of CUT should generate the same pattern that is applied to the circuit under test. If this happens, a conclusion can be made that the test response produced by the CUT with MSIC patterns that has minimum transitions given as input is accurate. Figure 5 gives the idea of reversible technique used in this work. Thus we can minimize the error in the CUT by applying the MSIC patterns generated from the MSIC test pattern generator.

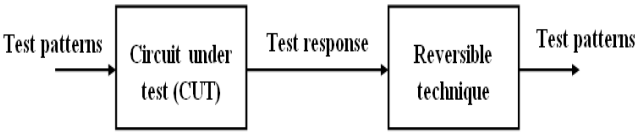


Figure 5: Reversible technique

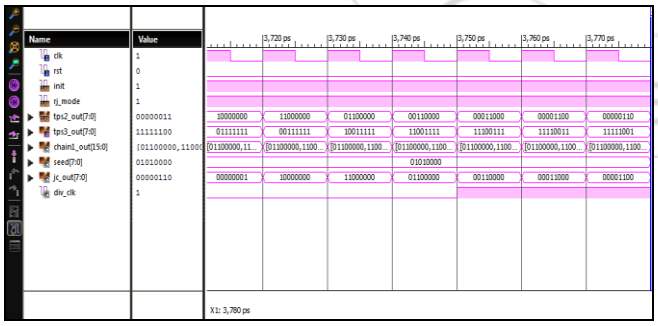
3.2 Look Up Table Method

Look up tables may be pre-calculated and stored in static program storage or stored in hardware for application specific platforms. A combinational circuit is used as circuit under test and output response of the CUT is stored in Look Up Table (LUT) for error comparison. Test responses are obtained after applying the test patterns from the MSIC test pattern generator to the circuit under test. Based on the circuit, output values are stored in the LUT corresponding to the inputs. LUT method compares the test response of the circuit under test and the data stored in the look up table.A typical LUT works as a comparator with stored responses and analyses the test responses to determine the correctness of the CUT. Fault is detected by verifying the output of the circuit under test and output of Look up Table. Test patterns are applied simultaneously to both CUT (XOR gate circuit) and LUT. The output from the circuit under test will be verified by comparing the output of LUT

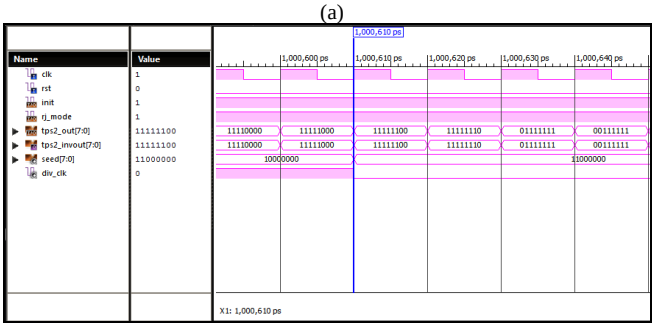
4. Results

In this section all the simulation results of test pattern generation and verification of test patterns are shown. The performance simulations of MSIC TPG along with CUT testing are carried out with Xilinx 13.2.The simulated output for the proposed MSIC test pattern generator shown in Figure6 (a). The verification of test patterns in the circuit under test is shown in Figure 6(b) and Figure 6(c).

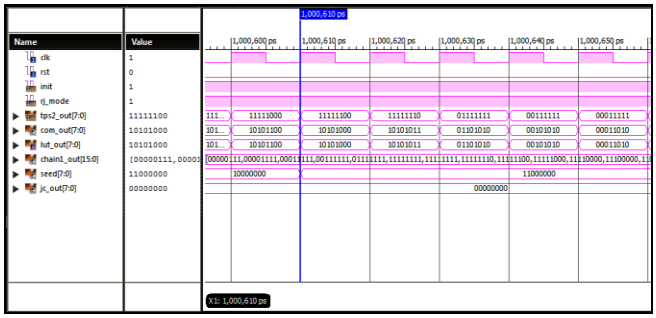
The reversible technique and the LUT methods are used for the validation of the CUT. These techniques are implemented on Sparton 3 kit. The reversible technique for testing will take more time duration of 10.049 ns for the verification of the circuit under test. The LUT method which initially stores the circuit under tests inputs and corresponding outputs values, compares the test response with the output of CUT. Therefore it takes only less time as compared to the reversible technique. The delay is 7.343 ns.



(a)



(b)



(c)

Figure 6: Simulation result of (a)Test per scan (b) reversible technique (c) look up table method

A comparison is done between these two techniques in terms of delay and area is shown in Table 1.

Table 1: Comparison of verification techniques

Validation method	*Delay (in ns)*	*Device utilization*
Reverse technique	10.049	57 out of 1920
LUT method	7.343	96 out of 1920

The LUT method since it stores all the input and output values of the circuit under test, the area covered by it is high. This again increases the size of circuit. The device utilization of LUT method in terms of number of slices is about 5%. The reversible technique unlike LUT method uses only the reverse circuit of the CUT and hence covers less area. The device utilization is nearly 2%

In VLSI testing speed and size are the two major factors that affect the circuit's performance. The LUT method that stores pre-calculated value reduces testing time, even if it covers larger area. Therefore, in application where area is not a major concern, LUT method can be used. In case of compact devices, where area is considered LUT method of testing is not used.

5. Conclusions

This paper is based on low-power test pattern generation method. Simulation results showed that an MSIC sequence had the favorable features of minimum transitions and uniform distribution of patterns. A flexible test per scan is developed with the combination of Reconfigurable Johnson counter and seed generator. The MSIC sequence produced by the MSIC test pattern generator may contain repeated test patterns but switching activity which results in error is reduced. Thus the system improves the test efficiency. This method also reduces the power consumption during testing mode with minimum number of switching activities between test patterns. After generating the MSIC patterns, the validation process is conducted on the combinational logic circuit and the output is verified via two techniques, the reversible technique and the LUT technique. From the comparison between these two techniques, a conclusion can be made that, in application where area is not a major concern, LUT method can be used. In case of compact devices, where area is considered LUT method of testing is not used.

References

[1] M. Nourani, M. Tehranipoor, and N. Ahmed, "Low-transition test pattern generation for BIST-based applications," *IEEE Trans. Comput.*, vol. 57, no. 3, pp. 303–315, Mar. 2008.
[2] F. Corno, M. Rebaudengo, M. Reorda, and M. Violante, "A new BIST architecture for low power circuits," in *Proc. Eur. Test Workshop*, May 1999, pp. 160–164.
[3] Y. Zorian, "A distributed BIST control scheme for complex VLSI devices," in *11th Annu. IEEE VLSI Test Symp. Dig. Papers*, Apr. 1993, pp. 4–9.
[4] P. Girard, "Survey of low-power testing of VLSI circuits," *IEEE Design Test Comput.*, vol. 19, no. 3, pp. 80–90, May–Jun. 2002.
[5] A. Abu-Issa and S. Quigley, "Bit-swapping LFSR and scan-chain ordering: A novel technique for peak- and average-power reduction in scan-based BIST," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 28, no. 5, pp. 755–759, May 2009.
[6] Prathyusha Nayineni, S.K. Masthan Jayamukhi. "Power optimization of BIST circuit using low power LFSR", International Journal of Computer Trends and Technology- volume 2 Issue2- 2011
[7] F. Liang, L. Zhang, S. Lei, G. Zhang, K. Gao, and B. Liang, "Test Patterns of Multiple SIC Vectors: Theory and Application in BIST Schemes" *IEEE Trans. on very large Scale integration (vlsi) systems*, vol. 21, no.4, April 2013.
[8] S. Wang and S. Gupta, "DS-LFSR: A BIST TPG for low switching activity," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 21, no. 7, pp. 842–851, Jul. 2002.
[9] Praveenkumar.J,Danesh.K, " Multiple Single Input Change Vectors for Built-In Self Test (MSIC-BIST)" *International Journal of Computational Engineering Research, Vol, 04, Issue, 2*Issn 2250-3005 , February 2014

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