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Circuit under Test Verification with MSIC Test Pattern Generator

Parvathy Chandra[1], Vishnu V. S.[2]

[1] PG Scholar, Embedded Systems, Sree Buddha College of Engineering, Kerala, India

[2] Assistant Professor, Dept.of Electronics and Communication, Sree Buddha College of Engineering, Kerala, India

Abstract: ***Improvement in quality and reliability are required for digital circuits as their complexity and density increases. Validation of VLSI circuits becomes more difficult with higher test cost. Built-In-Self-Test (BIST) techniques can effectively reduce complexity of VLSI testing, by the introduction of on-chip test hardware into the Circuit Under Test (CUT). In BIST architectures, the Test Pattern Generator (TPG) uses Linear Feedback Shift Register (LFSR) which generates pseudo random patterns that increases the switching activity of test patterns. The test pattern generator generates a multiple single input change (MSIC) vector which increases the accuracy of test response. The Single Input Change (SIC) vector generator uses a reconfigurable Johnson counter to generate minimum transition sequences. The TPG is used in test-per-scan scheme. A combinational circuit is used as the circuit under test, and the output response of CUT is stored in Look Up Table (LUT) for error comparison in LUT method of verification. Reversible technique is also used for the testing the circuit under test. The system is simulated using Xilinx 13.2 design suite.***

Keywords: BIST, CUT, LFSR, MSIC

1. Introduction

To eliminate the various defects caused by the manufacturing process, System on Chip (SoC) circuits depends on testing. Testing is the indigenous phase which attribute towards the successful implementation of any device. Importance of testing in Integrated Circuit is to improve the quality in chip functionality that is applicable for both commercially and privately produced products.

In Today's IC, as designs become more complicated Built In Self Test (BIST) has become progressively important. In order to test any circuit or device we require separate testing technique which should be done automatically. A BIST is used for this purpose. Built in self test techniques can effectively reduce the difficulty and complexity of VLSI testing. Thus BIST has become one of the major test techniques for today's large scale and high speed designs.

BIST is a Design For Test (DFT) methodology that aims at detecting faulty components in a system by introducing the test logic into the chip [1]. BIST is better known for its numerous advantages such as at-speed testing and reduced need for expensive external Automatic Test Equipment (ATE). The steps in a typical BIST approach are:

1) On-chip generation of test pattern.
2) Application of the test patterns to the circuit under test.
3) Analysis of circuit under test responses with on-chip output response analyzer (ORA)
4) Making decision whether the chip is faulty or not.

An efficient Test Pattern Generator (TPG) design is related to on-chip test pattern generation and it is an important subject in built in self test schemes. The basic BIST architecture shown in Figure1 consists of a test pattern generator (TPG), circuit under test (CUT) and an output response analyzer (ORA) also called as Output Data Analyzer (ODA) [2].Test patterns for the circuit under test are generated by the test pattern generator. A typical response analyzer is a comparator that compact stored responses of all possible inputs and analyzes the test responses to determine correctness of the circuit under test.

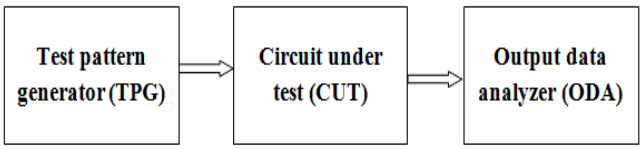


Figure 1: Basic BIST Architecture.

In conventional BIST architectures, the Linear Feedback Shift Register (LFSR) is commonly used in the test pattern generators due to simplicity and effectiveness of the LFSRs. A major drawback of these architectures is that the pseudorandom patterns generated by the LFSR lead to significantly high switching activities in the circuit under test [3], which can cause excessive power dissipation in the circuit under test. They also can damage the circuit and reduce the product yield and lifetime of CUT [4], [5]. The random nature of patterns generated by an LFSR significantly reduces the correlation not only among the patterns but also among the adjacent bits within each pattern. Therefore it is necessary that the patterns generated by the test pattern generator must have only minimum transitions.

Low correlation that exists between the consecutive test vectors increases switching activity and eventually power dissipation in the circuit during the test mode. The same happens when applying low correlated patterns to scan chains. The increasing switching activity in scan chain results in increasing power consumption [2] in scan chain and its combinational block. Several problems [1] are caused due to this extra power such as formation of hot spots, instantaneous power surge that causes circuit damage, difficulty in performance verification and reduction of the product yield and lifetime. By controlling the switching activity in the test

patterns, the power dissipation during testing can be reduced. Optimizing the power during testing [6] is an important aspect. Power reduction using the switching activity doesn't degrade the performance of the circuit rather it increases the accuracy. Several faults due to increased switching activity of the test patterns such as stuck at faults, bridging faults, etc. can be reduced and thus the accuracy of the test response can be improved.

The TPG can be modified by adding a Johnson counter (also called twisted ring counter) to the LFSR. This technique decreases the switching activity of the circuit under test and increases the fault coverage and generates the Multiple Single Input Change (MSIC) vectors for the test pattern generator. MSIC test pattern generator generates a minimum transition sequence that is; it generates test patterns with change only in single bit position. The switching activity in the circuit under test and the scan chains and, eventually, their power consumption are reduced by increasing the correlation between patterns and also within each pattern in the generated scan chain.

The rest of this paper is organized as follows. In Section 2, the MSIC-TPG scheme is presented. The verification of the circuit under test is described in Section 3. In Section 4, the simulations result of test per scan is provided to demonstrate the performance of the MSIC-TPGs. The simulation result of two techniques for the verification of circuit under test is also included in this chapter. Conclusions are given in Section 5.

2. MSIC Test Pattern Generator

Multiple Single Input Change (MSIC) is a test pattern generator (TPG) method that can change a Single Input Change (SIC) vector to exclusive low transition vectors for multiple scan chains [7],[9]. The first step in this process is to decompress the SIC vector to its multiple code words and the generated code words will bit-XOR with a same seed vector in turn. Hence, a test pattern with similar test vectors will be applied to all scan chains. The MSIC TPG consists of an SIC generator, a seed generator, an XOR gate network, and a clock and control block.

2.1 Test Pattern Generation Method

Consider *m* primary inputs (PIs) and *M* scan chains in a full scan design, and each scan chain has *l* scan cells. Figure 2 shows the symbolic representation for one generated pattern. The generated vector of an *m*-bit LFSR with the primitive polynomial can be expressed as $S(t) = S_0(t)S_1(t)S_2(t), \ldots, S_{m-1}(t)$ (hereinafter referred to as the seed), and the vector generated by an *l*-bit Johnson counter can be expressed as $J(t) = J_0(t)J_1(t)J_2(t), \ldots, J_{l-1}(t)$. In the first clock cycle, $J = J_0\ J_1\ J_2, \ldots, J_{l-1}$ will bit-XOR with $S = S_0S_1S_2, \ldots, S_{M-1}$, and the results $X_1X_{l+1}X_{2l+1}, \ldots, X_{(M-1)l+1}$ will be shifted into *M* scan chains, respectively. In the second clock cycle, $J = J_0\ J_1\ J_2, \ldots, J_{l-1}$ will be circularly shifted as $J = J_{l-1}\ J_0\ J_1, \ldots, J_{l-2}$, which will also bit-XOR with the seed $S = S_0S_1S_2, \ldots, S_{M-1}$. The resulting $X_2X_{l+2}X_{2l+2}, \ldots, X_{(M-1)l+2}$ will be shifted into *M* scan chains, respectively. After *l* clocks, each scan chain will be fully loaded with a unique Johnson codeword, and seed $S_0S_1S_2, \ldots, S_{m-1}$ will be applied to *m* PIs.

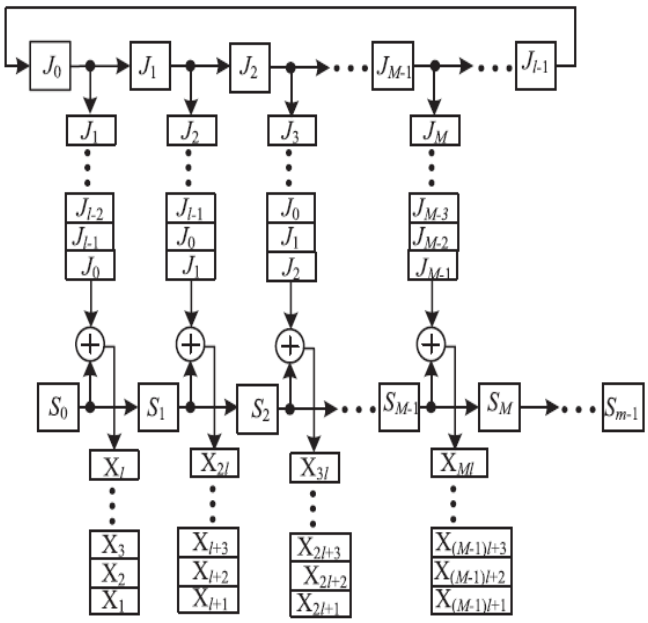


Figure 2: Symbolic representation of an MSIC pattern [7].

There are two kinds of SIC generators based on the different scenarios of scan length, to generate Johnson vectors and Johnson codewords, that is; the reconfigurable Johnson counter and the scalable SIC counter. For a short scan length, a reconfigurable Johnson counter is developed to generate an SIC sequence in time domain. An SIC counter named the "scalable SIC counter" is developed when the maximal scan chain length *l* is much larger than the scan chain number M. The SIC counter consist of subtractor, adder, chain of D flipflops and chain of muxes.

Reconfigurable Johnson Counter as shown in Figure 3 is preferably used when the scan length is less. The reconfigurable Johnson counter consists of a mux and an AND gate to make it operate in three different modes. The control signals for the reconfigurable Johnson counter are *Init* and *RJ_Mode*.

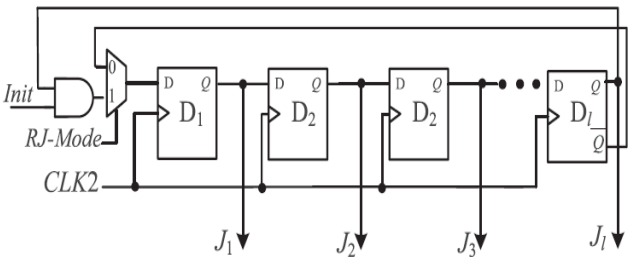


Figure 3: Reconfigurable Johnson counter[7]

The reconfigurable Johnson counter has three modes of operation. First is initialization mode (*Init* =0 and *RJ_Mode* =1), in which all flip flops are initialized. In normal mode(*Init* =0 and *RJ_Mode* =0) of operation, it acts as Johnson counter. The patterns generated in Johnson counter is circularly shifted in circular shift mode(*Init* =1 and *RJ_Mode* =1).

2.2 MSIC-TPG for Test per Scan schemes

The MSIC-TPG for test-per-scan schemes is illustrated in Figure 4. Tests per scan scheme consist of scan chains, test pattern generator, CUT, Look Up Table (LUT) block. The seed generator circuit produces unique seed vector by clocking the circuit. The reconfigurable Johnson counter is operated in all the three modes to generate every possible unique Johnson codeword. After XOR operation between seed vector and Johnson codeword, single bit change vectors are generated. These test vectors are given to CUT which should produce the expected outcome, which is stored in the LUT and to the scan chain blocks. The output of circuit under test is given to the look up table which compact the expected output of the circuit under test. The LUT makes a comparison of test response of CUT with the stored responses and decides whether the circuit is faulty or not.

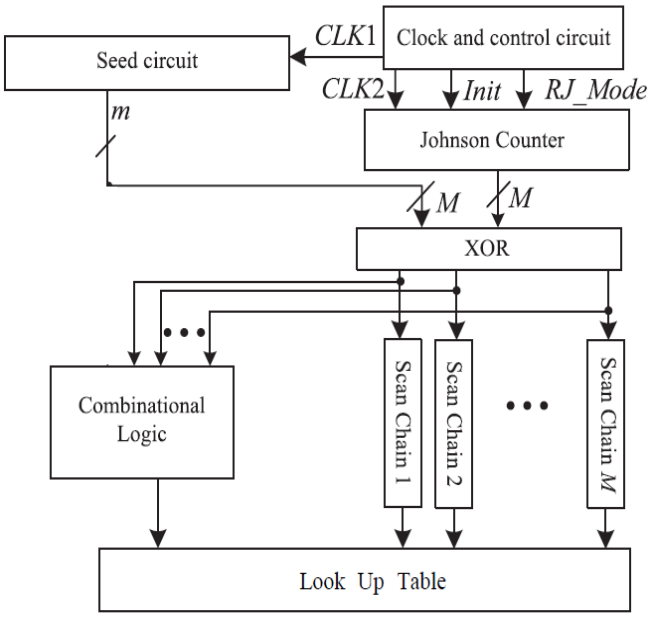


Figure 4: MSIC-TPGs for test-per-scan scheme

The test procedure for the test per scan scheme is as follows:

1) The seed circuit generates a new seed by clocking CLK1 one time.
2) *RJ_Mode* is set to "0". The reconfigurable Johnson counter will operate in the Johnson counter mode and generate a Johnson vector by clocking CLK2 one time.
3) After a new Johnson vector is generated, *Init* and *RJ_Mode* are set to 1. Now the reconfigurable Johnson counter operates as a circular shift register, and generates l codewords by clocking CLK2 l times. Then, a capture operation is inserted.
4) Repeat above two steps until $2l$ Johnson vectors are generated.
5) Repeat the above steps until the expected fault coverage or test length is achieved.

The main objective of the test pattern generator designed to produce single input change vector is to reduce the switching activity. Another requirement is that the MSIC sequence should not contain any repeated test patterns, because repeated patterns could prolong the test time and reduce test efficiency [8].

3. Verification of Circuit under Test

The verification of the circuit under test is done with the test per scan technique. From the scan chains produced from the test per scan method, one of the scan chain is considered as the input to the circuit under test. For testing the circuit, the test patterns generated from the Multiple single input change test pattern generator is applied as the input to the CUT. The MSIC sequence generated have the favorable features of uniform distribution and low input transition density. If the produced test patterns of MSIC TPG gives the expected output of the circuit under test without any error, a conclusion can be made that the test pattern generation in Built In Self Testing is sound. Reducing the switching activity between the test patterns can reduce the faults in the circuit under test to a great extend by eliminating errors like stuck at faults. MSIC test patterns are single input change vectors that have only single bit transition between test patterns.

A combinational circuit is used as the circuit under test. After applying the test patterns from the Multiple Single Input Change to the circuit under test (CUT), the verification of the CUT can be done in two ways. First is by using a reversible technique in the circuit under test. Another method is by using a Look Up Table (LUT) method. A typical LUT works as a comparator with stored responses and analyses the test responses to determine the correctness of the CUT.

3.1 Reversible Technique

To validate the CUT, the test patterns generated by MSIC test pattern generator is applied to the circuit under test. The circuit under test can be either combinational, sequential or a combination of both. A combinational circuit is used in this work. XOR gates are used in the combinational circuit because XOR gates possess reversible property. The XOR gate produces the same input as output, if the output of an XOR operation is XORed with any one of the input applied.

The circuit under test (CUT) considered must be reversible in nature for the verification of the CUT using reversible technique. The test patterns applied to the CUT produces corresponding test responses. The response of the reverse circuit of CUT obtained by inputting the test response of CUT should generate the same pattern that is applied to the circuit under test. If this happens, a conclusion can be made that the test response produced by the CUT with MSIC patterns that has minimum transitions given as input is accurate. Figure 5 gives the idea of reversible technique used in this work. Thus we can minimize the error in the CUT by applying the MSIC patterns generated from the MSIC test pattern generator.

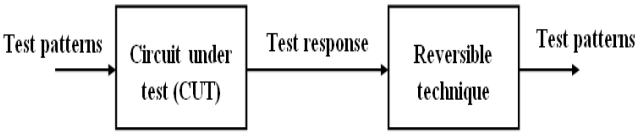


Figure 5: Reversible technique

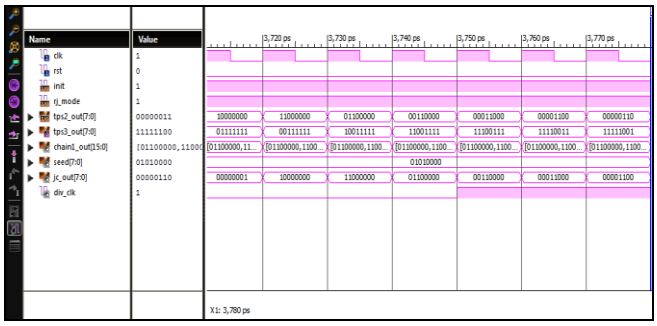
3.2 Look Up Table Method

Look up tables may be pre-calculated and stored in static program storage or stored in hardware for application specific platforms. A combinational circuit is used as circuit under test and output response of the CUT is stored in Look Up Table (LUT) for error comparison. Test responses are obtained after applying the test patterns from the MSIC test pattern generator to the circuit under test. Based on the circuit, output values are stored in the LUT corresponding to the inputs. LUT method compares the test response of the circuit under test and the data stored in the look up table.A typical LUT works as a comparator with stored responses and analyses the test responses to determine the correctness of the CUT. Fault is detected by verifying the output of the circuit under test and output of Look up Table. Test patterns are applied simultaneously to both CUT (XOR gate circuit) and LUT. The output from the circuit under test will be verified by comparing the output of LUT

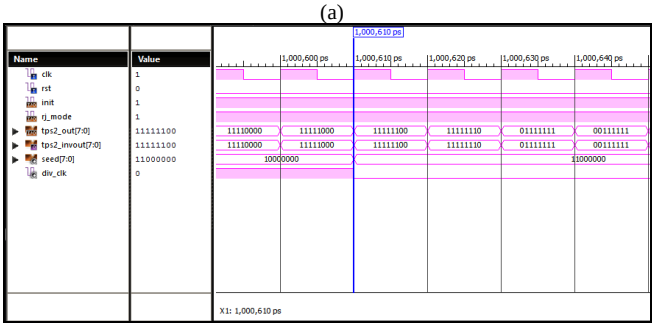
4. Results

In this section all the simulation results of test pattern generation and verification of test patterns are shown. The performance simulations of MSIC TPG along with CUT testing are carried out with Xilinx 13.2.The simulated output for the proposed MSIC test pattern generator shown in Figure6 (a). The verification of test patterns in the circuit under test is shown in Figure 6(b) and Figure 6(c).

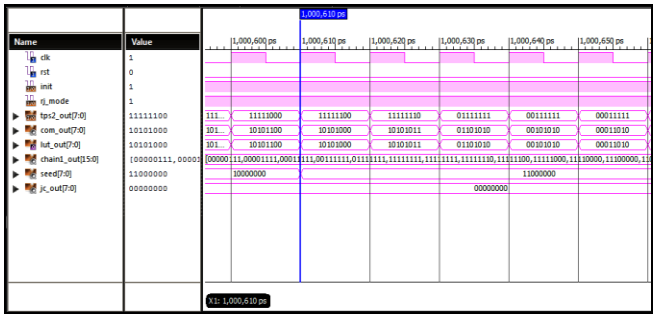
The reversible technique and the LUT methods are used for the validation of the CUT. These techniques are implemented on Sparton 3 kit. The reversible technique for testing will take more time duration of 10.049 ns for the verification of the circuit under test. The LUT method which initially stores the circuit under tests inputs and corresponding outputs values, compares the test response with the output of CUT. Therefore it takes only less time as compared to the reversible technique. The delay is 7.343 ns.



(a)



(b)



(c)

Figure 6: Simulation result of (a)Test per scan (b) reversible technique (c) look up table method

A comparison is done between these two techniques in terms of delay and area is shown in Table 1.

Table 1: Comparison of verification techniques

Validation method	*Delay (in ns)*	*Device utilization*
Reverse technique	10.049	57 out of 1920
LUT method	7.343	96 out of 1920

The LUT method since it stores all the input and output values of the circuit under test, the area covered by it is high. This again increases the size of circuit. The device utilization of LUT method in terms of number of slices is about 5%. The reversible technique unlike LUT method uses only the reverse circuit of the CUT and hence covers less area. The device utilization is nearly 2%

In VLSI testing speed and size are the two major factors that affect the circuit's performance. The LUT method that stores pre-calculated value reduces testing time, even if it covers larger area. Therefore, in application where area is not a major concern, LUT method can be used. In case of compact devices, where area is considered LUT method of testing is not used.

5. Conclusions

This paper is based on low-power test pattern generation method. Simulation results showed that an MSIC sequence had the favorable features of minimum transitions and uniform distribution of patterns. A flexible test per scan is developed with the combination of Reconfigurable Johnson counter and seed generator. The MSIC sequence produced by the MSIC test pattern generator may contain repeated test patterns but switching activity which results in error is reduced. Thus the system improves the test efficiency. This method also reduces the power consumption during testing mode with minimum number of switching activities between test patterns. After generating the MSIC patterns, the validation process is conducted on the combinational logic circuit and the output is verified via two techniques, the reversible technique and the LUT technique. From the comparison between these two techniques, a conclusion can be made that, in application where area is not a major concern, LUT method can be used. In case of compact devices, where area is considered LUT method of testing is not used.

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Author Profile

Parvathy Chandra. was born in Kerala, India in 1990. She is currently pursuing Master of Technology (M.-Tech) in Embedded systems in Sree Buddha College of Engineering, Alappuzha. She received her Bachelor of Technology (B.-Tech) degree in Electronics and Communication Engineering from CUSAT, India in 2012. Her areas of interest include Embedded system design, VLSI testing.

Vishnu V. S. was born in Kerala, India in 1986. He is presently working as Assistant Professor in the Dept of Electronics and Communication Engineering, Sree Buddha College of Engineering, Alappuzha and also doing part time Ph.D in Dept. of Electronics and Instrumentation in Noorul Islam University, Nagercoil. He received his B.-Tech degree in Electronics and Communication Engineering from Kerala University in 2007. He completed his Master of Engineering (M. E.) in Control and Instrumentation in 2010 from Anna University He has 1 year industrial experience in TATA Elxsi and teaching experience of about 6 years. His main areas of interest are control systems, process control, soft computing, mobile communications and embedded system design.