International Journal of Science and Research (IJSR)
ISSN (Online): 2319-7064
Index Copernicus Value (2013): 6.14 | Impact Factor (2013): 4.438

VHDL Implementation for Adaptive FIR filter and its Novel Application using Systolic Architecture

Ghanshyam A. Chune[1], Vijay Bagdi[2]

M.E.(WCC)Department, AGPCET Nagpur

Lecturer, AGPCET Nagpur

Abstract: ***The systolic architecture is an arrangement of processor where data flows synchronously across array element. To obtain perfect solution parallel computing is use in contradiction. The tremendous growth of computer and Internet technology wants a data to be process with a high speed and in a powerful manner. In such complex environment, the conventional methods of performing multiplications are not suitable to obtain the perfect solution. This paper demonstrates an effective design for adaptive filter using Systolic architecture for DLMS algorithm, synthesized and simulated on Xilinx ISE Project navigator tool in very high speed integrated circuit hardware description language and Field Programmable Gate Arrays (FPGAs). The DLMS adaptive algorithm minimizes approximately the mean square error by recursively altering the weight vector at each sampling instance. In order to obtain minimum mean square error and updated value of weight vector effectively, systolic architecture is used.***

Keywords: Systolic Architecture, DLMS algorithm, VHDL, FPGA, Xilinx ISE

1. Introduction

The Adaptive digital filters (ADFs) are widely used in various signal-processing applications, such as, echo cancellation, system identification, noise cancellation and channel equalization etc. Many of these applications require real-time adaptive filtering to implement the necessary functionalities with desired quality. For such applications the ADFs are therefore realized through dedicated VLSI systems. Amongst the existing ADFs least mean square (LMS)-based finite impulse response (FIR) adaptive filter is the most popular one due to its inherent simplicity and satisfactory convergence performance. As the delay in availability of the feedback error for updating the weights according to the LMS algorithm does not favors its pipeline implementation under high sampling rate condition. For that purpose the delayed LMS (DLMS) algorithm for pipeline implementation of LMS.

1.1 Systolic Architecture

In the computer architecture, the systolic architecture is a pipelined network arrangement of Processing Elements (PEs) called cells. Systolic architecture represent a network a processing element (PEs) that rhythmically compute and pass data through the stem, the PEs regularly pump data in an out such that regular flow of data is maintained, as a result systolic array feature modularity and regularity which are important property for VLSI design. The systolic array may be use as a coprocessor in combination of host computer pass through PEs and the final result is return to host computer as shown in figure of systolic system.

In order to achieve the high speed and low power demand in ASP applications, parallel array multipliers are widely used. In DSP applications, most of the power is consumed by the multipliers. Hence, low power multipliers must be designed in order to reduce the power dissipation.

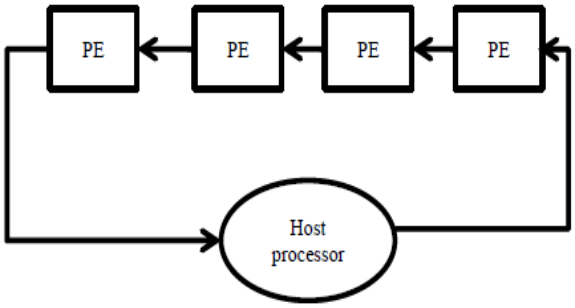

Figure 1.1: Basic Principle of systolic system

1.2 LMS (Least Mean Square) Algorithm

The LMS adaptive algorithm minimizes approximately the mean-square error by recursively altering the weight vector at each sampling instance. Thus an adaptive FIR digital filter driven by the LMS algorithm can be described in vector form as,

$$y(n)=WT(n)X(n)$$
$$e(n)=d(n)-y(n)$$
$$W(n+1)=W(n)+\mu e(n)X(n)$$

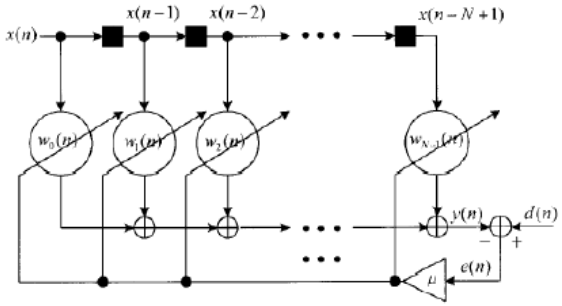

Figure 1.2: Block diagram of an adaptive FIR digital filter driven by LMS algorithm

Where $d(n)$ and $y(n)$denote the desired signal and output signal, respectively. The step-size μ is used for adaptation of the weight vector, and e(n) is the feedback error. In the above equations, the tap-weight vector $w(n)$ and the tap-input vector $x(n)$ are defined as.

$$W(n) = [w0(n), w1(n), \ldots, wn-1(n)]T$$
$$X(n) = [x(n), x(n-1), \ldots, x(n-N+1)]T$$

Where, *N* is the length of an FIR digital filter denotes the transpose operator. The block diagram of the LMS adaptive FIR digital filter is depicted in figure 1.2 here the symbol denotes the unit delay element. In this utilize the algebra for the design of a systolic-array implementation for adaptive filters based on the LMS algorithm. However, since the LMS algorithm contains a feedback loop, the delays created in the decomposition and retiming process prohibit the exact implementation of the algorithm. The design procedure leads to a systolic array which implements a special case of the so-called delayed LMS (DLMS) algorithm. The error ***e(n)*** used in this algorithm is available only after the processing delay of the systolic array, and thus, the update of the coefficients is performed with this delay.

1.3 DLMS (Delayed Least Mean Square) Algorithm

LMS algorithm uses the feedback-error corresponding to the *nth* iteration for updating the filter weights to be used for computing the filter output for the (*n*+1)Th iteration. The DLMS algorithm is similar to the LMS algorithm, except that in case of DLMS algorithm, the weight increment terms to be used in the current iteration are estimated from the error value and input samples corresponding to a past iteration. The weight update equation algorithm is given by,

$$W(n+1) = W(n) + \mu e(n-D)X(n-D)$$

here, *D* is the number of iterations by which the adaptation is delayed.

2. Related Work

1. One of the important implementation i.e. Conversion of the delayed LMS algorithm into the LMS algorithm. they shown in which way the delayed LMS (DLMS) algorithm can be transformed into the standard LMS algorithm at only slightly increased computational expense (R. D. Poltmann, 1995).

2. Another important implementation, An Efficient Systolic Architecture for the DLMS Adaptive Filter and Its Applications. In this paper an efficient systolic architecture for the delay least-mean-square (DLMS) adaptive finite impulse response (FIR), digital filter based on a new tree-systolic processing element (PE) and an optimized tree-level rule. It provide comprehensive comparison results for different -tap adaptive FIR filter structure and verify our systolic-array architecture of adaptive equalization and system identification applications (Lan-Da Van, Wu-Shiung Feng, 2001).

3. The another important implementation, VHDL Generation of Optimized FIR Filters, this paper a near optimum algorithm for constant coefficient FIR filters was used. This algorithm uses general coefficient representation for the optimal sharing of partial products in Multiple Constants Multiplications (MCM). The software implementation was developed in C language and produces VHDL code for the optimized FIR filter from a coefficient specification file. The developed software was applied to several FIR filters and compared to Matlab's Filter Design & Analysis (FDA). The FDA toolbox includes a feature to generate optimized VHDL code from the generated coefficients and was used to compare to the developed software (Fábio Fabian Daitx, Vagner S. Rosa, Eduardo Costa, Paulo Flores, Sérgio Bampi, 2008).

4. The another important implementation, A High-Speed FIR Adaptive Filter Architecture using a Modified Delayed LMS Algorithm. In this paper, a modified delayed least means square (DLMS) adaptive algorithm to achieve lower adaptation-delay. Authors proposed an efficient pipelined architecture for the implementation of this adaptive filter. They shown that the proposed DLMS adaptive filter can be implemented by a pipelined inner-product computation unit for calculation of feedback error, and a pipelined weight-update unit consisting of N parallel multiplies accumulators, for filter order N. They suggested a modified DLMS adaptive algorithm to achieve less adaptation-delay compared with the conventional DLMS algorithm, and shown that the proposed DLMS algorithm can be implemented efficiently by a pipelined inner product computation unit and parallel and pipelined weight update unit using carry-save reductions. Substantial reduction of adaptation-delay, ADP and EPS over the existing structures has been achieved by the proposed design (Pramod K. Meher, Megha Maheshwari, 2011).

5. Another important implementation, A New Pipelined Architecture for the DLMS Algorithm. This paper presents a design of a systolic array architecture for the 1-dimensional Finite Impulse Response adaptive filter. The design is based on the Delayed Least Mean Squares algorithm (DLMS). The performance of the proposed design is analyzed in terms of speed up, adaptation delay and throughput. The different N-tap 1 -D adaptive filters are analyzed and it is shown that the proposed scheme is superior in terms of adaptation delay, speed and throughput without the need for additional hardware (K.R.Santha, V Vaidehi, 2005).

6. Another important implementation, Efficient Systolic Architectures for l-D and 2-D DLMS Adaptive Digital. Two efficient ***N***th tap 1-D and window size *N* x *N* 2-D systolic adaptive digital filters utilizing the tree-systolic PE has been presented in this paper. Under considering maximum number of tap-connections of the feedback error signal, the practical rule to decide the optimized tree level without sacrificing the systolic characteristics is provided. At last, they verify I-D and 2-D efficient systolic architectures via applications of adaptive equalizer and image restoration (Lan-Da Van, Wu-Shiung Feng, 2000).

7. Another important implementation, A Systolic Architecture for LMS Adaptive Filtering with Minimal Adaptation Delay. This paper presents a systolic architecture with minimal adaptation delay and input/output latency, thereby improving the convergence behavior to near that of the original LMS algorithm. With the use of carry-save arithmetic, the systolic folded pipelined architecture can support very high sampling rates, Elimited only by the delay of a full adder (S. Ramanathan, V. Visvanathan, 1996).

8. Another important implementation, Delayed Block LMS Algorithm and concurrent architecture for high-speed implementation of Adaptive FIR Filter. In this paper, proposed the DBLMS algorithm which takes a block of *L* input samples and yields a block of *L* outputs in every training cycle. The simulation result shows that the performance of DBLMS algorithm is equivalent to that of the DLMS algorithm. However, the DBLMS algorithm offers *L* fold higher parallelism compared with the DLMS algorithm. We have utilized the inherent parallelism in DBLMS algorithm to derive a highly concurrent systolic-like architecture for high-speed implementation of adaptive FIR filter.

3. Proposed Work

The proposed work use Systolic Array architecture, which consist of no of processing element connected to one another, basic processing element of systolic architecture is as shown in figure 3.1.

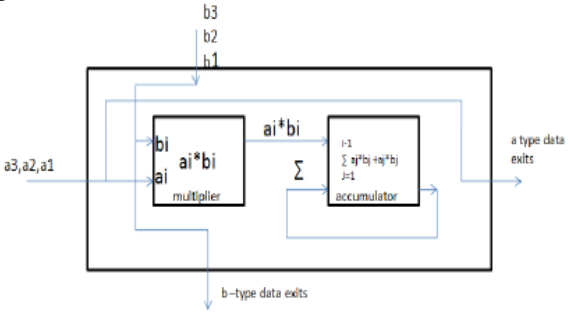

Figure 3.1: PE of systolic Architecture

Where A, B and C are the matrices with order m x k , k x n , and m x n respectively. Each PE of systolic array computes the multiplication of elements and accumulates to the corresponding element and then elements will be passed to neighbor PE in the systolic array.

First elements αi,j in row i of matrix A are injected first into PE as pipeline with the sequence αi,k of and the input time to the element of αi+1,j is one time unit later than αi,j . Similarly, elements bi,j in column j of matrix B are injected first into PE as pipeline with the sequence of bk,j and the input time to the element of the sequence of bk,j+1is one time unit later than of bk,j .

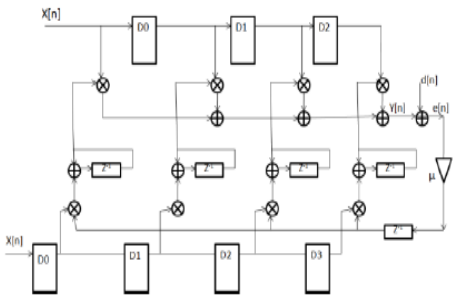

Figure 3.2: Direct form of DLMS adaptive FIR filter

The architecture of PE in this approach is shown in figure 3.1 which performs the Multiplication and Accumulation on data. Figure 3.2 shows the direct forms of DLMS FIR filters, which mainly consists of shift registers, adders and multipliers. The signal samples are multiplied by filter coefficients and are gathered together in the adder block. The DLMS FIR filter consists of some registers in feedback line. Figure 3.3 shows highly realizable systolic architecture of the DLMS adaptive digital filter.

Where z-1 denotes a unit delay, we insert a unit delay element in the feedback path so as to maintain the lowest critical period. And observe that when *p* is equal to zero, this architecture can be reduced to a fully pipelined architecture .On the other hand, if *p* is greater than zero, this architecture performs better convergence sacrificing systolic features.

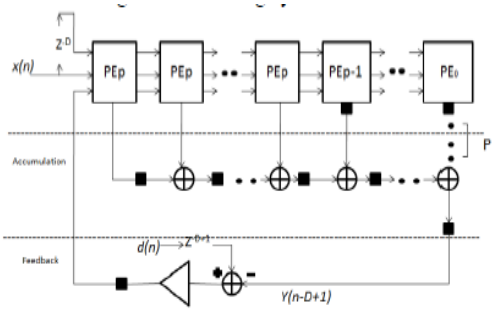

Figure 3.3: Systolic architecture with cascaded systolic-tree PEs.

The architecture for realization of Adaptive FIR filter using DLMS algorithm consist of no. of PE's connected to one another. No of PE's is equal to no of Taps of an FIR filter, Propose work design for 4-Tap Fir filter therefore no PE's equal to 4. If Taps of filter increase then no of PE's increase. This architecture is use for obtaining mean square error. This MSE is again use for obtaining updated value of weight coefficient and the procedure is continuous until we get minimum MSE. Shows different simulation result and find out time require for obtaining minimum MSE for different input, and desired output combination.

4. Simulation Result

The simulation results for realization of adaptive digital FIR filters using DLMS algorithm on FPGA chip are presented and the performances of DLMS algorithm is obtain in terms of chip area utilization and time require for minimum MSE.

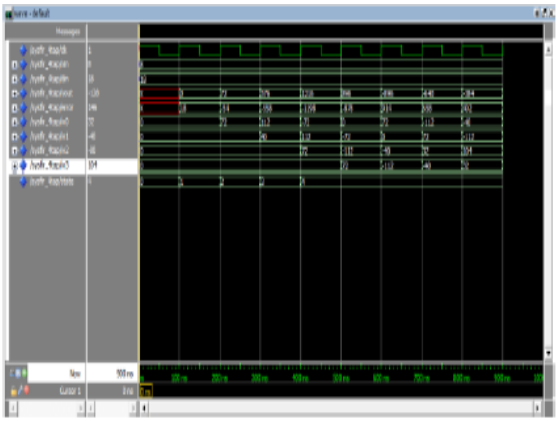

Figure 4.1: Simulation result for Xin=8 and Din=18

Figure 4.1 shows the Modelsim view of 32-tap adaptive FIR filter, code is written in VHDL language. Figure 4.2 shows simulation output waveform for 4-tap adaptive FIR filter.

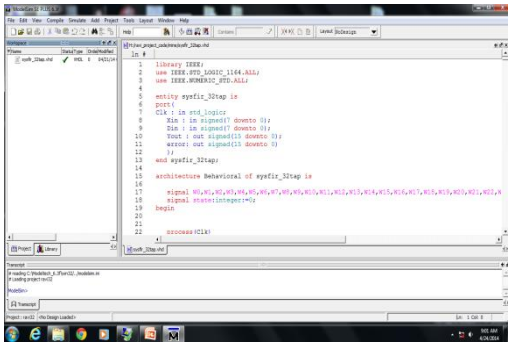

Figure 4.2: VHDL code for 32-tap FIR filter

The digital adaptive filters (DAF) were modeled by VHDL and implemented on Spartan 3 FPGA family. The Xilinx and model-sim software was used for synthesize and simulation of VHDL codes. Initially the filter weights w0, w1, w2, and w3 are assumed to be zero and obtain the updated value for reducing the error using the inputs information and error values. In these simulation results the learning factor was assumed to be μ=0.5. Simulation result for different input and desired output combination are as shown in figures.

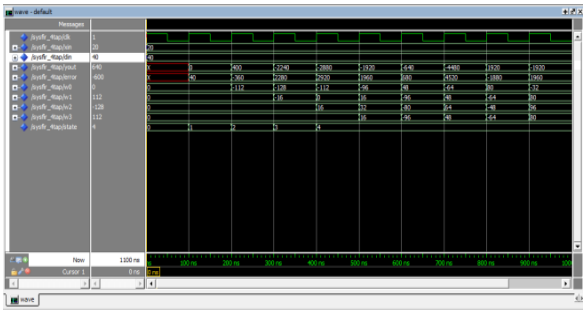

Figure 4.3: Simulation result for Xin=20 and Din=40

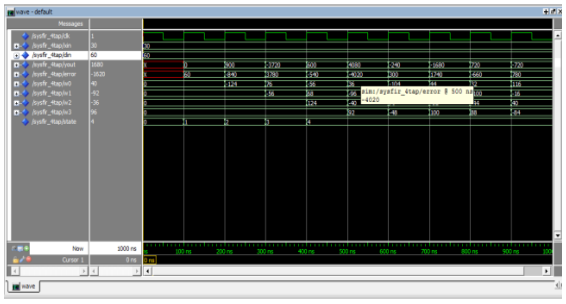

Figure 4.4: Simulation result for Xin=30 and Din=60

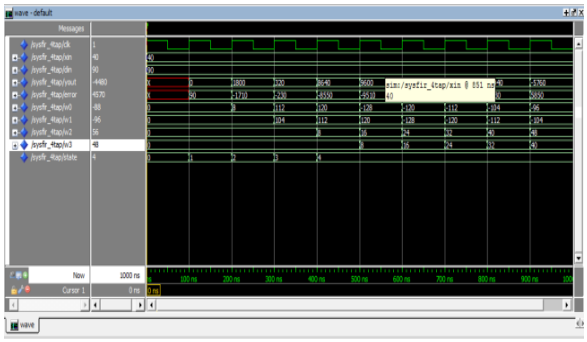

Figure 4.5: Simulation result for Xin=40 and Din=90

Synthesis result for adaptive FIR filter using Xilinx is as shown in table 4.1.

Table 4.1: Synthesis Result

Sr. no	Parameters	Utilization
1	No. of slices	179
2	Minimum period	19.408 ns
3	Power supply	0.060(W)

5. Conclusion

In this brief, We presented the modified proposed Adaptive FIR filter using Systolic Architecture. The key idea is to provide a involving the concept of pipelining and parallel processing into systolic architecture highly reduce adaption delay, chip area and power consumption. Design observes different adaption delay chip area and power consumption for different input and desired output combination. The proposed structure significantly involves less adaption delay chip area and power consumption as compared to the existing structures.

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Author Profile

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