Figure 4.1 shows the Modelsim view of 32-tap adaptive FIR filter, code is written in VHDL language. Figure 4.2 shows simulation output waveform for 4-tap adaptive FIR filter.

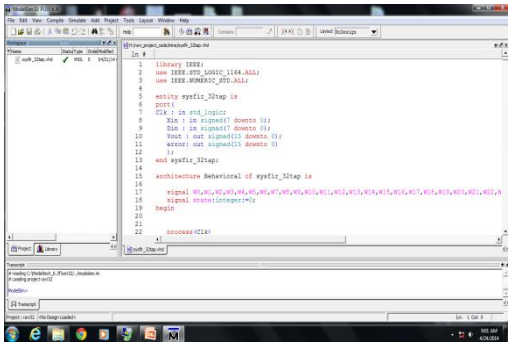

Figure 4.2: VHDL code for 32-tap FIR filter

The digital adaptive filters (DAF) were modeled by VHDL and implemented on Spartan 3 FPGA family. The Xilinx and model-sim software was used for synthesize and simulation of VHDL codes. Initially the filter weights w0, w1, w2, and w3 are assumed to be zero and obtain the updated value for reducing the error using the inputs information and error values. In these simulation results the learning factor was assumed to be μ=0.5. Simulation result for different input and desired output combination are as shown in figures.

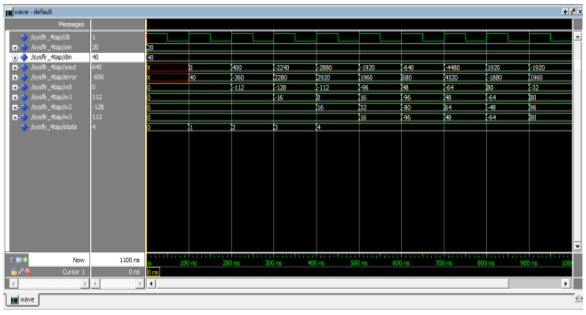

Figure 4.3: Simulation result for Xin=20 and Din=40

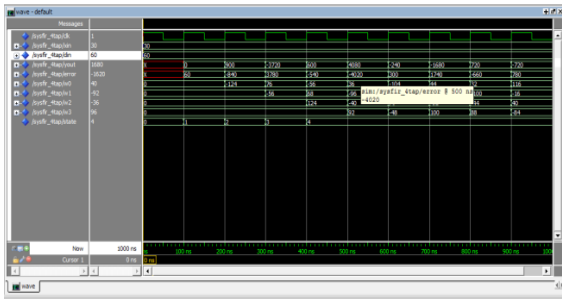

Figure 4.4: Simulation result for Xin=30 and Din=60

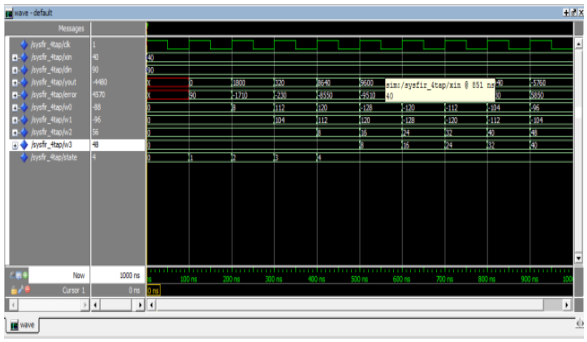

Figure 4.5: Simulation result for Xin=40 and Din=90

Synthesis result for adaptive FIR filter using Xilinx is as shown in table 4.1.

Table 4.1: Synthesis Result

Sr. no	Parameters	Utilization
1	No. of slices	179
2	Minimum period	19.408 ns
3	Power supply	0.060(W)

5. Conclusion

In this brief, We presented the modified proposed Adaptive FIR filter using Systolic Architecture. The key idea is to provide a involving the concept of pipelining and parallel processing into systolic architecture highly reduce adaption delay, chip area and power consumption. Design observes different adaption delay chip area and power consumption for different input and desired output combination. The proposed structure significantly involves less adaption delay chip area and power consumption as compared to the existing structures.

References

[1] R. D. Poltmann 1995, Conversion of the delayed LMS Algorithm into the LMS algorithm, IEEE Signal Processing Lett, vol. 2, p. 223.
[2] Fábio Fabian Daitx, Vagner S. Rosa, Eduardo Costa, Paulo Flores, Sérgio Bampi 2008, VHDL Generation of Optimized FIR Filters, international conference on signal and system.
[3] Lan-Da Van, Wu-Shiung Feng 2001, An Efficient Systolic Architecture for the DLMS Adaptive Filter and Its Applications, IEEE transaction on circuit and system-II, VOL.48, NO 4.
[4] Pramod K. Meher, Megha Maheshwari 2011, A High-Speed FIR Adaptive Filter Architecture using a Modified Delayed LMS Algorithm, IEEE 978-1-4244-9474-3/11/00.
[5] K.R.Santha, V Vaidehi 2005, A New Pipelined Architecture for the DLMS Algorithm, IEEE Indicon 2005 Conference, Chennai, India.
[6] Lan-Da Van, Wu-Shiung Feng 2000, Efficient Systolic Architectures for l-D and 2-D DLMS Adaptive Digital, IEEE 0-7803-6253-5/00/.
[7] S. Ramanathan, V. Visvanathan 1996, A Systolic Architecture for LMS Adaptive Filtering with Minimal Adaptation Delay, 9th International Conference on VLSI Design.
[8] Basant K. Mohanty, Promod K.Meher, Delayed Block LMS Algorithm and concurrent architecture for high-speed implementation of Adaptive FIR Filter.
[9] Hesam Ariyadoost, Yousef S. Kavian, Karim Ansari-As 2011, Performance Evaluation of LMS and DLMS Digital Adaptive FIR Filters by Realization on FPGA, International Journal of Science & Emerging Technologies, Vol-1 No. 1.
[10] Bairu K. Saptalakar, Deepak kale, Mahesh Rachannavar, Pavankumar M. K. 2013, Design and Implementation of VLSI Systolic Array Multiplier for DSP Applications, International Journal of Scientific Engineering and

Technology (ISSN: 2277-1581) Volume 2 Issue 3, PP : 156-159 1.

[11] Purushothaman A, Dr.C.Vijaykumar2011, Implementation of Low power systolic based RLS adaptive Filter using FPGA, IEEE.

[12] Mahendra Vucha, Arvind Rajawat 2011, Design and FPGA Implementation of Systolic Array Architecture for Matrix Multiplication, International Journal of Computer Applications, (0975 – 8887) Volume 26– No.3

[13] C. Wenyang, L. Yanda. and J. Yuc 1991, Systolic Realization for 2D Convolution Using Conrigurable Functional Method in VLSI Parallel Array Designs, Proc. IEEE, Computer und Digital Technology, Vol. 138, No. 5, pp. 361- 370.

[14] Peter Mc Curry, Fearghal Morgan, Liam Kilmartin 2001, Xilinx FPGA implementation of a pixel processor for object detection applications, In the Proc. Irish Signals and Systems Conference, Volume 3, Page(s), 346 – 349.

[15] Feifei Dong, Sihan Zhang and Cheng Chen 2009, Improved Design and Analyze of Parallel Matrix Multiplication on Systolic Array Matrix, IEEE.

[16] H. Herzberg, R. Haimi-Cohen, and Y. Be'ery 1992, A systolic array realization of an LMS adaptive filter and the effects of delayed adaptation, IEEE Trans. Signal Processing, vol. 40, pp. 2799–2803.

[17] M. D. Meyer and D. P. Agrawal 1993, A high sampling rate delayed LMS filter architecture, IEEE Trans. Circuits Syst. II, vol. 40, pp. 727– 72

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