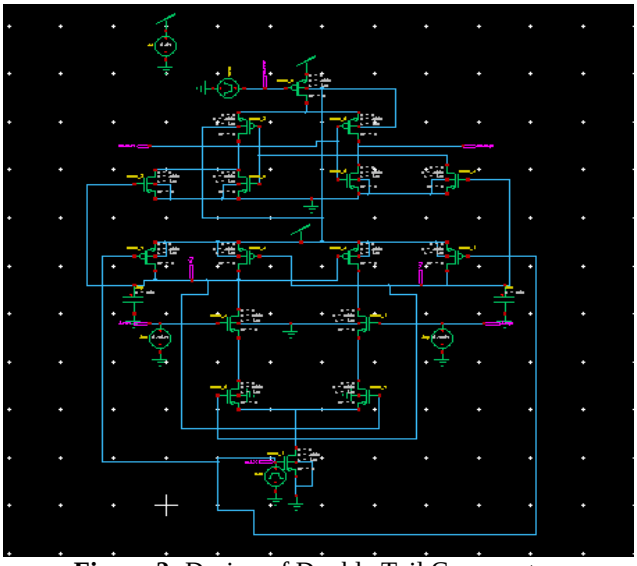

Figure 2: Design of Double Tail Comparator

As shown in figure 2, according to the input suppose Vinp>Vinn, then fn drops faster than fp. As long as fn continues falling, the corresponding pmos control transistor starts to turn on, pulling fp node back to VDD. So another control transistor (Mc2) remains off, allowing fn to be discharged completely. The control transistor Mc1 is on when Mc2 is grounded which results in static power consumption so two more switches (Msw1 and Msw2) are added. During the decision making phase the nodes fn and fp are precharged to VDD and it starts its different discharging. As soon as the comparator detects that one of the fn/fp is discharging faster, control transistor will help to increase the voltage difference. In other words, the operation of the control transistors with the switches emulates the operation of the latches [1].

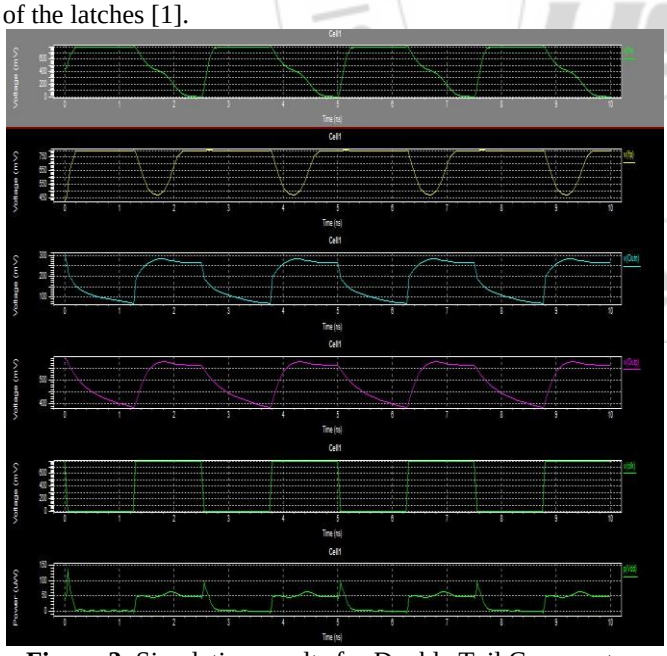

Figure 3: Simulation results for Double Tail Comparator

3. Successive Approximation Registor ADC

The most common ADCs are SAR ADCs. The main reason comes down to simplicity and design specifications. SAR ADCs have a conversion speed about 50kHz to 4MHz and take small chip area in comparison to flash ADCs, which are fast but take up a large area. Successive Approximation Register ADC is a better choice for low power applications as shown in table1. SAR ADC convert analog input to a digital code successively. In other words, one bit is determined in each clock cycle using binary search algorithm. The conversion time is maintained constant in SAR type A/D converter, and it is proportional to the number of bits in the digital output, unlike the other converters. The basic principle of this A/D converter is that the unknown analog input voltage is approximated against an n-bit digital value trying one bit at a time, beginning with the MSB [4]. Design of SAR ADC is shown in figure 4.

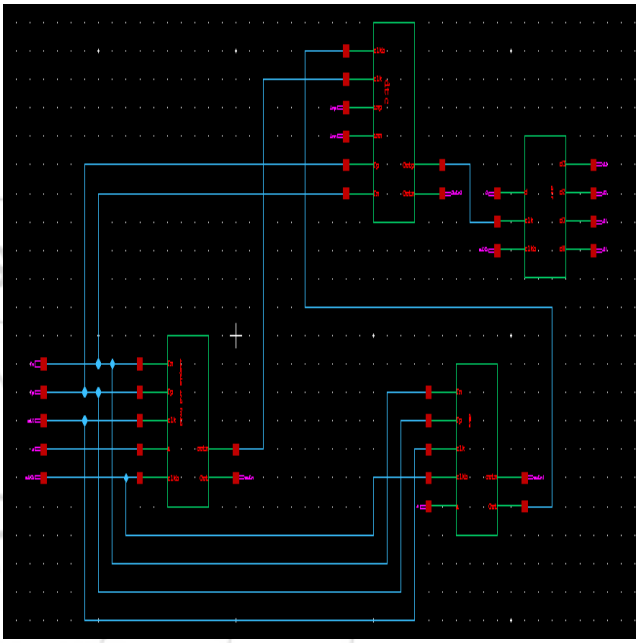

Figure 4: Design of SAR ADC

This type of A/D converter operates by successively dividing the voltage range by half, as explained in the following steps:

1) The MSB is initially set to 1 with the remaining three bits 0. The digital equivalent is compared with the unknown analog input voltage.
2) If the input voltage is higher than the digital equivalent, the MSB is retained as 1 and the second MSB is set to 1. Otherwise, the MSB is set to 0 and he second MSB is set to 1.
3) Comparison is made as given in step1 to decide whether to retain or reset the second MSB. The third MSB is set to 1 and the operation is repeated down to the LSB and by this time, the converted digital value is available in SAR.

Table 1: Comparison Between ADC's Topologies

Type	*Advantage*	*Disadvantage*
Dual Slope	• Greater noise immunity	• Slow • High precision external components required to achieve accuracy
Flash	• Very Fast	• Needs many parts (255 comparators for 8-bit ADC) • Lower resolution • Expensive • Large power consumption

S AR	• Capable of high speed • Medium accuracy • Good tradeoff between speed and cost • High resolution	• Speed limited ~5Msps (medius-fast)
Sigma-Delta	• High resolution	• Slow due to oversampling

This method uses a very efficient search strategy to complete an n-bit conversion in just n-clock periods. Therefore, for an 8-bit successive approximation type A/D converter, the conversion requires only 8 cycles, irrespective of the amplitude of analog input voltage. The circuit employs the a SAR which finds the required value of each successive bit by trial and error method. The analog output equivalent of the D/A converter is applied to the no inverting input of the comparator, while the other input of the comparator is connected with the unknown analog input voltage Vi under conversion. The comparator output is used to activate the successive approximation logic of SAR ADC [2].The simulation results for the SAR ADC is shown in figure 4.

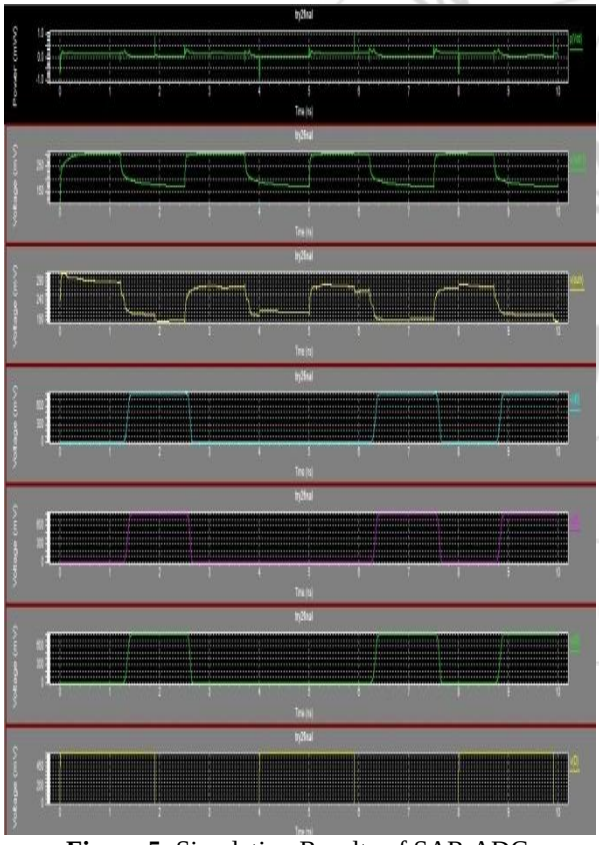

Figure 5: Simulation Results of SAR ADC

Table 2: Simulation Results For SAR ADC

Technology(nm)	65nm
Voltage(v)	o.8
Delay(ns)	1.205
Frequency(MHz)	500
Peak Power(µw)	0.06
Average Power(µw)	.0342

4. Conclusion

The primary advantages of SAR ADCs are low power, high resolution and accuracy, and a small form factor. Because of these benefits, SAR ADCs can often be integrated with other larger functions. Successive-approximation is the architecture of choice for nearly all multiplexed data acquisition systems, as well as many instrumentation applications. The SAR ADC is relatively easy to use, has no pipeline delay, and is available with resolutions to 18 bits and sampling rates up to 3 MSPS. SAR ADC is designed in tanner 13.0 software in 0.65um CMOS technology with power supply of 0.705v for vinn and supply voltage for vinp is 0.710v and having 500MHz frequency.

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