Clock signal is one of the main sources of chip power, high switching activity, heavy capacitive loading of the clock network. Mostly the latch based circuits are used. The low power circuits are most powerful in the circuit as the scaling increase the leakage powers increases. So far, removing these kinds of leakages there are many kinds of power gating techniques and to provide a better power efficiency[3]. The process of scaling techniques to nano meter regime has resulted in a rapid increase in leakage power dissipation. Here, the clock gate which could be enables the clock signal from the clock distribution network. This technique could be activating the clock which is needed for the operation of the circuit. The unnecessary clock signals are not activated during the clock gating. This saves the dynamic power of the circuit. The auto gated flip flops which are to be using clock gating technique for only small power consumption. The implementation of this technique could be much more difficult. The clock enabling signal from the each flip flop defines the more power dissipation included the gated logic. This circuit depends on the application for the device and it cannot be added as a delay based component.
Circuit simulation with inclusion of parasitics show that sensible power dissipation reduction is possible if input signal has reduced switching activity. In a synchronous system, a flip flop is triggered by a certain directional transition of a clock signal. For the clock to be another signal rather than the master clock, it must offer the same directional transition to trigger the flip flop and it must be in step with the master clock.

This look ahead clock gating has been shown[5] to be very useful in reducing the clock switching power than the data driven clock gating. The look ahead clock gating having the advantages that it stops the clock pulses also in the master latch, second making it applicable for large and general designs and third avoiding the tight timing constraints.

Clock gating is being used for reduction of power consumption in low power circuits for quite a while now. Adaptive clock gating is most rigorous of them all. Since gating the clock signals involve additional circuitry there exists a tradeoff between the additional number of gates and the total power consumption of gated clock.

4. Implementation

Data driven clock gating circuit diagram implementation is shown in the figures 3 and its respective waveforms in figure 4. The data driven clock gating causes area and power overhead. The power consumption could be reduced by using clock gating technique. This data driven clock gating signals having activity to enable the clock signals. So, the flip flops and the latches are to be enabled by using the gate signals. The outputs from the XOR gates are ORed to give the combination of output joint gate signals from the flip flops and then latched to avoid the glitches presented in the specified units[5]. The clock of the flip flop can be disabled in the next cycle by XORing its output with the present input data that will appear at its output in the next cycle. The data driven gating suffers from a very short time window where the gating circuitry can properly work. The cumulative delay of the XOR, OR, latch and the AND gater must not exceed the setup time of the flip flop. Such constraints may exclude five percent to ten percent of the flip flops from being gated due to their presence on timing critical paths. The exclusion percentage increases with the increase of critical paths, a situation occurring by down sizing or turning the transistors of non critical path to high threshold voltage for future power savings.

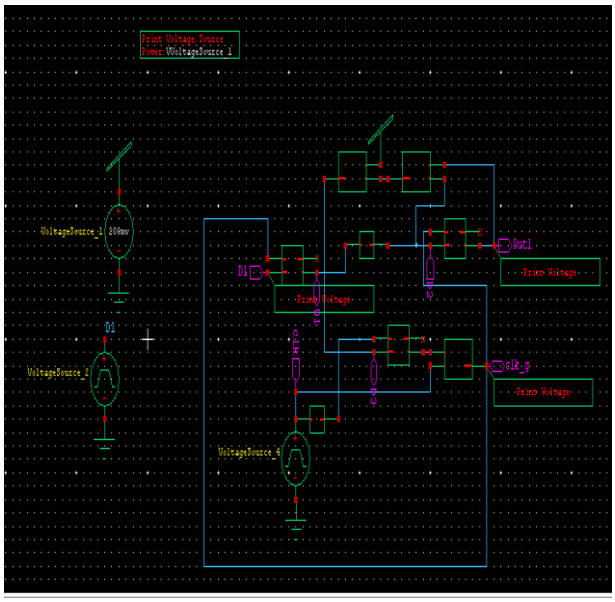

Figure 3: Data Driven clock gating Circuit Diagram

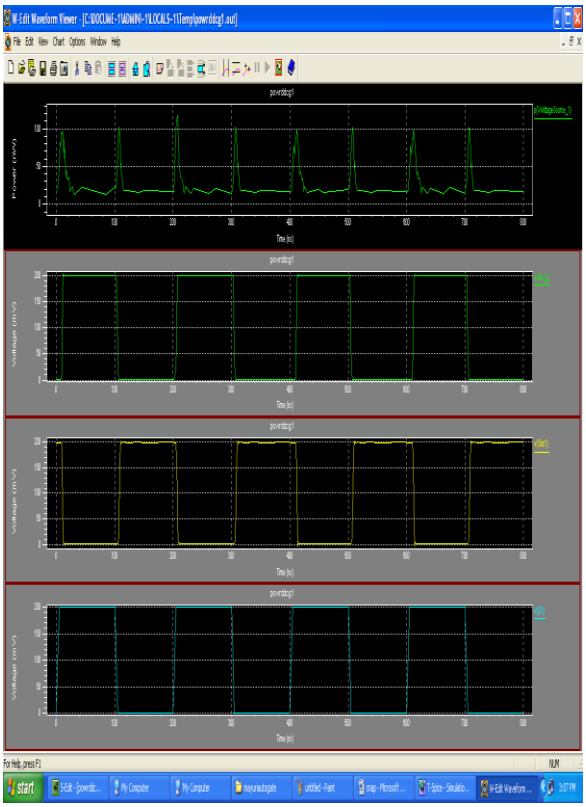

Figure 4: Data Driven clock gating Waveforms

The look ahead clock gating circuit diagram implementation is illustrated and shown in figure 5 and its waveform is shown in figure 6. The two flip flops are there the first is source flip flop and the second is the target flip flop. The

logic driving a target flip flop does not have an input externally of the block. X(D) denote the set of the XOR outputs of the source flip flops, and denoted by Q (D) the set of their corresponding outputs. The source flip flops can be found by a traversal of the logic path from D back to Q(D). Figure 6 shows the waveforms for look ahead clock gating circuit. The waveform shows input, output and the power waveforms. Clock enabling signals are very well understood at the system level and thus can effectively be defined and capture the periods where functional blocks and modules do not need to be clocked. Those are later being automatically synthesized into clock enabling signals at the gate level. In many cases, clock enabling signals are manually added for every flip flop as a part of a design methodology. Still, when modules at a high and gate level are clocked, the state transitions of their underlying flip flops depend on the data a being processed.

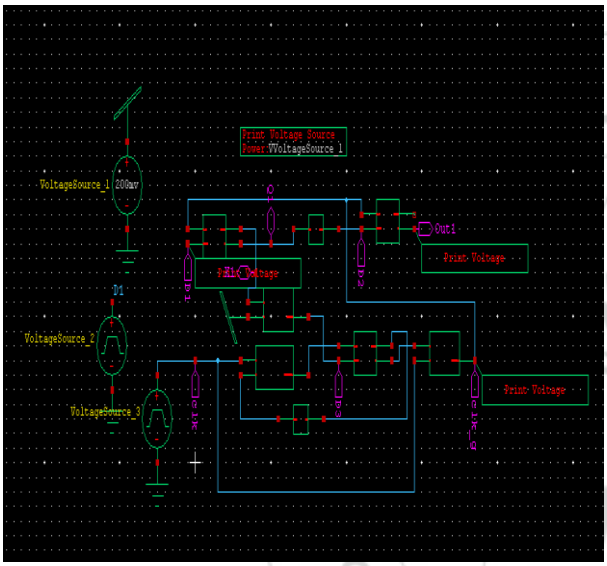

Figure 5: Look Ahead clock gating Circuit Diagram

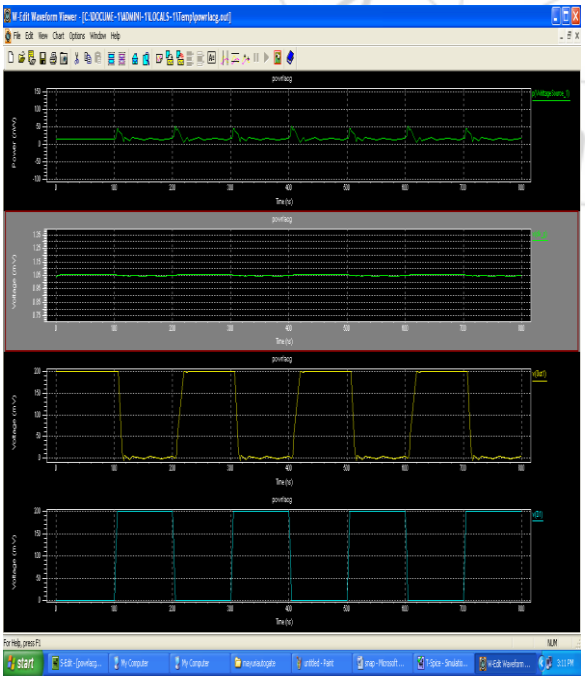

Figure 3: Look Ahead clock gating Waveforms

5. Simulation Results

The simulation results for the existing and proposed flip techniques were obtained and shown, in a 22nm technology at room temperature using Tanner EDA tools 13.00 over the supply voltage 200mv and frequency. Following table I shows the power comparison results for the data driven clock gating and look ahead clock gating delay for the respective designs. Table shows that data driven clock gating consumes 24nw and the look ahead clock gating consumes 16nw which is less than the data driven clock gating. With the reduction in the power consumed, the proposed technique is more beneficial.

Table 1: Power Consumption and Delay for Data Driven Clock Gating and Look Ahead Clock Gating.

Design Name	Supply Voltage	Power consumed	Delay
Data driven clock gating with inverter	200mv	24nw	4.2145ns
Look ahead clock gating with inverter	200mv	16nw	6.9005ns
Look ahead clock gating with adder	200mv	37nw	8.6123ns

6. Conclusion

In this paper, a low power look ahead clock gating is introduced and compared it with the previously clock gating technique i.e. the data driven clock gating. The result shows that the proposed low power look ahead clock gating is having the less power consumption than the previous data driven clock gating. This look ahead clock gating has been shown to be very useful in reducing the power. One of the major sources responsible for power consumption in digital circuits is the systems clock signal. It contributes towards a large amount of power consumption. Look ahead clock gating has been shown to be very useful in reducing the power consumed by digital systems. As this look ahead clock gating computing the clock enabling signals of each flip flop one cycle ahead of time, based on the present cycle data of the flip flop on which it depends, the drawbacks of the previously three gating methods have been overcome. The tight timing constraints existing in the auto gated flip flop and data driven clock gating methods has been avoided using this look ahead clock gating.

The look ahead clock gating has compared with the data driven clock gating method. The data driven clock gating method shows more power consumption than the look ahead clock gating method. The result shows a minimum power consumption than the data driven clock gating.

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