transistor is enhanced. The operating range of CC LSs depends only on the transistor threshold voltage (Vt) and size; but, the operating range of CC LSs is difficult to extend to the subthreshold region because the NMOS drive strength decreases exponentially. CC LSs require an exponential increase in NMOS transistor size, for converting a subthreshold voltage, which is impractical. So the subthreshold level conversion is not possible for small area. This level shifter supports bidirectional level conversion but full range bidirectional level conversion is somewhat challenging. Pull-up and pull-down strength must be analyzed for all combinations of input and output levels. Therefore, it has limited bidirectional regions because of unbalanced pull-up and pull-down strength.

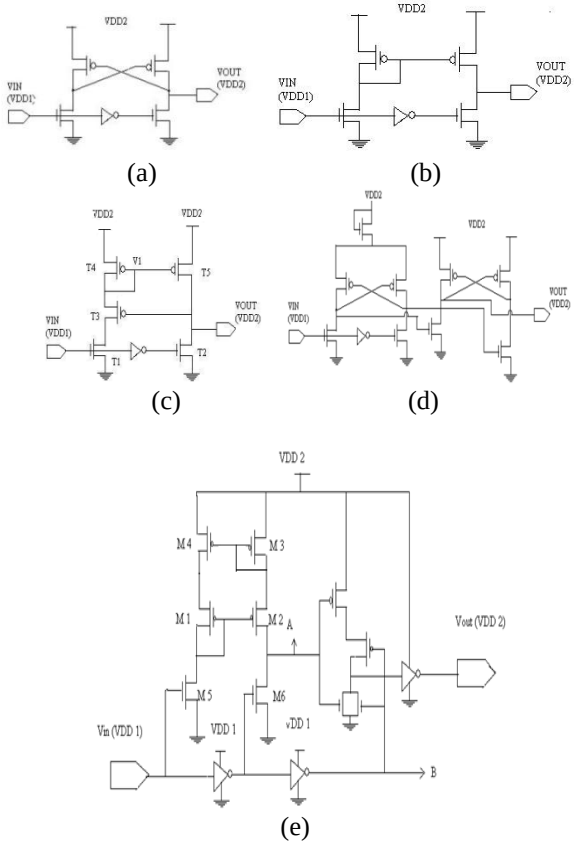


Figure 1: Conventional level shifters using (a) a cross coupled structure (CC); (b) a current mirror structure (CM); (c) a Wilsons current mirror structure (WCM); (d) a two stage cross coupled structure (TSCC); (e) a modified Wilsons current mirror structure

A Current Mirror structure: Fig. 1(b) shows a LS that uses a basic current mirror (CM). This can convert a deep subthreshold level because a high drain-to-source voltage of PMOS transistors facilitates the construction of a stable current mirror; it offers an effective on-off current comparison at the output. However, when the input voltage is suprathreshold, a high amount of quiescent current occurs. Because of this high power consumption limits the use of the conventional CM LS. A CM LS has a high quiescent current because of the bias currents.

Wilson current mirror structure: Fig. 1(c) shows Wilson current mirror (WCM) structure, which reduces the power consumption under a suprathreshold input. Here Balanced rising and falling delay ensures a 50% signal duty cycle. When input and output levels are close to each other, the duty cycle of the WCM LS is problematic. The WCM LS has a long rising delay, Because of a weak Pull up network, which is up to one hundred times longer than the falling delay. So the signal skew arises. Two stage cross coupled structure: Fig. 1(d) shows a two- stage CC LS (TSCC), in which the pull-up driving strength

Table I: Qualitative Comparisons for Subthreshold and Wide-Range Level Conversion

Criteria	CC	CM	WCM [3]	TSCC [6]	MWCM [4]	Proposed
1 .Small area for sub.vt. LC		√	√	√	√	√
2. Low power	√		√	√		√
3.Bidirectional LC.	√	√		√	√	√
4. Size & vt Insensitivity		√	√		√	√
5. Balanced Rising falling Delay	√	√		√	√	√

is reduced by a header NMOS, which expands the convertible input voltage. Operating range of the LS is determined by the transistor size and the Vt. As this is two stages cross coupling structure so the size automatically gets increases.

Modified Wilson current mirror structure: Fig. 1(e) shows modified Wilson current mirror structure. This level shifter also satisfy basic criterion that is small area for threshold level conversion. Bidirectional level conversion is possible; that is input and output levels can be scaled independently. This structure also balances the rising and falling delay. This provides less power consumption.

3. Proposed Level Shifter Structure

The proposed level shifter is a hybrid structured having Self biased cascode current mirror; CMOS logic gate and PTL based buffers. With the help of self biased cascode current mirror, the levels of voltage/current increases easily than the mirror circuit. It is also useful for low voltage analog and mixed mode circuit. The cascode connection is an effective method to suppress the channel length modulation. It also reduces the ratio errors due to difference in output and input voltages. The advantages of the cascode arrangement are it provides higher output impedance and it reduces the effect of miller capacitance on the input. The biasing technique is applied to keep the cascode transistor always operating in the saturation region so that the high precision and high output impedance can be maintained over a large operating range.

Pass transistor logic style is more power efficient than the CMOS logic style. The basic difference between the pass transistor logic style and CMOS logic style is that the source side of the logic transistor is connected to the some input signals instead of the power supply. In this logic style one

pass transistor is sufficient to perform the whole logic operation, which reduces the number of transistors. In CMOS inverter, the tripping of the inverter is depends upon the input. When input is LOW, the output of the inverter is HIGH. When input is HIGH, the output of the inverter is LOW. But in Pass transistor logic the output of the inverter depends upon the input as well as the circuit input.

Current mirror is the basic building block, which is widely used in analog VLSI design. Sensitivity and temperature variation should be very less for high performance analog circuit applications. Also it has the wide range of the working frequency. The proposed level shifter structure is shown in Fig. 2.

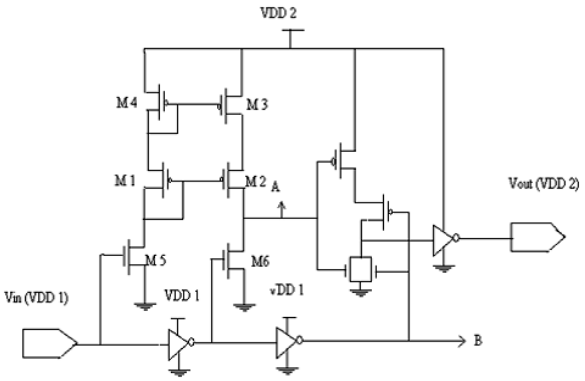


Figure 2: Proposed circuit diagram

A cascode current mirror is located with the help of transistors M1, M2, M3 and M4. The level shifter can be divided in three main blocks; first self biased cascode current mirror; second delay circuit and third one is the CMOS OR gate. Here self biased cascode current mirror circuit balances the rising and falling delay but when input and output levels are close to each other then there is a problem skews that is cascade PMOS has insufficient drive currents which increases the rising delay. To reduce the rising delay, a delay path is designed. This delay path is designed with the help of inverters which acts as a buffer. At last the CMOS OR gate is there in output stage which gives proper output, and limits the leakage current. When VDD1 is sub-threshold and VDD2 is high, the cascode current mirror structure balances the rising and falling delay at Node A. The CM-type structure provides a wide operating range, and the stacked PMOS transistors in the complementary OR gate limit the leakage current.

When input voltage increases, the rising signal from Nodes A and B that achieves the trip-point voltage more quickly triggers the rise of VOUT. When VDD2 is higher than VDD1, then the voltage level at the point A get increases. When VDD2 is lower than VDD1, then the voltage level at the point B get increases. When VDD2 is considerably greater than VDD1, the cascode current mirror has similar rising and falling delays. To balance the rising and falling delay when VDD2 is less than VDD1, two VDD1 inverters are used long channel length. All low-Vt transistors (LVTs) were used for performance analysis. Using these LVTs reduces circuit delay and power consumption in the circuit. When the input level is ultra-low and has a slow slew rate at that time it has high short circuit power. In this level shifter, NMOS LVTs reduces the transition time and short-circuit power consumption where as PMOS LVTs reduces the rising delay and the voltage drop.

4. Simulation and Measurement Results

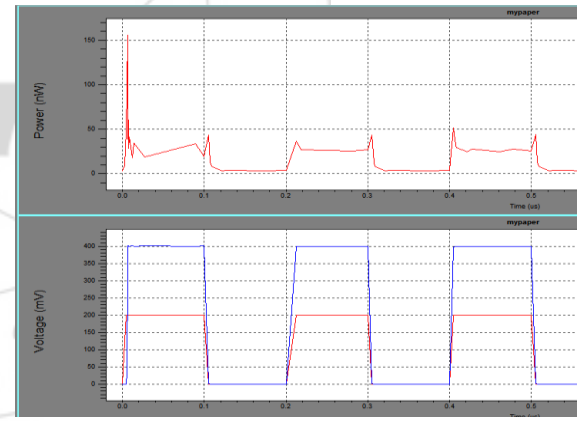
Tanner tool is used for the simulation of the proposed level shifter circuit. The simulation and measurement results were verified using 22-nm technology. The minimal operating range for the proposed level shifter circuit in less than 200mv.
In 22-nm technology the ΔV that is the voltage drop is 100mv.

Table II shows the comparison of the proposed level shifter circuit with Modified Wilsons current mirror Circuit

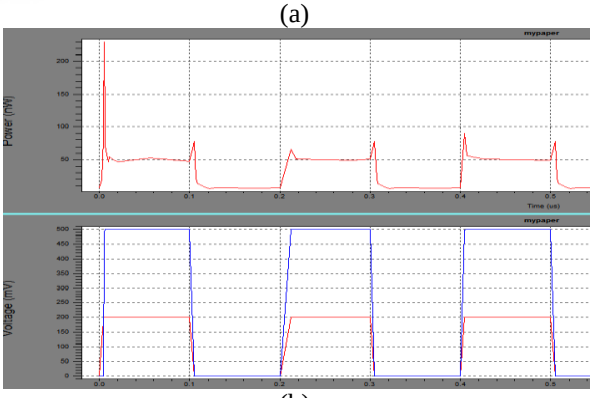
Table 2

SR.No.	Parameters	Self-biased Cascoding Current mirror. VDD1= 200mv		Modified Wilsons Current Mirror. VDD1=200mv	
		VDD2=400mv	VDD2=800mv	VDD2=400mv	VDD2=800mv
1.	Power Consumption	16nW	173nW	23nW	566nW
2.	Delay	50ns	54ns	52ns	53ns
3.	Duty cycle	28%	38%	20%	24%

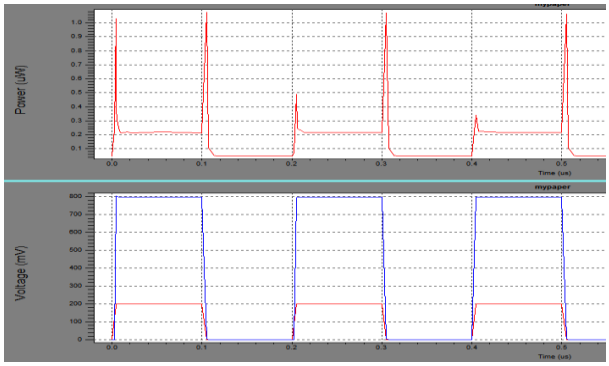
Fig. 5 shows the graphical representation of power consumption for input that is constant 200mv and the VDD2 which is 400mv, 500mv, 800mv, and 1200mv respectively.



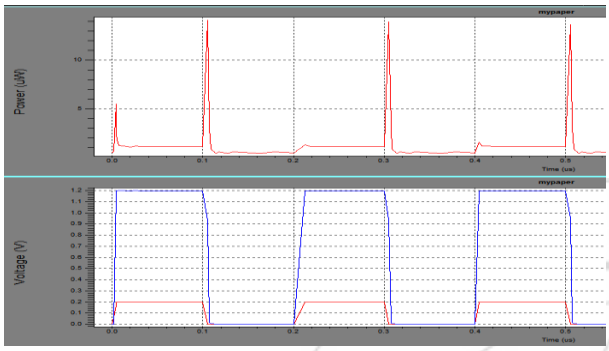
(a)



(b)



(c)



(d)

Figure 5: Simulation waveform of corresponding power consumption: (a) 200mv-400mv (b) 200mv-500mv (c) 200mv-800mv (d) 200mv-1200mv

5. Conclusion

In this paper, A Wide range level shifter using self biased cascode current mirror is presented. This is used for various applications where the ultra low power is required. This self cascode current mirror level shifter is designed for full rang and bidirectional level conversion. The minimal operating voltage is the deep sub-threshold voltage which is less than 200mv, close to the minimal supply voltage of the digital circuit and the maximal operating voltage is the standard supply voltage defined in transistor technology which is 1.2v. The power consumption of the proposed level shifter is verified using 22nm technology. The performance of the level shifter is compared with existing level shifter and according to the results it can be concluded that this level shifter gives best results with low power consumption.

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