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Level Shifted Pulse Width Modulation in Three Phase Multilevel Inverter for Power Quality Improvement

S. B. Sakunde[1], V. D. Bavdhane[2]

[1] PG Student, Department of Electrical Engineering, Zeal education society's DCOE, Narhe ,Pune, Maharashtra, India

[2]Assistant Professor, Department of Electrical Engineering, Zeal education society's DCOE, Narhe ,Pune, Maharashtra, India

Abstract: ***This paper emphasize on harmonics elimination by using 5 level cascaded H-bridge (CHB) inverter. The CHB inverter is having more importance in power electronics application due to reduction in switching losses to other type of inverter. The inverter is adopted with level shifted carrier PWM (LSCPWM) technique. The reference harmonics compensating current signal is generated by synchronous reference frame (SRF) theory and DC side voltage of inverter is regulated by using PI controller. The inverter functions as a DSTATCOM for reduction of harmonics and improvement of power factor. System is designed in MATLAB/SIMULINK for 11kV distribution system.***

Keywords: Synchronous reference frame theory (SRF), phase shifted carrier pulse width modulation (PSCPWM), level shifted carrier pulse width modulation (LSCPWM), cascaded H bridge multilevel inverter (CHB)

1. Introduction

With present distribution system, the use of non-linear devices has been increased to large extent which results in injection of large amount of harmonics in the distribution side which further leads to major power quality issues. The consequences observed are voltage sag, swell, heating effects in rotating devices, reactive power burden, lagging power factor etc. [1-5]

With development in power utility and power electronics, various techniques have been implemented for reduction of harmonics. The multilevel inverter found their importance in power quality improvement.[6-9] The most important topologies like diode-clamped inverter (neutral-point clamped), capacitor-clamped (flying capacitor), and cascaded multilevel inverters with separate dc sources are discussed in literatures. Various control and modulation techniques are being presented for these topologies of inverters. [10-12]

This paper focuses on level shifted pulse width technique used for cascaded 5 level H-bridge inverter. This inverter functions as DSTATCOM in order to reduce harmonics and improves the power factor also.

2. DSTATCOM

DSTATCOM consists of voltage source converter (VSC) with DC link capacitor connected in shunt, capable of absorbing or supplying the reactive power. As VSC is having two voltage levels, the power injection takes place but harmonics remain same. In order to reduce the harmonic contents ,DSTATCOM with multilevel inverter is expected for better operation. DSTATCOM also improves power factor to unity.[9]

DSTATCOM converts DC link voltage into set of three phase AC voltage so that active and reactive power transfer to transmission line takes place. If DSTATCOM voltage is equal to source voltage then there is no power transfer to transmission line. If DSTATCOM voltage is greater than source voltage then power is injected to transmission line. If DSTATCOM voltage is lower than source voltage then power is absorbed from transmission line. The schematic diagram of DSTATCOM is presented in fig.1.

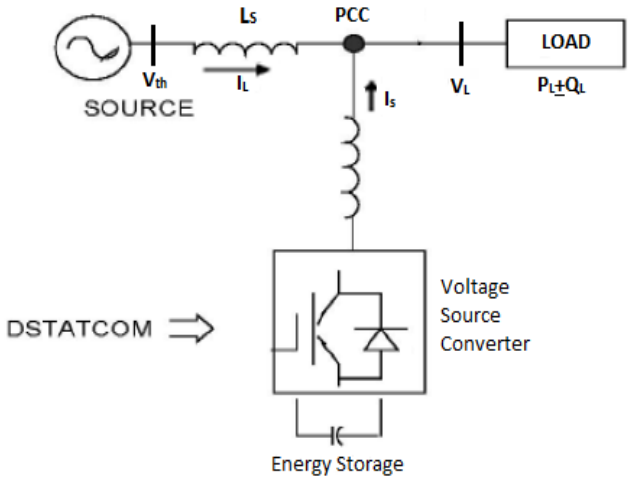

Figure 1: Schematic diagram of DSTATCOM

This paper proposes DSTATCOM with five level CHB inverter with DC link as capacitor which stores or inject power as per requirement. DSTATCOM is connected in shunt to transmission line through inductive reactance which is useful for filtering action. Also the DSTATCOM produces current having magnitude equal to of harmonics current but opposite in direction so that harmonics current get nullified. As it is capable of injecting reactive power at point of common coupling (PCC), the voltage profile is improved which leads to improved voltage regulation.

3. Three Phase Cascaded Multilevel Inverter

A five level LSPWM based CHB is illustrated in fig.2. DC source is connected to each inverter separately. Each inverter in a phase generates three different voltage outputs, +Vdc, 0, and –Vdc by different combinations of the four switches. In CHB inverter the ac outputs of each of the different full bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels of inverter x in a cascaded inverter is defined by x=2y+1, where y is per phase separate dc sources.

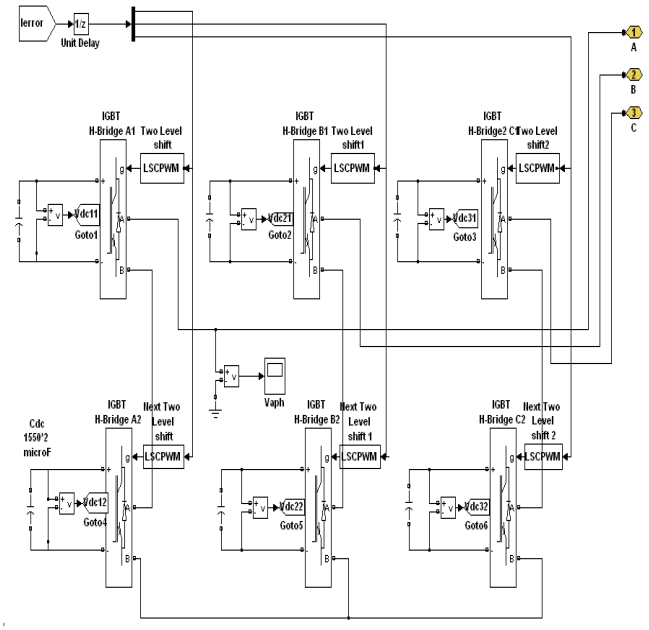

Figure 2: Three phase cascaded five level inverter

4. PWM technique for gate signal generation

Generally following two PWM methods are used for gate signal generation in multilevel inverters.

1. Level Shifted Carrier PWM (LSCPWM)
2. Phase Shifted Carrier PWM (PSCPWM)

The level shifted pulse width modulation technique has three types [13]

1. In Phase disposition
2. Phase disposition opposition
3. Alternate phase opposition disposition

This work focuses on in phase disposition method where all the carrier signals are in phase as shown in Fig.3. The numbers of carrier waveforms required are given by m-1, where m is number of output voltage levels. So the 5 level CHB inverter requires four triangular carrier waveforms. The triangular carrier waveforms with frequency 2 kHz are chosen.

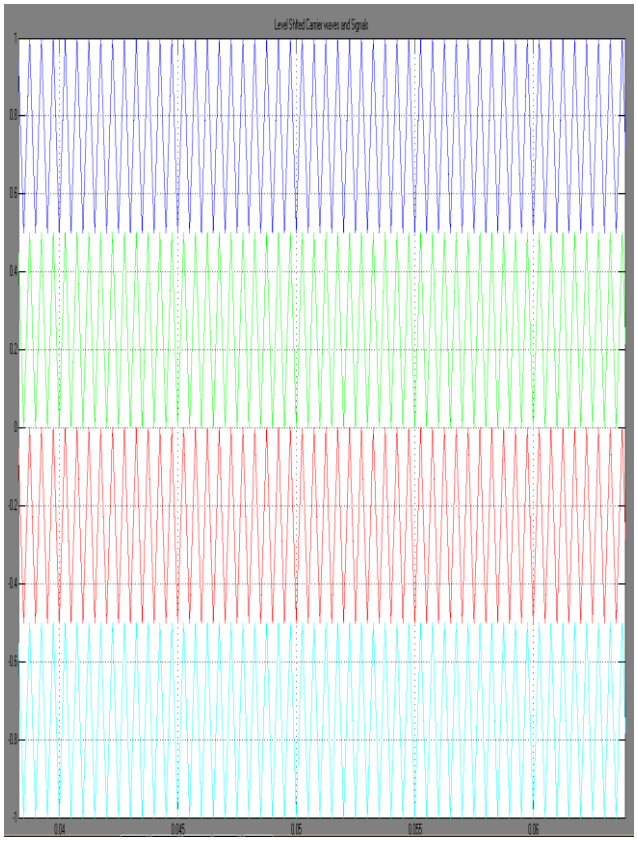

Figure 3: Level Shifted carrier PWM

The level shifted carrier pulses are generated with repeating sequence in MATLAB/SIMULINK environment as shown in fig. 4. Carrier waveform is continuously compared with error signal to provide gate signal to inverter.

5. MATLAB Modeling and Results

The system parameters considered for simulation study are tabulated in table-1.

Table 1: System parameter

System parameter	*Rating*
Source voltage	11 kV
Frequency	50Hz
DC bus capacitance	1550e-6F
Inverter series inductance	10 mH
Source resistance	0.1 ohm
Source inductance	0.9 mH
Load resistance	60 ohms
Load inductance	30mH

5.1 Results Obtained Without DSTATCOM

The Matlab model for basic power system without any compensating device is shown in Fig.5. The basic power system with 11kV source is considered and designed with parameters tabulated above.

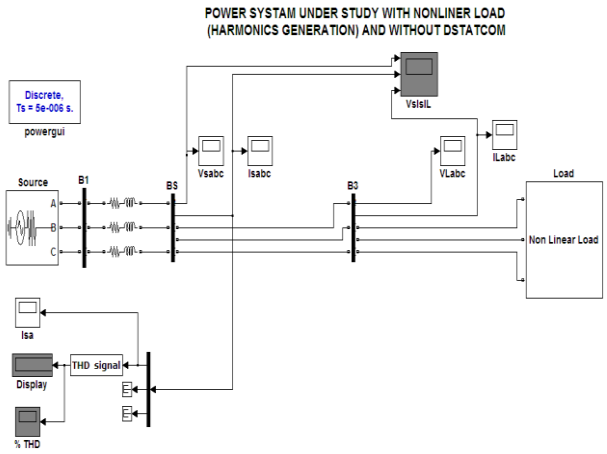

Figure 5: Basic uncompensated power system under study with a nonlinear load

The source voltage, current and load current without DSTATCOM are presented in fig.6. It seems that load current and source current both are same and non sinusoidal without DSTATCOM.

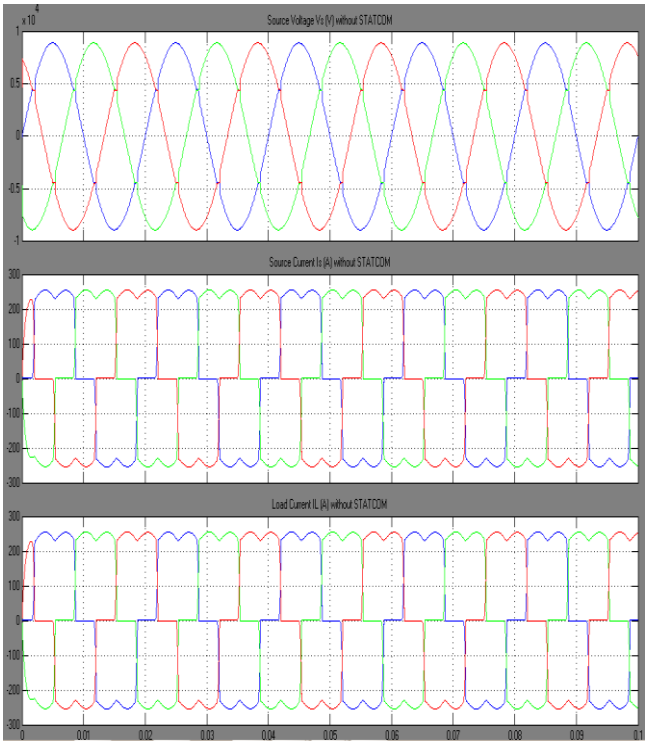

Figure 6: Source voltage, source current and load current without DSTATCOM

The harmonic spectrum of Phase-A source current without DSTATCOM is presented in fig.7. The THD of source current without DSTATCOM is observed as 28.25%.

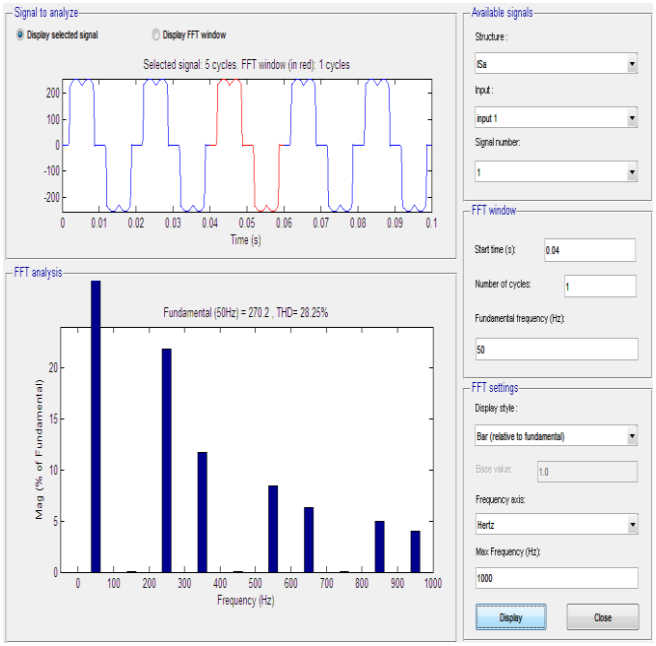

Figure 7: Harmonic spectrum of Phase-A Source current without DSTATCOM

5.2 Results Obtained LSCPWM based DSTATCOM

The MATLAB/SIMULINK model of power system under study compensated with multilevel CHB based inverter with LSCPWM using SRF based method is represented in fig.8.

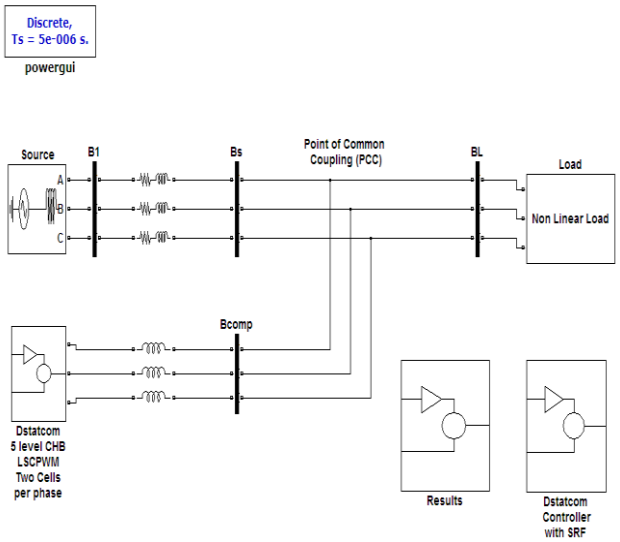

Figure 8: Simulink model of power system with DSTATCOM

The voltage of Phase A of Five level LSPWM inverter is represented in fig. 9. It shows five step output.

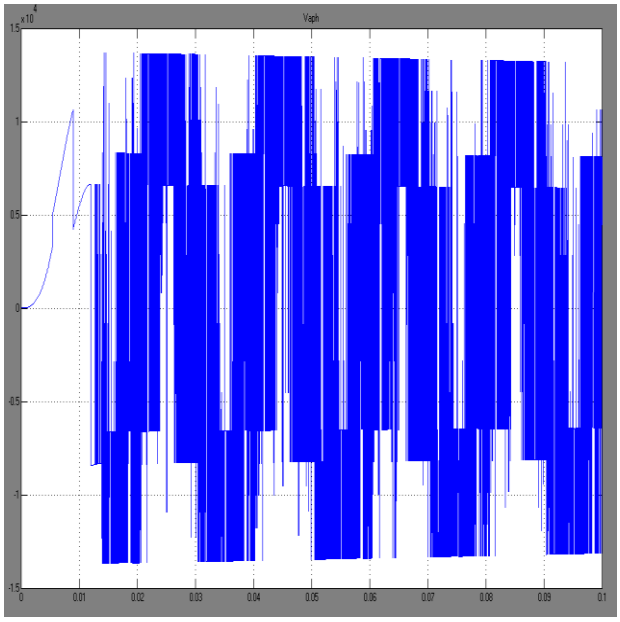

Figure 9: Five level output voltage of inverter

Fig.10 shows source voltage, current and load current with five level CHB inverter with LSCPWM based DSTATCOM using SRF method. In this case the source current is found more sinusoidal in comparison to system without compensating device.

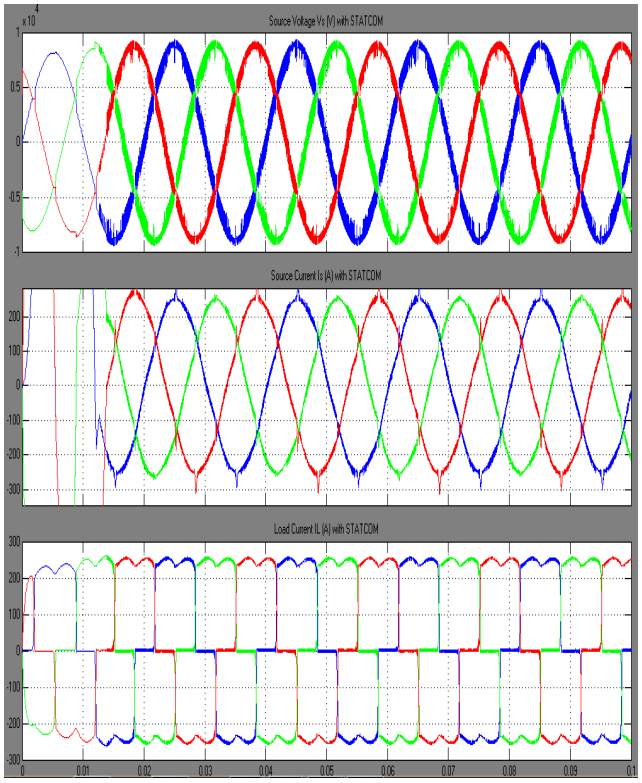

Figure 10: Source voltage, current and load current with five level CHB inverter with LSCPWM based DSTATCOM

Harmonic spectrum analysis of Phase-A Source current with five level CHB inverter with PSCPWM based DSTATCOM using SRF method is shown in fig.11. The THD of source current with five level inverter is further reduced to 4.68%.

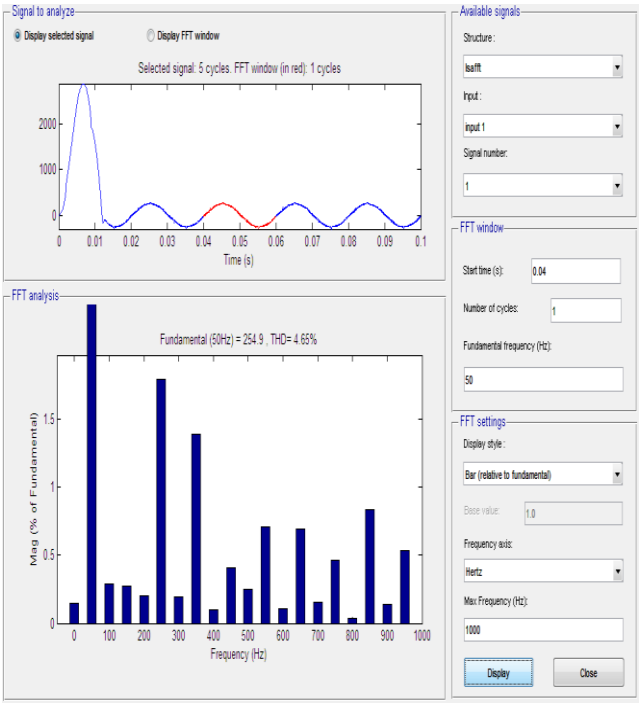

Figure 11: Harmonic spectrum analysis of Phase-A Source current with five level CHB inverter with LSCPWM based DSTATCOM

For this case the source current and voltage both are found to be in phase, so power factor is unity as shown in fig.12.

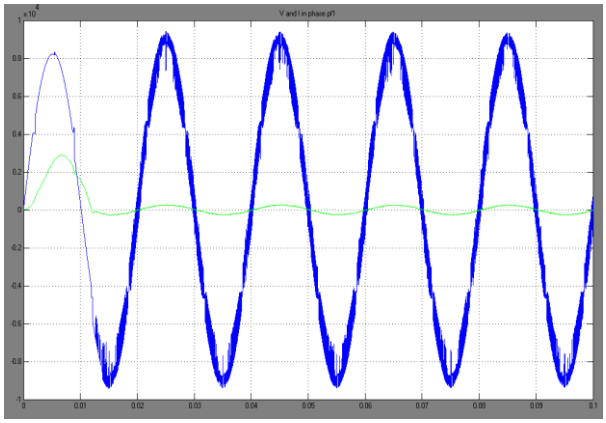

Figure 12: Phase-A Source voltage and current

Meanwhile the DC side voltage of capacitor is regulated to 11KV as shown in fig.13.

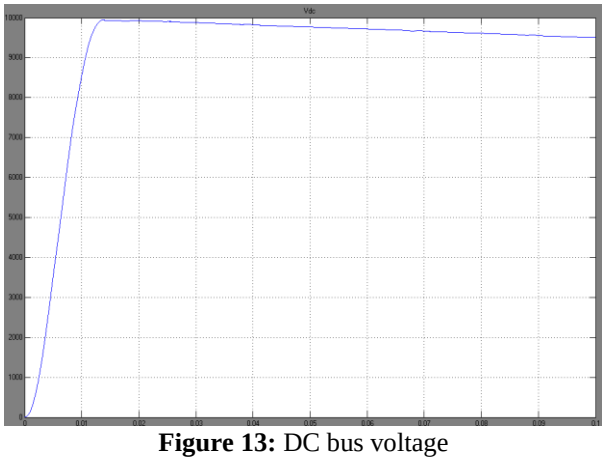

Figure 13: DC bus voltage

6. Conclusion

In this paper five level multilevel inverter with LSCPWM based CHB inverter is presented. The percentage of total harmonic distortion is reduced with LSCPWM multilevel inverter method of gate signal generation from 28.25 to 4.65 %. This method found superior in support to power quality issue. The total harmonics distortion can be further reduced by increasing number of steps of inverter.

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