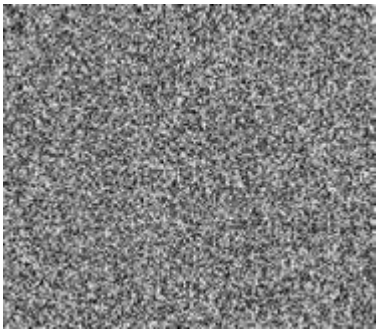
converted grey image. Header file is then read in XPS using system c and after implementing on SPARTAN 3 EDK board we get the results as shown in figure 5.

(a) Input Image



(b) Encrypted Image

(c) Decrypted Image

Figure 5: (a) Input Image (b) Encrypted Image (c) Decrypted Image

4. Conclusion

AES algorithm on FPGA based image encryption and decryption has been proposed in this paper to protect the confidential image data from an unauthorized access. This AES algorithm can process with the data block of 128 bit and cipher key length of 256 bit. Same key is used to encrypt and decrypt the data. The use of 256 bit cipher key to achieve the high security, because 256 bit cipher key is difficult to break. As a result of this secure transmission of image can be possible. Xilinx platform studio (XPS)10.1 with impulse c is used for synthesis of AES algorithm.

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