



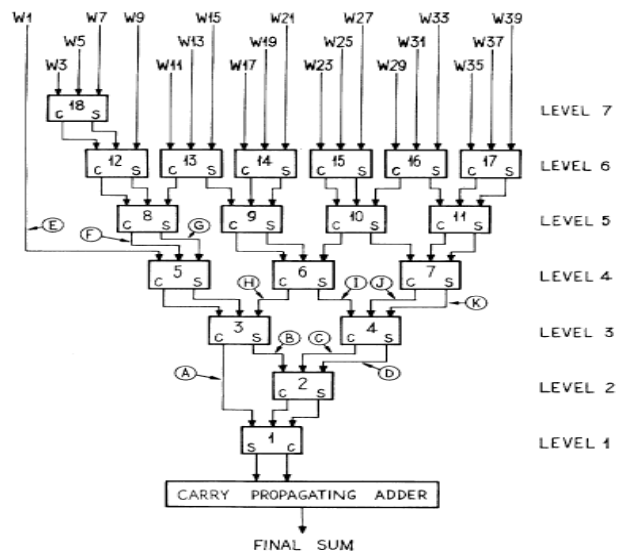
full adder in reduced complexity Wallace Multiplier at the place of Full adder of standard Wallace Multiplier in order to reduce Area, Power and improvement in speed. An Energy Efficient CMOS Full adder design using alternative logic scheme gives low power delay product (PDP), in terms of speed, power consumption and reduced area. This paper proposes use of new Energy Efficient switching method that is Adiabatic switching for CMOS full adder in reduced complexity Wallace multiplier in order to reduce power even further.

Adiabatic Logic is the term given to low-power electronic circuits. The problem of energy dissipation in smaller and faster circuit is solved by Adiabatic logic. The main causes of energy dissipation in CMOS circuits is due to the charging and discharging of the node capacitor. In adiabatic switching, the process of charging and discharging the node capacitances is carried out in a way so that a small amount of energy is wasted and a recovery of the energy stored on the capacitors is achieved. Adiabatic switching can be achieved by ensuring that the potential across the switching devices is kept arbitrarily small. This can be achieved by charging the capacitor from a time varying voltage source or constant current source.

## 2. Literature Review

1. Authors Shahebaj Khan, Sandeep Kakde, Yogesh Suryawanshi proposed a technology entitled “VLSI Implementation of Reduced Complexity Wallace Multiplier Using Energy Efficient CMOS Full Adder” in which modified reduced complexity Wallace Multiplier with reduced power consumption and area by using Energy Efficient CMOS Full Adder at the place of conventional Full adder is presented. From the literature view it can be seen that proposed multiplier reduced power and total number of gate count i.e. area is reduced.

2. Author C. S. WALLACE et.al. in this paper suggested a technology for multiplier entitled “A Suggestion for a Fast Multiplier” suggest A Multiplier is an easily hardware implementable and efficient methodology, that multiplies two integers. For unsigned multiplication, up to n shifted copies of the multiplicand are added to form the result. The entire procedure is carried out into three steps 1.partial product (PP) generation 2.partial product grouping & reduction 3.final addition. The following diagram shows the adder tree design by Wallace.



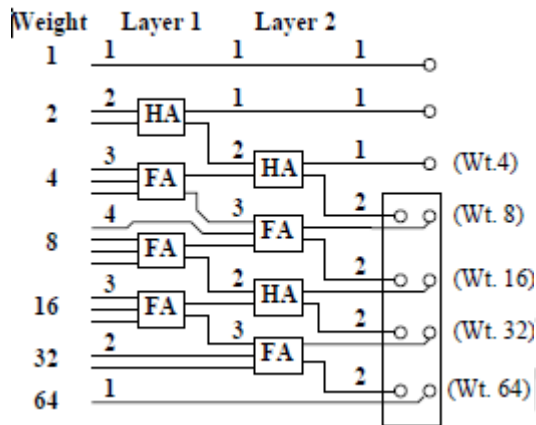
3. Authors Kazunari Kato, Yasuhiro Takahashi, and Toshikazu Sekine in paper entitled “Two Phase Clocking Sub threshold Adiabatic Logic”. They propose a novel sub-threshold adiabatic logic. Our previously proposed ultra-low power sub threshold adiabatic logic has been a problem that noise margin is reduced, so that it is impossible to implement a cascade connection. In this paper, they propose a novel sub-threshold adiabatic logic. To evaluate their proposed circuit, a half adder, full adder, dynamic flip flop and 4×4 array multiplier are designed, and then the operation function and power dissipation are confirmed. From the simulation results, the power dissipation of the proposed multiplier is lower than that of the conventional CMOS.

4. Author Nazrul Anuar, Yasuhiro Takahashi, and Toshikazu Sekine in paper entitled “4-bit Ripple Carry Adder using Two Phase Clocked Adiabatic Static CMOS Logic” proposed the low energy operation of 4-bit ripple carry adder (RCA) employing two phase clocked adiabatic static CMOS logic (2PASCL) circuit techniques. They evaluate NOT, NAND, XOR and NOR logic gates on the basis of the 2PASCL topology using SPICE implemented using 0.18 m CTX CMOS technology. For NOT circuit, the analytical and simulation values are compared. By removing the diode from charging path, the higher output amplitude is achieved and the power consumption of the diode is eliminated. From the simulation results, they noticed that 4-bit 2PASCL RCA can save an average of 71.3% of dissipated energy as compared to that with a static 4-bit CMOS RCA at transition frequencies of 10 to 100 MHz. The results indicate that 2PASCL technology can be advantageously applied to low-power digital devices operated at low frequencies, such as radio-frequency identifications (RFIDs), smart cards, and sensors.

5. Authors M. Chanda, A. Dandapat, Toshikazu SekineH. Rahamanin paper entitled “Ultra Low-Power Sequential Circuit Implementation by a Quasi Static Single Phase Adiabatic Dynamic Logic (SPADL)” proposed Implementation of sequential logic circuits by using a novel Quasi-Static Single-phase Adiabatic Dynamic Logic (SPADL) has been presented. SPADL uses only a single sinusoidal source as supply-clock. This not only ensures

lower energy dissipation, but also simplifies the clock design which would be otherwise more complicated due to the signal synchronization requirement. Simplicity and static logic resembled characteristics of SPADL logic, substantially decreases circuit complexity with improved driving ability and circuit robustness.

### 3. Proposed Work



**Figure:** Wallace Tree Multiplier

Wallace multipliers act in three stages: 1) Generate all bits of the partial products in parallel. Collect all partial products bits with the same place value in bunches of wires and reduce these in several layers of adders till each weight has no more than two wires. For all bit positions which have two wires, take one wire at corresponding place values to form one number, and the other wire to form another number. Add these two numbers using a fast adder of appropriate size.

We assume that Full adders and half adders will be used. A full adder takes 3 inputs and produces one output of the same weight (sum) and another of higher weight (carry). This is called a (3,2) adder. It reduces the number of wires at its own weight by 2 and adds one wire at the higher weight. A half adder takes 2 inputs and produces one output of the same weight (sum) and another of higher weight (carry). This is a (2,2) adder. It reduces the number of wires at its own weight by 1 and adds one wire at the higher weight. The reduction algorithm is general and can be used with any adders of type (n, m). For example, a carry save adder is of type (4, 2).

Each reduction stage looks at the number of wires for each weight and if any weight has more than 2 wires, it adds a layer of adders. When the numbers of wires for each weight have been reduced to 2 or less, we form one number with one of the wires at corresponding place values and another with the other wire (if present). These two numbers are added using a fast adder of appropriate size to generate the final product.

At any layer, if we find 3 wires for any weight, we place a Full Adder, which generates 1 wire of the same weight and 1 wire with the next higher weight. We place enough full adders in this layer such that the remaining wires for any weight are less than 3. If only one wire is left, it is carried through to the next layer. If there are two wires left after

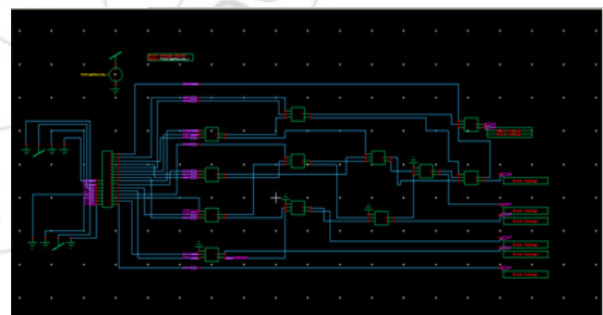
using Full Adders for all groups of 3, we have the option of either passing them both through to the same weight or to pass 1 wire to the same weight and the other to the next higher weight (using a Half Adder). Different rules apply for the last reduction step and the earlier ones.

Bits on the right with no in-coming carry are reduced with a half adder. This reduces the size of the final adder as single wires will be left for bits on the right. If this is not the last layer and the next layer will have In-coming carry wires, we pass through the 2 wires if it will make the number of output wires at this weight a multiple of 3. Otherwise, we place a half adder. The reduction procedure is carried out for all weights. Starting from the least significant weights. At the end of each layer, we count wires for each weight again, and if none has more than 2 wires, we proceed to the final addition stage. If any weight has 3 or more wires, we add another layer, and repeat this procedure till the number of wires for all weights is reduced to 2 or less. Now we compose one number from one of the left over wires at corresponding weights and another from the remaining wires. Finally, we use a conventional fast adder of appropriate size to add the two numbers.

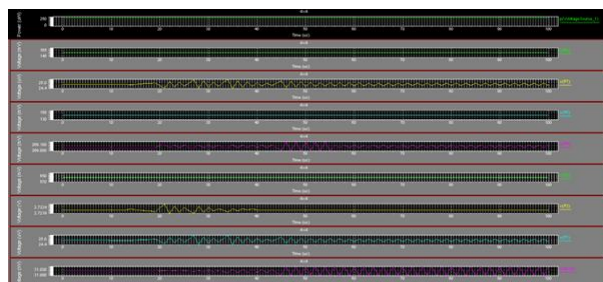
Consider a multiplier for 4X4 bits. Partial products are generated in parallel and we have the following wires:

Weight	Terms	Wires
1	a0b0	1
2	a0b1, a1b0	2
4	a0b2, a1b1, a2b0	3
8	a0b3, a1b2, a2b1, a3b0	4
16	a1b3, a2b2, a3b1	3
32	a2b3, a3b2	2
64	a3b3	1

### 4. Implemented Work



**Figure:** conventional RCWTM without Adiabatic



**Figure:** Waveform of conventional RCWTM without Adiabatic

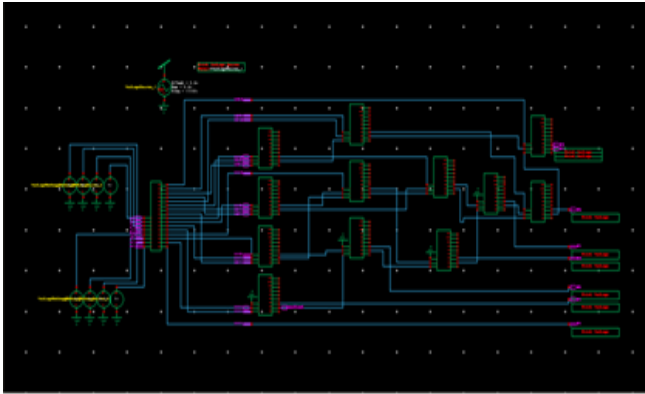


Figure: RCWTM using Adiabatic Logic

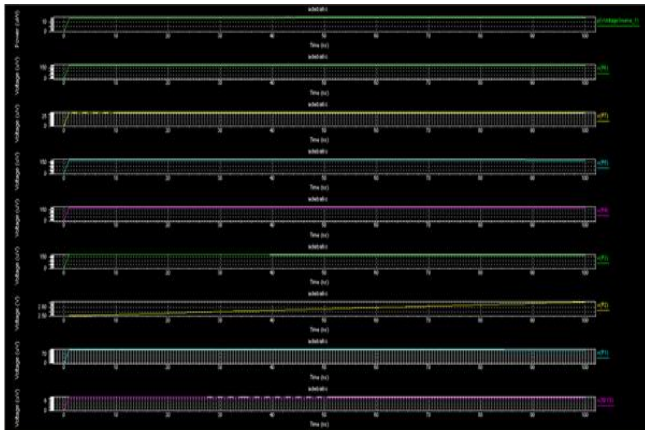


Figure: Waveform of RCWTM using Adiabatic Logic

## 5. Comparison Table

COMPARISON TABLE BETWEEN POWER AND CURRENT OF RCWTM AND RCWTM USING ADIABATIC LOGIC

PARAMETER	RCWTM	RCWTM ( ADIABATIC)
CURRENT	104.41593 $\mu$ A	6.83052 nA
POWER	313.24780 $\mu$ W	17.07630 nW

## 6. Conclusion

The CMOS Switching method for designing low voltage and low power Wallace Tree Multiplier has been presented. The proposed Adiabatic Switching structure and the RCWM to benefit the high speed and low power. A simple approach is proposed in paper to reduce the area and power of RCWM. This new switching technique offers the great advantage in the reduction of area and also the total power. In this paper, energy efficient Reduced Complexity Wallace Tree Multiplier Proposed. By the process of charging and discharging the node capacitances is carried out in a way so that a small amount of energy is wasted and a recovery of the energy stored on the capacitors is achieved.. They have analyzed the Adiabatic switching can be achieved by ensuring that the potential across the switching devices is kept arbitrarily small. This can be achieved by charging the capacitor from a time varying voltage source or constant current source. Due to the small area required for adiabatic switching this multiplier is high speed, low area and very low power multiplier.

## References

- [1] Shahebaj Khan, Sandeep Kakde, Yogesh Suryawanshi, "VLSI Implementation of Reduced Complexity WallaceMultiplier Using Energy Efficient CMOS Full Adder", 978-1-4799-1597-2/13 ©2013 IEEE
- [2] C. S. WALLACE, "A Suggestion for a Fast Multiplier", IEEE TRANSACTIONS ON ELECTRONIC COMPUTERS.
- [3] Kazunari Kato, Yasuhiro Takahashi, and Toshikazu Sekine, "Two Phase Clocking Subthreshold Adiabatic Logic", 978-1-4799-3432-4/14 ©2014 IEEE
- [4] Nazrul Anuar, Yasuhiro Takahashi, and Toshikazu Sekine, "4-bit Ripple Carry Adder using Two Phase Clocked Adiabatic Static CMOS Logic", 978.1.4244.4547.9/09 c 2009 IEEE
- [5] M. Chanda, A. Dandapat, Toshikazu SekineH. Rahamanin, "Ultra Low-Power Sequential Circuit Implementation by a Quasi Static Single Phase Adiabatic Dynamic Logic (SPADL)", 978-1-4244-4547-9/09 ©2009 IEEE
- [6] S.Kim and M.C.Papaefthymiou . "Single-phase source-coupled adiabatic logic," in Proc. Int. Symp. Low-Power Electron. Design, San Diego, CA, Aug. 1999, pp. 97–99.
- [7] H.Mahmoodi-Meimand , A.Afzali-Kusha and M.Nourani, "Adiabatic carry look-ahead adder with efficient power clock generator," *IEEE Proc.-Circuits Devices Syst.*, Vol. 148, No. 5, Oct 2001
- [8] Mohamed Asan Basiri M, Samaresh Chandra Nayak, Noor Mohammad Sk, "Multiplication Acceleration Through Quarter", 978-1-4799-2866-8/14©2014 IEEE

## Author Profile



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