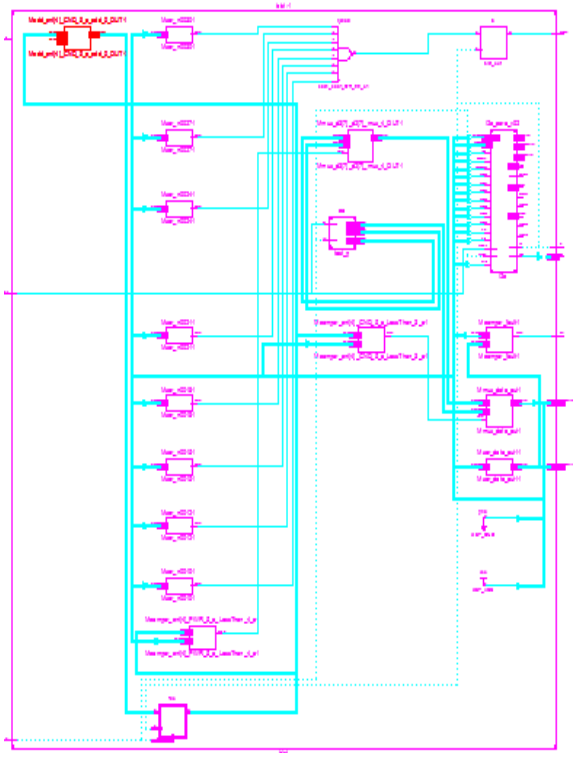

Figure 10: Top level schematics of I2C with BIST capability

Figure 10 shows that schematic of I2C with BIST. There are different blocks in this schematic I2C, BIST, CA, and Comparator.

B. Simulation Results

The timing diagram achieved from Test bencher showed that the received data in the receiver. Then the design is tested in the Xilinx where it also gave the correct output.

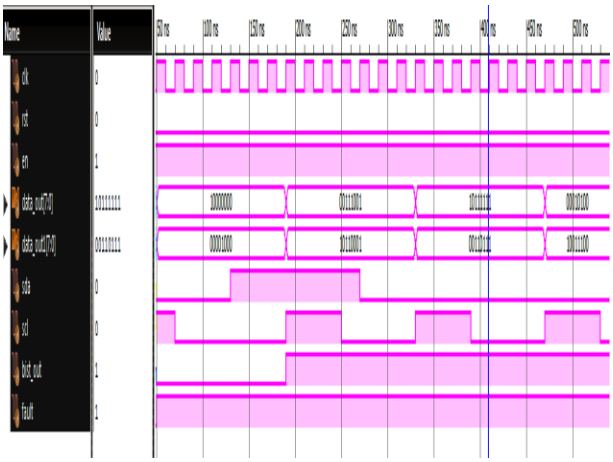

Figure11: I2C with BIST with Fault

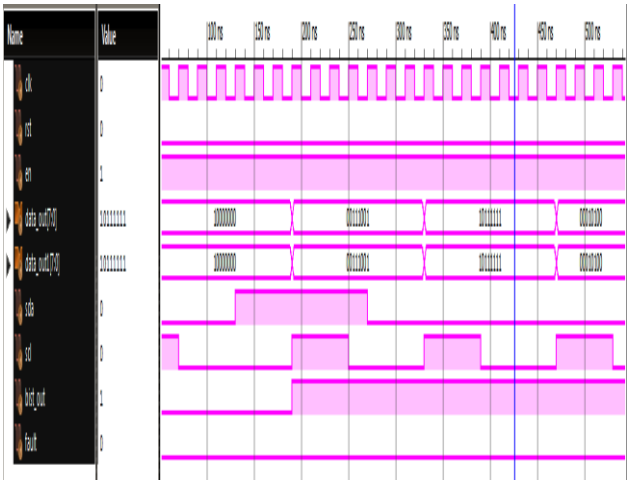

Figure 12: I2C with BIST without Fault

The Device utilization summary and timing summary are given in Table IV and Table V respectively. From the table it is seen that only 25% if the flip flops are used. In case of inputoutput buffers it is 21%. The Number of slice LUTs is only5% and the Number of fully used LUTs FF pair So that, there are many more featherscan be added with the proposed architecture. In the timingsummary, it is seen that the minimum period is 5.03ns whichis much lesser than conventional previous paper.

Table 1: Device Utilization Summary

Name	Used Blocks	Percentages (%)
Number of Slice Flip Flops	39out of 384	0%
Number of slice LUTs	126 out of 2400	5%
Number of fully used LUTs FF pair	34 out of 131	25%
Number of bonded IOBs	22 out of 102	21%
Number of GCLKs	2 out of 16	12%

Table 2: Timing Summary

Parameters	Seconds
Minimum period	5.03ns
Minimum input arrival time before clock	2.972ns
Maximum output required time after	7.302ns

5. Conclusion

In this paper, a Xilinx based implementation of I2C with BIST capability is presented. Here all the modules are designed and simulated with Verilog HDL. Then the system isdownloaded in the Xilinx Spartan-6 FPGA (XC6SLX4). The simple 2-wire serial I2C-bus minimizes interconnections so ICs have fewer pins and there are not so many PCB tracks; result — smaller and less expensive PCBs. Inter integrated circuit is more speedy stable and much more flexible. Built-In Self-Test (BIST), as the name suggests is a technique in which the circuit is capable of testing itself .I2C with BIST capability can gives more proper result at the simulation .It also save valuable time and cost of testing circuits significantly.

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