

3.3 Clock and Data Slider

The CDS consists of one Comma Detector and Data Alignment (CDDA) block, one Dynamic Clock Phase Shifting (DCPS) block, and one Changeable Delay Tuning (CDT) block. As shown in the figure 4. Bit-shift value of RX_data which is given by 'n' and the phase offset ΔP between RXRECCLK and the transmitted clock, satisfy the following equation:

$$\Delta P = n * 360^\circ / N \text{ where } n = 0,1,2,\dots,N-1,\dots,\dots(2)$$

Where, N is the internal data-path width of the GTX transceiver. In our implementation the value of 'N' is 20 bits. The Comma detector and data alignment (CDDA) block is responsible for finding commas, such as the K28.5 symbol (one of 8 b/10 b control characters) , in the parallel received data Data_in. In our implementation, we have included an undefined symbol 'U' as the required comma bit. Once it finds such a comma bit, it can determine the bit-shift value n.

By equation (2), we attain the phase offset ΔP, which might change after each power-up or reset. Based on the phase offset ΔP, the Dynamic clock phase shifting (DCPS) block provides four multi-phase clocks to the Changeable delay tuning (CDT) block. The four clocks, namely Rec_clk,

Rec_clk90, Rec_clk180, and Rec_clk270, have the same frequency as RXRECCLK. Their output phases relative to RXRECCLK are ΔP, ΔP+90°, ΔP+180° and ΔP+270° respectively. Utilizing the four multi-phase clocks, the CDT block transfers the received parallel data Data_in from the RXRECCLK clock domain to the Rec_clk clock domain.

3.3.1 Comma Detector and Data Alignment

The simplified structure of CDDA is as shown in Figure 5. The bit-shift value can be extracted from Data_in. The output of CDDA consists of partial bits of Data_in and partial bits of Data_in's delay register, namely RXDATA_DLY. The bit_shift value decides how to combine the two data sources.

The CDDA block is responsible for finding commas as explained above. In the parallel received data Data_in, it locates a comma bit, later from this we find out the bit-shift value n. By using equation (2), we can obtain the phase offset ΔP , which might change after each power-up or reset. Four possible bit-shift values between the received data Data_in and TXDATA correspond to four possible phase offsets between RXRECCLK and the transmitted clock. The CDDA block also achieves the realignment for received Data_in. From now onwards we mention Data_in as RXDATA in further sections.

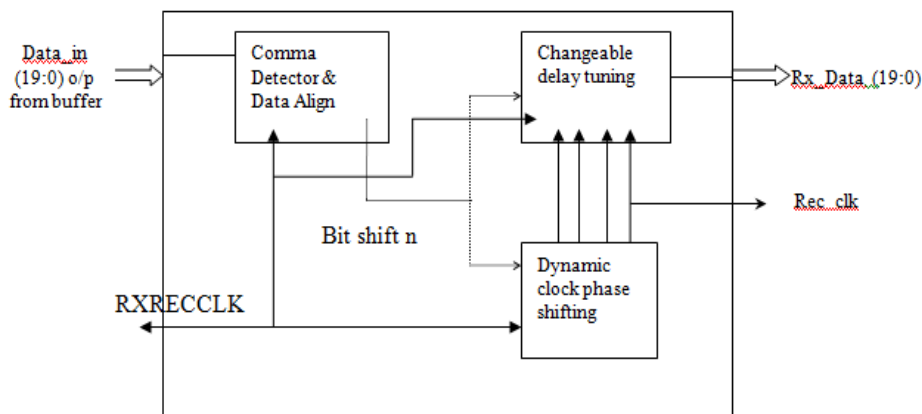


Figure 4 Block diagram of Clock and data slider block at the receiver end.

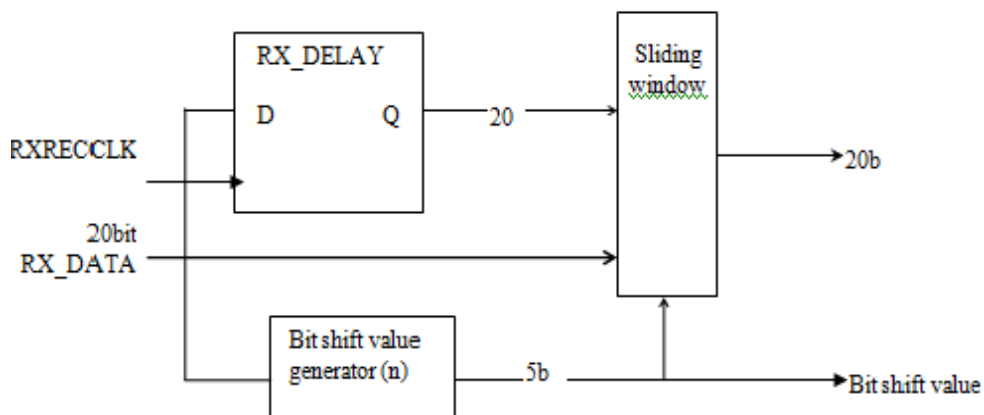


Figure.5 Structure of the Comma Detector and Data Alignment block

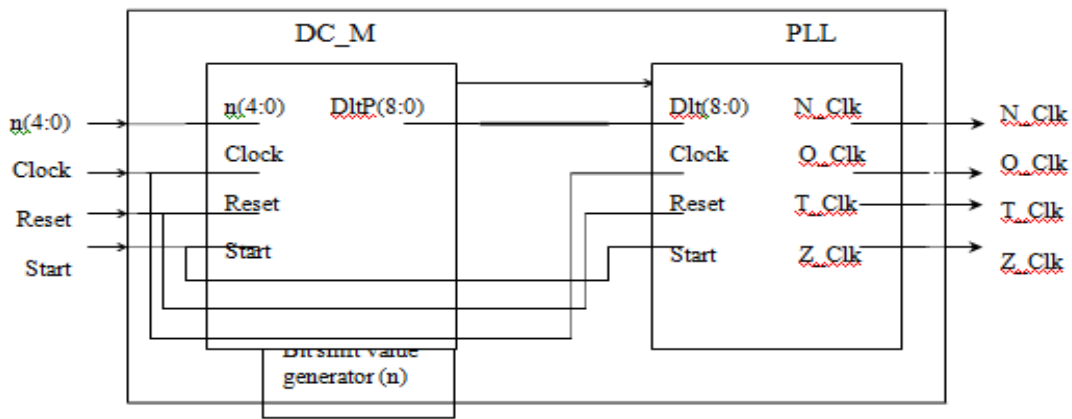


Figure. 6 Structure of the Dynamic Clock Phase Shifting block

3.3.2 Dynamic Clock Phase Shifting Block

A Digital Clock Manager (DCM), a Phase-Locked Loop (PLL), and a Phase Shift Control Unit are used to construct the DCPS block, as shown in Fig. 5. The DCM provides coarse and fine-grained phase shifting. When fine-grained phase shifting is activated, all the output clocks of the DCM are adjusted, so we can further extend the phase-shift range by using the CLK180 output of the DCM. The PLL provides coarse-grained phase shifting. The CLK0, CLK90, CLK180, and CLK270 output clocks of the PLL are each phase-shifted by a quarter of the input clock period relative to each other.

The Phase Shift Control Unit enables the DCM to execute the phase-shifting function. It operates based on the following two steps:

- 1) It first resets the DCM and waits for the DCM to relock. So, the phase-shift value P is 0 ns.
- 2) If $\Delta P \leq 180^\circ$, the phase of the CLK0 output clock of the DCM is incremented from 0° to ΔP and it is chosen as the input clock of PLL. If $\Delta P > 180^\circ$, the phase of the CLK0 output clock of the DCM is incremented from 0 to $(180^\circ - \Delta P)$, and the CLK180 output clock of the DCM is chosen as the input clock of PLL. The CLK_SEL signal, driven by the Phase-Shift Control Unit, performs a selection between the two input clocks of PLL

3.3.3 Changeable Delay Tuning Block

The CDT block consists of a Comma Comparator, a Delay Tuning Unit, and an asynchronous FIFO, as shown in Fig. 6. In Comma Comparator, the parallel input data realigned by the CDDA block is compared to a constant predefined comma character. The Delay Tuning unit consists of four parallel independent delay units and one multiplexer. Each delay unit is composed of two or three cascaded registers. The bit-shift value is used as the select signal for the multiplexer, which performs a selection among the four delay units. The asynchronous FIFO bridges the RXRECCLK clock domain and the Rec_clk clock domain

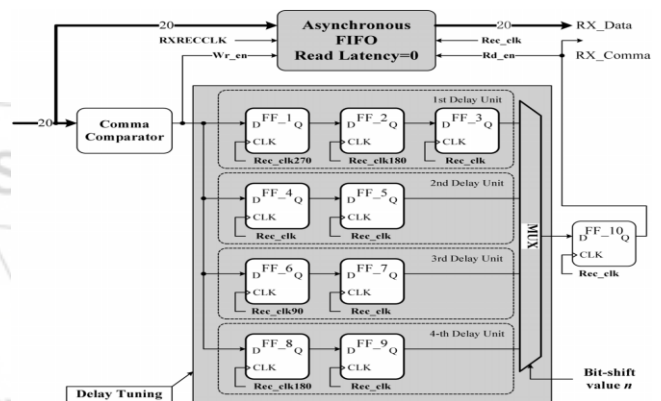


Figure 7: Structure of the Changeable delay tuning block

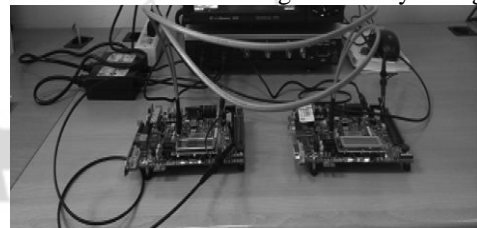


Figure 8: Test platform for our serial transceiver.

4. Experimental Results

The simulation result in figure 9 shows the various latencies in received data at different phase offsets. Here, we have generated four different phase clocks they are 0° , 90° , 180° and 270° . The received data at phase shifted clocks is bit shifted. As we can observe from the figure that at 270° the data is shifted by 3 bits, at 180° data is shifted by 2 bits similarly at 90° it is shifted by single bit but we receive unchanged data at 0° clock. The simulation result in figure 10 shows the complete fixed latency serial transceiver output deserialization. After this it is fed to the CDS block. In CDS block the clock shifting and data alignment is achieved hence the output at the receiver after decoding is Rx_out = 1100110011001100 and appropriate Rec_clk as output.

5. Conclusion

Our solution can process all the possible clock phase offsets, so the transmitter and receiver need not use the same reference clock. Utilizing the external circuit to perform the clock phase-shift and data bit-shift, our solution reduces the dependence on the transceiver architecture.

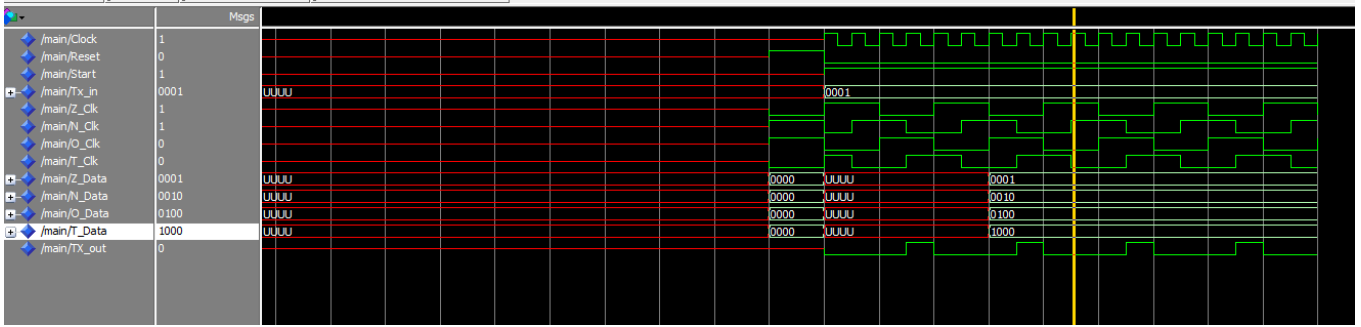


Figure 9: The above simulation result shows that phase offset results in data latency.

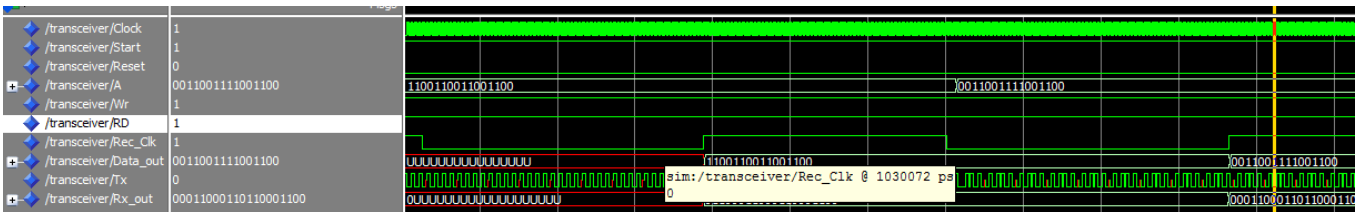


Figure 10: The above simulation result shows the complete transceiver out.

References

- [1] SCAN25100 24576, 1228.8, and 614.4 Mbps CPRI SerDes with Auto RE Sync and Precision Delay Calibration Measurement, Texas Instruments, 2013.
- [2] TLK2711 A 1.6 TO 2.7 GBPS TRANSCEIVER, Texas Instruments, 2012 [Online].
- [3] B. G. Taylor, "TTC Distribution for LHC Detectors," *IEEE Trans. Nucl. Sci.*, vol. 45, no. 3, pp. 821–828, Jun. 1998.
- [4] P. Moreira, A. Marchioro, and K. Kloukinas, "The GBT, a Proposed Architecture for Multi-Gb/s Data Transmission in High Energy Physics," in *Proc. Topical Workshop Electron. Particle Physics Prague*, Czech Republic, Sep. 3–7, 2007.
- [5] White Rabbit [Online]. Available: <http://ohwr.org/projects/whiterabbit/documents>
- [6] F. Lemke, D. Slognat, N. Burkhardt, and U. Bruening, "A Unified DAQ Interconnection network with precise time synchronization," *IEEE Trans. Nucl. Sci.*, vol. 57, no. 2, pp. 412–418, Apr. 2010.
- [7] R. J. Aliaga, J. M. Monzo, M. Spaggiari, N. Ferrando, R. Gadea, and R. J. Colom, "PET system synchronization and timing resolution using high-speed data links," *IEEE Trans. Nucl. Sci.*, vol. 58, no. 4, pp. 1596–1605, Aug. 2011.
- [8] H. Le Provost, Y. Moudou, and S. Anvar *et al.*, "A readout system-on chip for a cubic kilometer submarine neutrino telescope," *J. Inst.*, vol. 6, no. 12, p. C12044, Dec. 2011
- [9] P. P. M. Jansweijer and H. Z. Peek, Measure Propagation Delay Over a 1.25 Gbps Bidirectional Data Link, Tech. Rep. ETR 2010-01, 2010 [Online]. Available: <http://www.nikhef.nl/pub/services/biblio/technical-reports/ETR2010-01.pdf>
- [10] A. Aloisio, F. Cevenini, R. Giordano, and V. Izzo, "High-speed, fixed-latency serial links with FPGAs for synchronous transfers," *IEEE Trans. Nucl. Sci.*, vol. 56, no. 5, pp. 2864–2873, Oct. 2009.