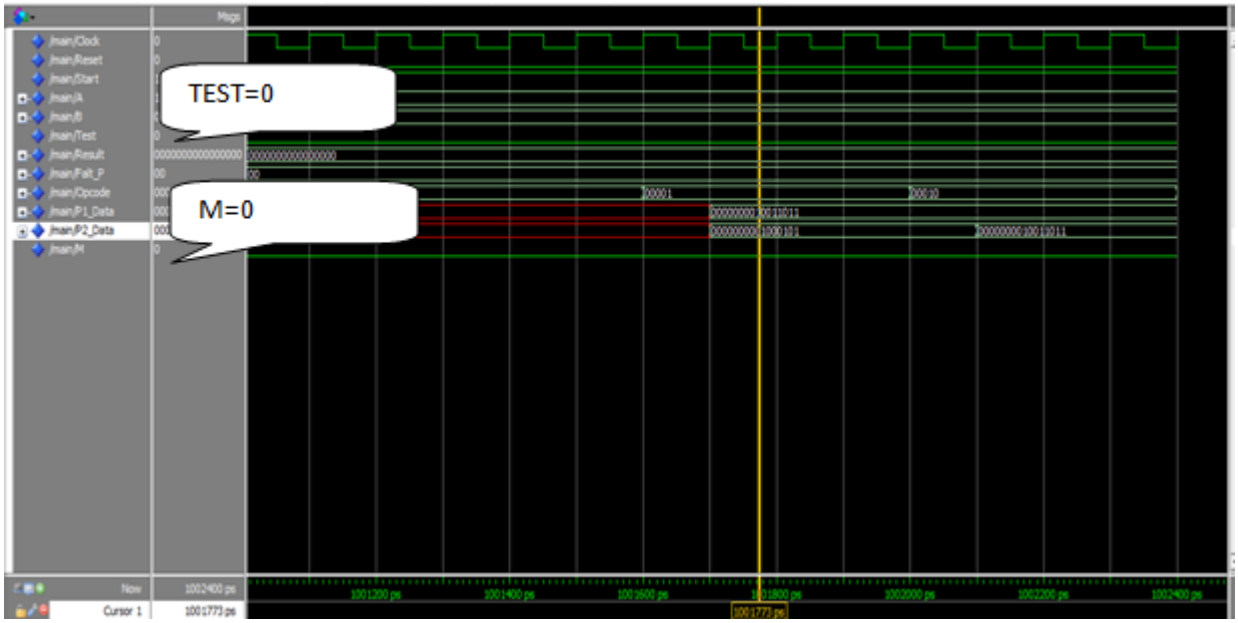

Figure 3.1: simulation result when MIHST is off

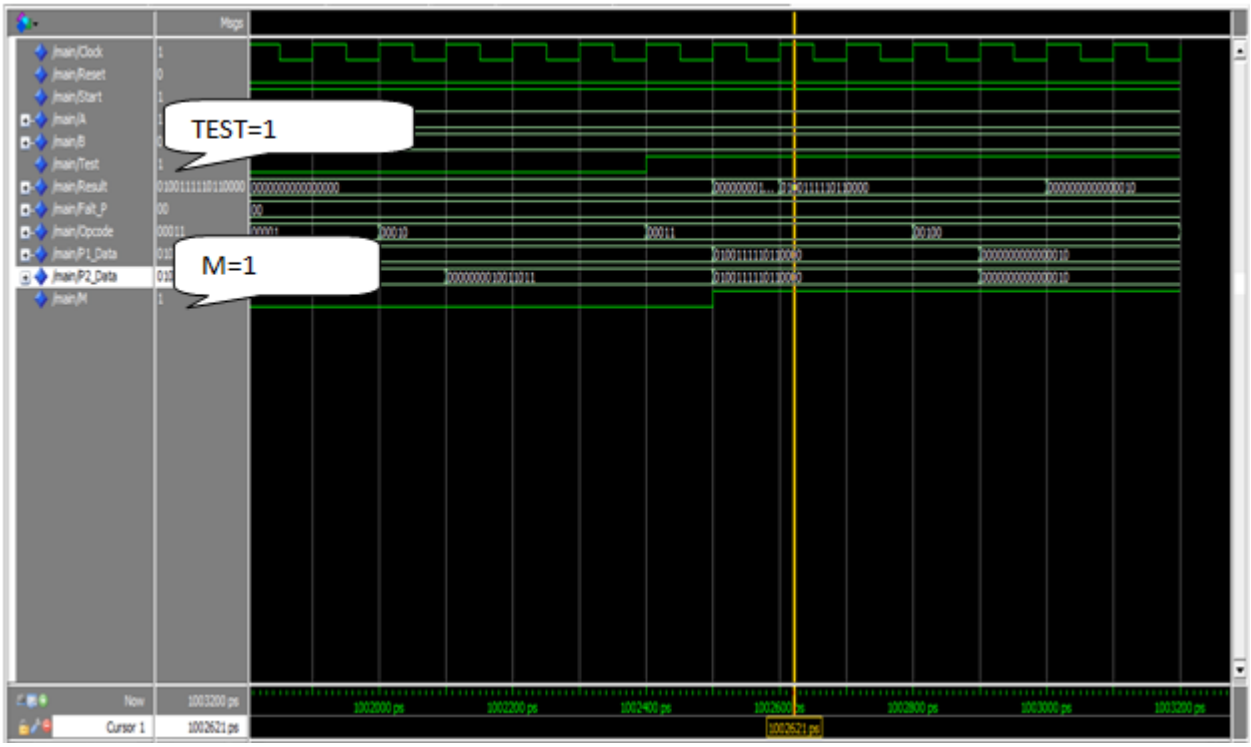

Figure 3.2: simulation result when MIHST unit is ON

The above fig3.2 shows the simulation results when test unit is ON, it is indicated by the TEST signal. When all the input signal are provided with TEST signal as '1' then MIHST unit is ON both the processor runs and testing mechanism is carried out. for example show in fig 5.2.1 the inputs are clock, reset and start signal which are provided by the appropriate values and two operands values A and B are provided by user in above case we took A=11100011 and B=01101100.As a result both the processor and testing mechanism is carried out. The output of both processor is compared with the testing unit results, by which we come to know which processor has fault which is indicated by the signal fault_p.If this signal is '0' means no is both the processor, if its '1' then there is fault in the processor. The operation of processor depends on the opcode generated by testing unit which is 5bit so we can test 32 instructions.

When opcode is 00001 addition operation is carried out in both of the processors named P1 and P2.The results of both the processor is compared with the testing unit, which in turn indicate which of the processor has fault which is shown by signal FALT_P signal.
00-indicates both the processors are faultless
01-indicates processor P1 has fault
10-indicates processor P2 has fault
11-indicates both the processors are fault

As our proposed approach has same fault coverage as SBST technique by it has less application time and test program size. The experimental result is shown below in the table format.

Table 1: Comparison of MIHST unit and SBST approach

	MIHST approach	SBST approach
Execution Time (secs)	7.36	9.43
Test Program Size (kilobytes)	193996	200140

4. Conclusion

The project proposes a new method which is based on the introduction of a special hardware module used for generating the instruction required for the test, which are stored in internal memory. Several advantages we come across when we compare proposed model with the SBST approach, while covering same fault coverage. The cost of insertion of the MIHST unit is limited. Experimental result is carried out on the two processors and the fault is identified that the new method achieving the same fault coverage as SBST with reduced test execution time and less usage of system memory. Currently, work is going on regarding developing MIHST unit which can be able to support the adoption of this method to a wider number of processors.

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