International Journal of Science and Research (IJSR)
ISSN (Online): 2319-7064
Index Copernicus Value (2013): 6.14 | Impact Factor (2013): 4.438

Sobel Edge Detection implementation using FPGA

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Abstract: ***Edge detection is an important tool in digital image processing applications for extracting information from image. Sobel operator based edge detection algorithm creates an image which highlights edges and transitions. In real-time image processing applications, it is required to process large data of pixels in a given timing constraints. Hence, speed of image processing is a big problem. Reconfigurable device like FPGAs deploy parallelism techniques in image processing algorithms thereby reducing execution times and increasing speed of operation. This paper presents implementation of sobel edge detection algorithm on FPGA. Xilinx ISE Design Suite-14.2 software platform is used to design an algorithm using Verilog language.***

Keywords: edge detection, sobel operator, gradient, FPGA

1. Introduction

Digital image processing is widely used for image processing operations like feature extraction, segmentation, pattern recognition, etc. Edge detection, within image processing, is a basic tool used to obtain information from the frame for feature extraction and object segmentation. The purpose of edge detection is to reduce the amount of data in an image significantly and to preserve the structural properties for further image processing. The image is defined in spatial domain. Edge detection technique divides this domain into meaningful parts or regions. In terms of digital image processing, edge is a collection of pixels. Edges characterize boundaries and are therefore a problem of fundamental importance in image processing. Edges typically occur on the boundary between two different regions in an image. Edge detection allows user to observe those features of an image where brightness of image area changes significantly, indicating the end of one region in the image and the beginning of another. Many edge detection techniques have been developed for extracting edges from digital images. Sobel edge detection operator is insensitive to noise and the masks of sobel operator are relatively small. Thus, this operator is used. Sobel edge detection is gradient based edge detection method used to find edge pixels in image.

In early processes, the edge detection was mainly performed on software due to its large hardware requirement. But today's researches on programmable devices make it possible to implement edge detection algorithms on these devices. Design turn-around time of these devices varies from few hours to few days. During the recent years, Field programmable gate arrays (FPGAs) have become the dominant form of programmable logic device [5]. In comparison to previous programmable devices like programmable array logic (PAL) and complex programmable logic devices (CPLDs), FPGAs can implement far larger logic functions. FPGAs are reconfigurable, that is, they have the ability of changing functionality of the device. Gate array is basic internal architecture that makes re-programming possible. This increases flexibility of the device. FPGAs are parallel in nature and they have high computational density compared to other commercially available platforms such as general purpose microprocessors, DSPs. Therefore, the application of FPGAs in image processing has large impact on image or video processing. Also, image or video processing often requires large memory to handle video data stream, image processing, which increase the complexity of hardware and software. DSP or microprocessor solution may increase system greatly. Thus, FPGA is a better solution. Hence, this paper presents implementation of sobel edge detection algorithm on FPGA.

2. Sobel Edge Detction

Edge detection uses differential operators and detects changes in the gradients of the gray levels [3]. It is divided into two main categories:

1. First order edge detector/ Gradient based operator
2. Second order edge detector/Laplacian based operator

Sobel is first order or gradient based edge operator. It performs a 2-D spatial gradient measurement on an image. Sobel is a discrete differentiation operator and it is used to compute an approximate absolute gradient magnitude at each pixel of an image for edge detection. Sobel operator has two masks, one mask finds out horizontal edges and other mask finds out vertical edges. This operator uses a pair of 3×3 kernels which are convolved with the original image to calculate approximations of the derivatives. One kernel is the other rotated by 90 degree as shown in Figure-1. Gx is designed to respond to edges running horizontally and Gy is designed to respond to edges running vertically. The direction and the strength of the edge at a particular location in the image can be computed by using the gradients Gx and Gy. These resulting gradient approximations can then be combined together to give absolute gradient magnitude at each point in the image.

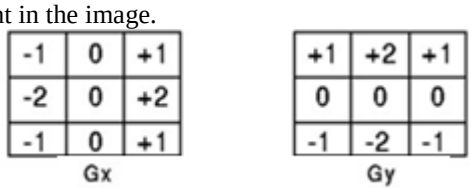

Figure 1: Sobel masks

The magnitude of gradient is calculated as:

$$|G|=\sqrt{G_x{}^2 + G_y{}^2} \quad (1)$$

The angle of orientation of the edge is given by:

$$\theta = \arctan(G_y / G_x) \quad (2)$$

In this case, orientation 0 is taken to mean that the direction of maximum contrast from black to white runs from left to right on the image, and other angles are measured anti-clockwise from this. Figure-2 shows the labeling of neighborhood pixels.

a_0	a_1	a_2
a_7	[i , j]	a_3
a_6	a_5	a_4

Figure 2: Labeling of neighborhood pixels.

For pixel [i,j], partial derivatives gx and gy can be computed using equations (3) and (4) [6].

$$g_x = (a_0 + ca_1 + a_2) - (a_6 + ca_5 + a_4) \quad (3)$$

$$g_y = (a_2 + ca_3 + a_4) - (a_0 + ca_7 + a_6) \quad (4)$$

Where, constant c=2.

Flowchart for sobel edge detection is shown in Figure-3.

3. Implementation of Sobel Edge Detection Algorithm

This paper proposes implementation of edge detection using sobel operator, with the help of verilog hardware description language. An image is taken as an input. If this input image is colored, then firstly, this RGB image is converted to grayscale image with the help of MATLAB R2013a. This image is very large, thus it is resized. Then this image is written into a text file and value of every pixel in an image is obtained.

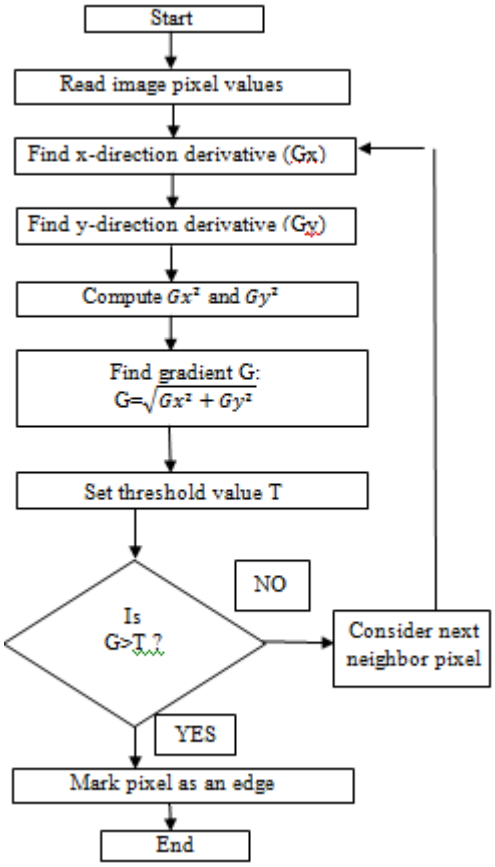

Figure 3: Flow chart of sobel edge detection

Further implementation is done in Xilinx ISE design suite. With the help of Xilinx ISE, text file generated by MATLAB is read. Gradients (Gx and Gy) and their magnitudes are calculated in verilog HDL synthesis. By implementing square root function in verilog, resulting gradient (G) is obtained. After synthesizing the code in verilog, it is simulated and its timing analysis is done. Process flow of edge detection is shown in Figure-4.

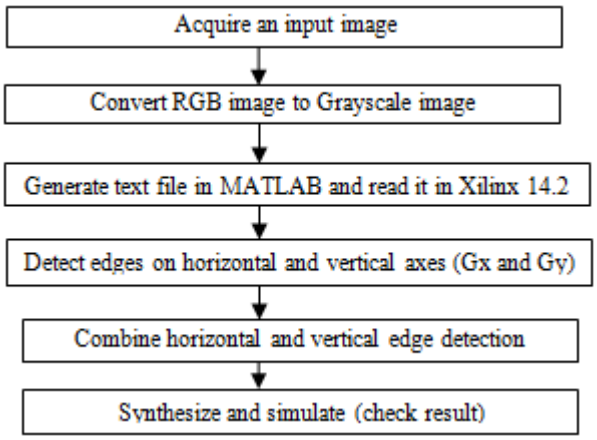

Figure 4: Process flow of edge detection

4. Results

A colored image is given as an input to MATLAB. This image is shown in Figure-5. As shown in process flow, image is first converted from RGB to gray. This reduces amount of data in image. Result of RGB to gray conversion is shown in Figure-6. Text file generated using MATLAB is shown in Figure-7.

Figure 5: A colored input image

Figure 6: RGB to gray converted image

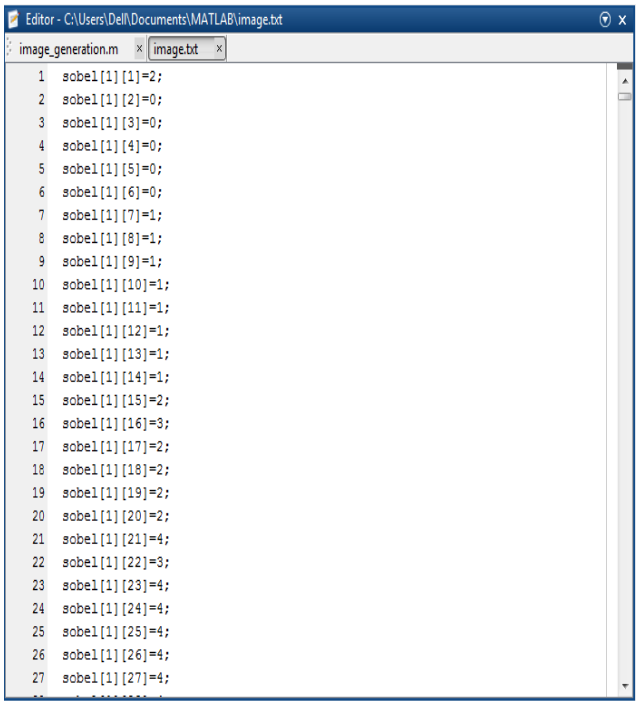

Figure 7: Text file

Code for sobel edge detection is written in verilog and it is synthesized and simulated using Xilinx ISE 14.2. Simulation result of edge detection is shown in Figure-8.

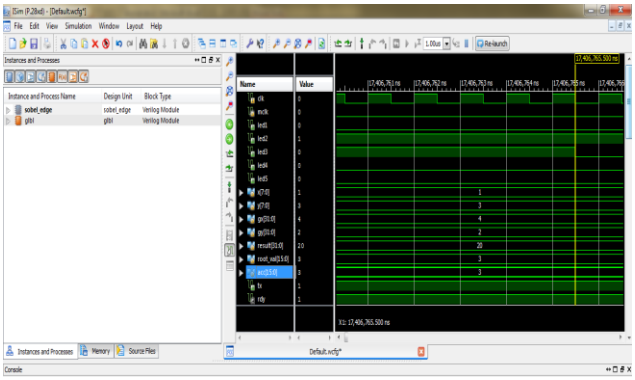

Figure 8: Simulation result

g_x and g_y are gradients calculated at location (x,y). At negative edge of clock (mclk), root_val gives resulting gradient (G) at location (x-1, y-1), which is sent to terminal window from FPGA using serial communication.

Code is implemented using FPGA Spartan 6, device XC6SLX45, package CSG484; working at 100MHz. Utilization of FPGA hardware resources is shown in table-1.

Table 1: Device utilization summary

Slice Logic Utilization	Used	Available	Utilization
Number of Slice Registers	411	54,576	1%
Number of used Flip Flops	358		
Number of Slice LUT's	7,444	27,288	27%
Number of bonded IOBs	7	320	2%

Values of gradient (G) are displayed on terminal window, in ASCII form, as shown in Figure-9.

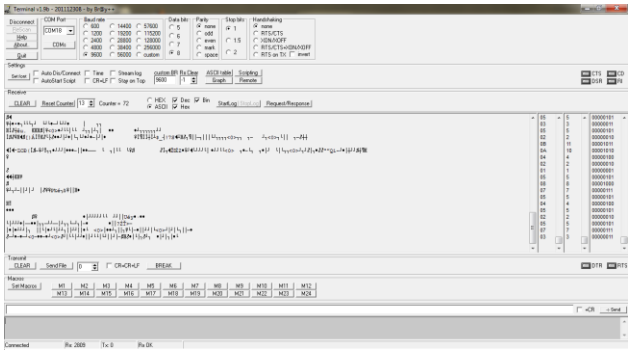

Figure 9: Result on terminal window

5. Conclusion and Future Scope

This paper presented FPGA based sobel edge detection. Sobel edge detection algorithm is chosen because it has less deterioration at high levels of noise. Parallel nature of FPGA reduces processing time and increases speed. Algorithm for sobel edge detection is coded using verilog HDL.

This algorithm can be used in various image processing applications such as in medical imaging, video surveillance. It can also be used in lane departure warning system to detect edges of lanes.

Pipelined sobel edge detection algorithm can be used in future to improve speed. This will be helpful for high speed applications.

References

[1] Chaple G., Daruwala R.D., "Design of Sobel operator based image edge detection algorithm on FPGA" International Conference on Communications and Signal Processing (ICCSP), pp 788 – 792, 3-5 April 2014.
[2] Vanishree, Reddy K.V.R., "Implementation of pipelined sobel edge detection algorithm on FPGA for High speed applications" , International Conference on Emerging Trends in Communication, Control, Signal Processing & Computing Applications (C2SPCA), pp 1 – 5, 10-11 Oct. 2013.
[3] Rashmi, Mukesh Kumar, and Rohini Saxena "Algorithm and technique on various edge detection: A survey" Signal & Image Processing: An International Journal (SIPIJ) Vol.4, No.3, June 2013
[4] Alghurair D., Al-Rawi, S.S., "Design of Sobel operator using Field Programmable Gate Arrays", International Conference on Technological Advances in Electrical, Electronics and Computer Engineering (TAEECE), pp 589 – 594, 9-11 May 2013.
[5] G. Anusha, Dr.T. JayaChandra Prasad, Dr.D. Satya Narayana , "Implementation of SOBEL Edge Detection on FPGA" International Journal of Computer Trends and Technology, vol3,Issue-3,2012.
[6] G.T. Shrivakshan, Dr.C. Chandrasekar, "A Comparison of various Edge Detection Techniques used in Image Processing" International Journal of Computer Science Issues (IJCSI), Vol. 9, Issue 5, No 1, September 2012.
[7] Varun Sanduja, Rajeev Patia, "Sobel Edge Detection using Parallel Architecture based on FPGA"

International Journal of Applied Information Systems (IJAIS), vol 3, no.4, July 2012.

[8] Zhegyang, Zhilehi Chai , "Image Edge Detection Based on FPGA " Ninth International Symposium on Distributed Computing and Applications to Business Engineering and Science (DCABES), pp 169 – 171, 10-12 Aug. 2010.