International Journal of Science and Research (IJSR)
ISSN (Online): 2319-7064
Index Copernicus Value (2013): 6.14 | Impact Factor (2013): 4.438

Design and Implementation of Low Power 32 bit Reversible Carry Skip Adder

Rewati D. Gatfane[1], Manisha Waje[2]

[1]Department of E & Tc, G. H. Raisoni College of Engineering and Mangement, Wagholi, Pune, India.

[2] Professor, Department of E & Tc, G. H. Raisoni College of Engineering and Mangement, Wagholi, Pune, India.

Abstract: ***In emerging nanotechnology, new reversible logic appears to be promising due to its wide application in emerging technologies. Reversible logic has many other applications on quantum computing, DNA computing, molecular computing, optical computing, quantum dot cellular automata, DSP application etc. In this paper, low power 32 bit Carry Skip Adder is proposed using reversible logic to reduce the transistor overhead. MTSG gate, Toffoli gate, Fredkin gate is used to design proposed the carry skip adder. The structural functionality of the 32 bit carry skip adder is verified using Digital Schematic Editor and Simulation, Microwind software. After comparing the performance analysis of 32 bit CSA using MTSG gate is efficient than other carry skip adder.***

Keywords: Reversible logic, Reversible basis gates, Garbage output, Quantum computing, Carry skip adder.

1. Introduction

Reversible computation can be performed only by reversible gate in the system. Reversible logic belong to the conservative logic family which exhibits the relation of equal number of 1's in the output as there are in the input. The conservative logic is not reversible in nature, still all the gates in reversible logic has one to one mapping between the input and output vectors so that results in the property that there are equal number of 1's in the output as in the input.

In reversible circuit the amount of heat dissipation is kTln2 Joule for every bit of information loss, where k is Boltzmann constant and t is the operating temperature. Launder proved that heat dissipation (power dissipation) for 1 bit information loss is at least kTln2 during any computation. Later in 1973 C. H. Bennett come with the idea that launder's theory is only for irreversible logic but for any reversible logic model power dissipation or heat dissipation in any device can be made zero.

A. Properties of reversible logic gates

1. Reversible logic performs unitary operation.
2. Reversible gate must have one to one mapping between input and output vectors, there exhibits relation Iv↔Ov.
3. Reversible circuit design using minimum number of reversible gates.
4. Quantum cost of the circuit is the cost of the circuit, in term of the cost of primitive gate. The cost of 1x1 gate is 0 and 2x2 gate is 1.
5. Garbage output: The gate output that is generated by directly passing the input should not be considered as garbage as the output can be easily measured from the input port and vice versa.

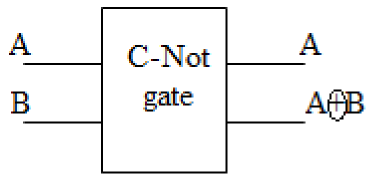
B. Limitation of reversible gates

1. Fan-out is not permitted.
2. Loops are not allowed.

C. Basic reversible gates

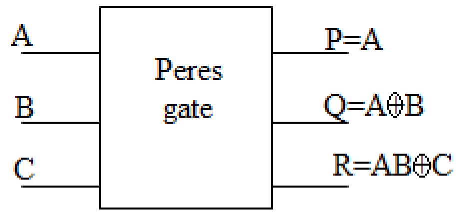
1. C-Not gate

This gate is called as controlled Not Gate. C- Not gate is acts as fanout by keeping b=0. It is 2x2 gate because of two input and two output.



2. Peres gate

Single Peres gate can implement logic operation such as AND, X-OR, NAND etc. double Peres gate can be use as full adder. It is 3x3 reversible gate i.e. input triple is associated with output triple.

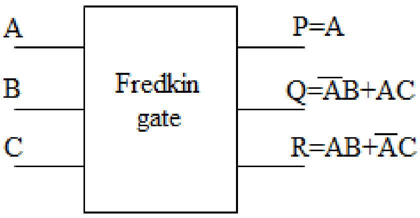


3. Fredkin gate

It acts as a parity preserving gate. This reversible gate is introduced by Petri. It has forward computation and backward computation as follow

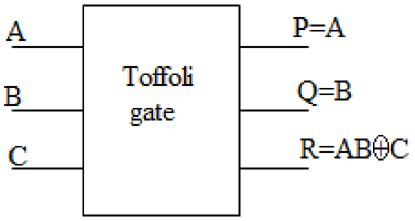
Forward computation
P=A
If A=0 then Q=B and R=C
Else Q=C and R=B

Backward computation
A=P
If P=0 then B=Q and C=R
Else C=Q and B=R



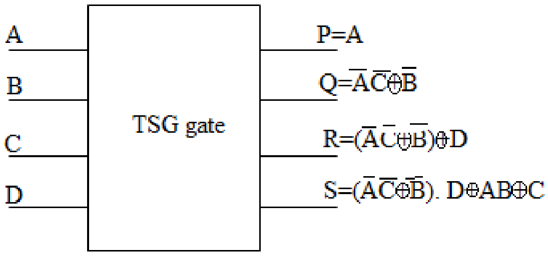
4. Toffoli gate

Toffoli gate is also used as AND, X-OR etc. Here the output P and Q are directly generated by hand wiring. Toffoli gate has forward computation and backward computation.

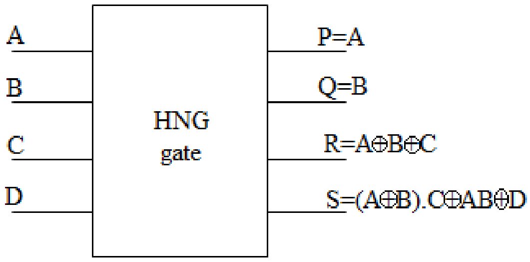


Following gates acts as reversible full adder. Use to design various reversible circuits.

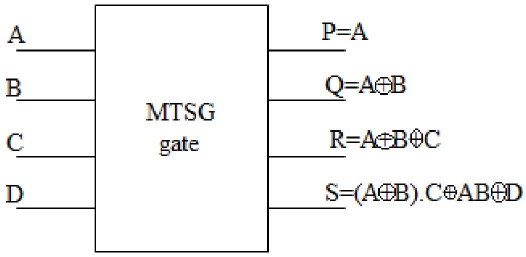
5. TSG gate



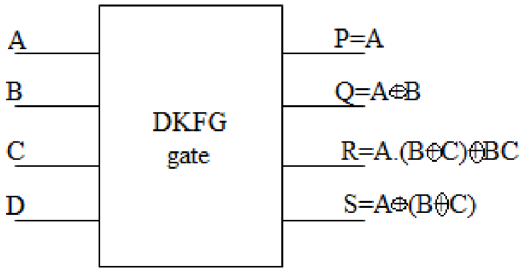
6. HNG gate



7. MTSG gate



8. DKFG gate



2. Proposed 32 bit Carry Skip Adder

The new reversible 32 bit Carry Skip Adder (CSA) is optimizing transistor realization block diagram shown in fig 3.1. Block diagram is give for 4 bit, this can be converts to 32 bit. Consider eight block of 4 bit CAS, Cout of every 4 bit carry skip adder is given to next carry skip adder. 32 bit input is applied by making eight 4 bit block of MTSG gate. This 32 bit CSA design using MTSG gate which itself act as reversible full adder. To design CSA other two kind of reversible gate is used they are fredkin gate and toffoli gate. These gates are reliable gate which gives best result in constant input, garbage output and with number of transistor used. Using these fredkin gate and toffoli gate two more 32 bit CSA is design in which different reversible full adder is used they are HNG gate and DKFG gate.

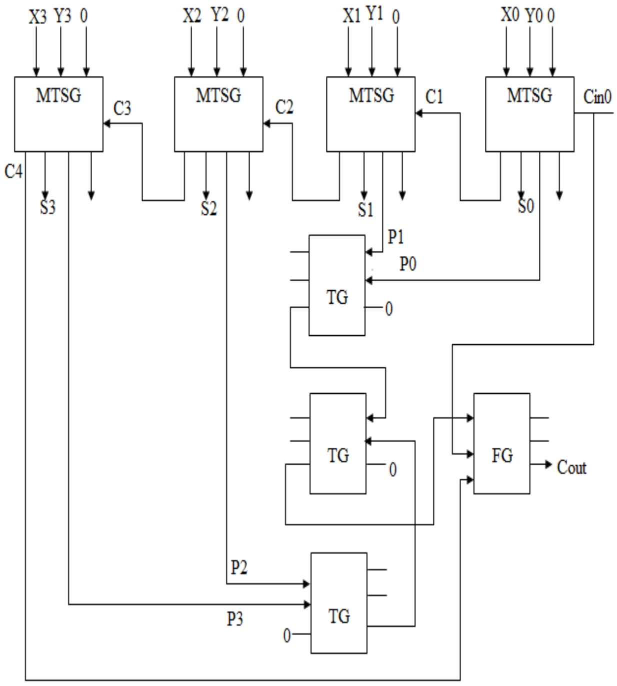


Figure 3.1: block diagram of 4 bit carry skip adder

3. Experimental Results

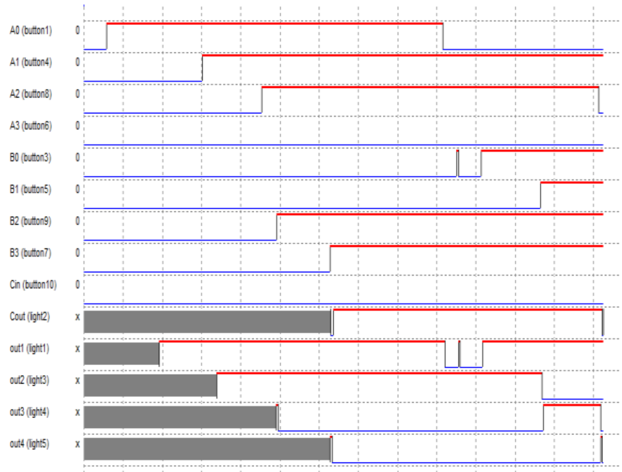


Figure 4.1 Timing diagram of 4 bit CSA using MTSG gate

32 bit CSA is compared with three carry skip adder designed using HNG gate, TSG gate, DKFG gate. The comparison is made on transistor realisation and also the garbage output, constant input, number of reversible gate is given. Less transistor use to design the circuit leads to low power; it means number of transistor decrease power required is decrease. And another parameter delay is also depended on the circuit length indirectly the number of transistor used. Table 4.1 and table 4.2 shows the comparative results of 4 bit and 32 bit CSA respectively. The transistor used for CSA using MTSG gate is less compared to other three CSA. The number of transistor in 4 bit CSA makes the huge difference in 32 bit CSA.

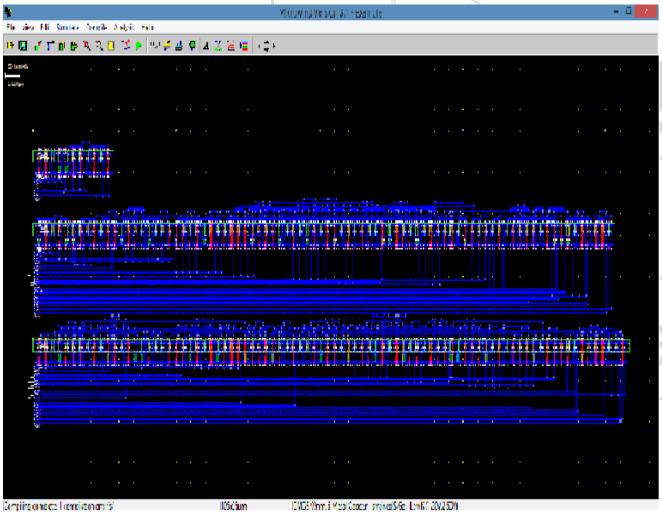


Figure 4.1: Layout design of 32 bit CSA using MTSG gate

Table 4.1Comparative experimental result of different 4 bit CAS adder

	MTSG proposed	TSG	HNG	DKFG
Constant input	7	7	7	7
Garbage output	1	1	1	4
Number of reversible gate	8	8	8	8
Number of transistor in circuit	81	85	97	107

Table 4.2: Comparative experimental result of different 32 bit CAS adder

	MTSG proposed	TSG	HNG	DKFG
Constant input	56	56	56	56
Garbage output	8	8	8	32
Number of reversible gate	64	64	64	64
Number of transistor in circuit	648	680	776	856

4. Conclusion

The transistor realisation of carry skip adder using MTSG gate is given. The new 32 bit carry skip adder is given to the computational complexity to avoid transistor over head. Reducing the transistor over head heat dissipation (power dissipation) is also reduced. Result show the number of transistor used for 32 bit CSA using MTSG is 648 while using TSG gate is 680. The difference in the number of transistor used is 32 and with respect to HSG, DKFG gate is 128, 208 respectively.

References

[1] Rakshith Saligram, “Design of Low Logical Cost Conservative Reversible Adders using Novel PCTG”, International Symposium on Electronic System Design, 2013.
[2] Raghava Garipelly, P. Madhu Kiran, “A Review on Reversible Logic Gates and their Implementation”, International Journal of Emerging Technology and Advanced Engineering, Volume 3, Issue 3, March 2013.
[3] Yu Pang, Junchao Wang, “A 16-bit Carry Skip Adder Designed by Reversible Logic”, 5th International Conference on BioMedical Engineering and Informatics, 2012.
[4] Himanshu Thapliyal, A.P Vinod, “Transistor Realization of Reversible TSG Gate and Reversible Adder Architectures”, IEEE Transaction 2006.
[5] Hafiz Md. Hasan babu, Ahsan Raja Chowdharuy “Design of reversible binary coded desimal adder using reversible 4 bit parallel adder.”, IEEE 2005.
[6] J.W. Bruce, M.A. Thornton, L. Shivakumaraiah, P.S. Kokate, and X. Li “Efficient Adder Circuits Based on a Conservative Reversible Logic Gate.”, IEEE 2002.
[7] Syhed Zarreuddin, Ch Sandeep “Implementation of reversible ALU using Koggo-stone adder.” ,IJARECE .
[8] Lafifa Jamal, Md. Shamjusjoha, Hafiz Md. Hasan babu “Design of optimal reversible carry look ahead adder with optimal garbage and quantum cost. ” IJET 2012
[9] V. Kamalakanan, Shilpkala V. , Ravi H. N. “Design of adder/substractor circuit based on reversible gate. ” IJAREEIE 2013
[10] D. P. Bala Subramanium, k. Kalaikaviya, S.Tamilsilvan “Low-Geometry high speed Feynman Toffolic 8 bit carry skip adder”JGREC 2012.
[11] Kunal Das, Debashis De, “Competent Universal Reversible Logic Gate Design for Quantum dot Cellular Automata”, WSEAS Transactions on Circuits and Systems, Issue 12, Volume 11, December 2012.

[12] Behrooz Parhami, “Fault-Tolerant Reversible Circuits”, Proc. 40th Asilomar Conf. Signals, Systems, and Computers, Pacific Grove, CA, October 2006.
[13] Prashanth.N.G, Manojkumar.S.B, “Design and Synthesis of Reversible Fault Tolerant Carry Skip Adder/Subtractor”, International Journal of Emerging Science and Engineering (IJESE) ISSN: 2319–6378, Volume-1, Issue-8, June 2013.
[14] Syed.Zaheeruddin, Ch.Sandeep, “Implementation of Reversible ALU using Kogge-Stone Adder”, International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE) Volume 2, Issue 10, October 2013.