

Low Power PLL with Time Shift Circuit Using Parallel PFD Configuration

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Abstract: In this work a low noise power efficient parallel-PFD PLL is proposed. Parallel circuit configuration improves the SNR of the circuit. The proposed circuit includes delay circuit with 8/9 frequency divider and a 3 stage VCO. For reducing more noise time shifted circuit by using VCO is proposed. The proposed design is simulated using Tanner EDA in 180nm technology. In terms of power consumption, band phase noise the new current comparison domino offers significant improvement compared to existing system.

Keywords: PLL, PFD, DMP.

1. Introduction

Low noise PLL is an active area of research. The phase locked loop has a wide variety of applications. Various applications like applications, such as high level modulation scheme [1] satellite communication [2] and clock generator [3], radar, biomedical instruments require a very low noise performance for their oscillators. Low-jitter low-phase-noise phase-locked loop (PLL) is an essential building block hence obtaining a low noise PLL circuit is a challenging issue.

The output phase noise of the PLL is usually contributed from the phase noises of the voltage-controlled oscillator (VCO), the phase frequency detector (PFD) and the input reference signal. In general, the phase noise of the VCO to the output of the PLL is a high-pass response, while the PFD and reference to the output are a low-pass response. To achieve a low-jitter low-phase-noise PLL, the loop bandwidth should be properly designed [3]. However, the phase noise of the VCO degrades as the operation frequency

Increases toward microwave and MMW bands. Therefore, a wide loop bandwidth can be chosen for suppressing the phase noise of the VCO, but the widest loop bandwidth is usually limited by the input reference frequency due to the consideration of stability.

Distributed Wireless Sensor Networks (WSN) and actuators are emerging as a viable solution for home automation, environment monitoring and many other industrial, healthcare and consumer applications. Three major design considerations in WSN applications are power consumption, volume and costs [4]. Reducing the power-consumption will increase the lifetime and reduce the battery size, resulting in lower volume and costs.

There are several reasons which motivate to design a low power low noise PLL. Critical component to the phase noise of PLL is phase frequency detector (PFD) [5], [6]. Hence this work proposed a method to equate the phases of two inputs to the PFD (F_{ref} and F_{div}) by using a time shifted circuit and using another VCO at the output of LF. It reduces the SNR of PFD by parallelizing the circuit. However generally, the SNR improvement will degrade due to the noise correlation. To avoid the noise correlation of PFDs, the proposed PLL adopt a timing shifted architecture. For a

timing shifted operation of parallelized PFDs, both VCO and reference signal have to be delayed independently. The two inputs to the PFD are maintained independently to obtain the same phase. F_{div} is delayed by using divider circuit and F_{ref} is maintained using a comparator and VCO_{fb} .

2. System Preliminaries

A) PFD and a Charge Pump

The phase frequency detector (PFD) is one of the main parts in PLL circuits. PFD produces an error output signal which is proportional to the phase difference between the phase of the feedback clock and the phase of the reference clock. A PFD as shown in figure (1) is used for this design. The PFD use only 10 transistors, whereas a conventional PFD uses 54 transistors. It has been observed that the PFD could operate up to frequencies about 4.6 times higher than that by conventional PFD.

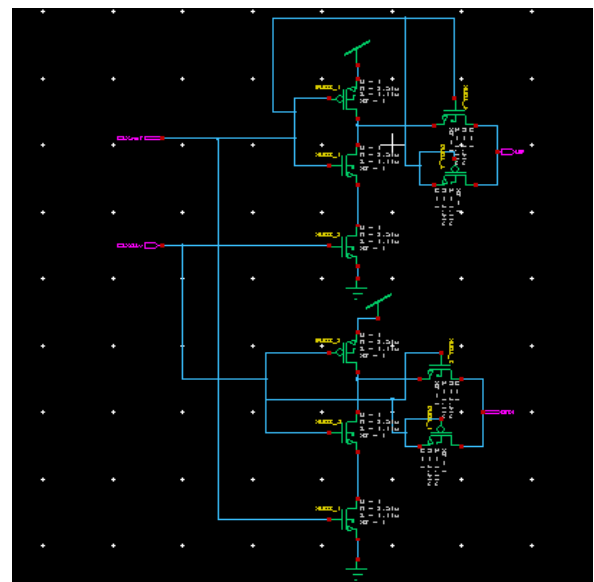


Figure 1: Phase Frequency Detector

The Charge Pump (CP) is another important part of PLL. CP converts the phase or frequency difference information of two input signals into a voltage which is used to tune a Voltage Controlled Oscillator (VCO) toward reference input frequency.

B) Loop Filter

The Loop Filter (LF) is necessary to generate necessary control signals into the VCO and is also necessary to store the charge from the CP. Figure (2) shows the passive filter which is used for this design.

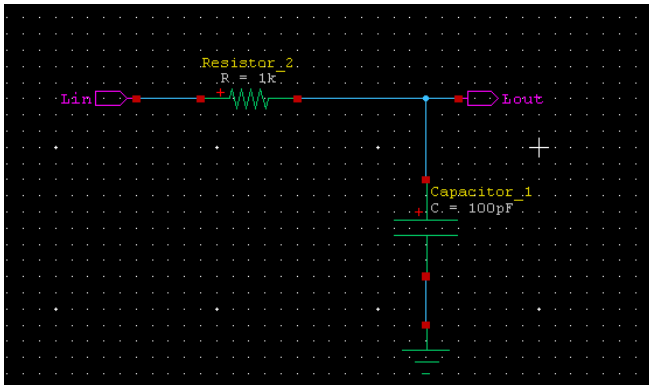


Figure 2: Loop Filter

C) Voltage controll oscillator

Figure 3 shows a 3 stage VCO. The purpose of the VCO is to either speed up or slow down the feedback signal according to the error generated by the PFD, if the PFD generates an up (UP) signal, the VCO speeds up. On the contrary, if a down (DN) signal is generated, the VCO slows down. The output of the VCO is then fed back to the PFD in order to recalculate the phase difference, thereby forming the closed loop frequency control system.

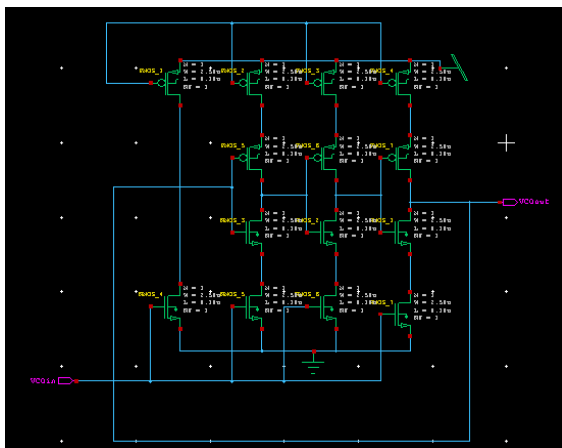


Figure 3: 3-stage VCO

3. System Description

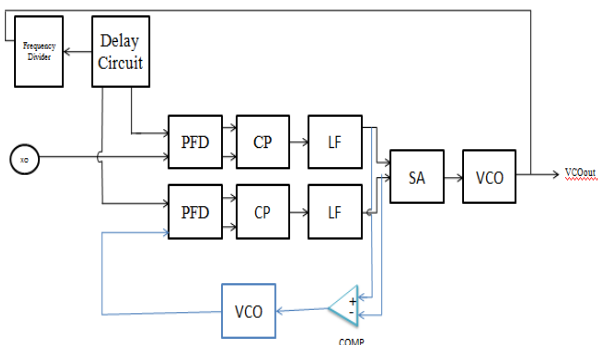


Figure 4: Multi-PFD PLL with time shifted Circuit

Figure 4 shows the proposed architecture of parallel PFD PLL. Two PFD's are parallelized with charge pump and loop filter. The output voltage of loop filter is added by summing amplifier and given to the VCO as control voltage. The PFD detects the rising edges of the input signals, and generates a pulse whose width is a time difference of rising edges of input signals. The pulse width of PFD output should be short from a view point of output noise, because output pulse contains a voltage or current noise. In other words rising edges of two input signals of each PFD must be in same time. For this reason both the inputs to the PFD are delayed independently.

A) Parallel-PFD

Parallelizing n circuits can improve the SNR with a factor n [7]. Therefore, in proposed design by parallelizing the two PFD noise will reduce to 4db. Practically these PFD's are closely placed on the die to avoid the correlation between noises produced by each PFD.

B) Time shifted mode for Division Signal

One of the inputs to the PFD is F_{div} signal. This signal is adjusted by frequency divider and delay circuit in time shifted mode. Frequency divider is composed of 8/9 dual modulus prescaler (DMP) and counter. Time delay is generated by D-Flip Flop (DFF) with the clock of DMP output signal. Therefore the delay time Δt is 8 or 9 times a period of VCO signal. This re-timing by DFF also has an advantageous effect of reducing PLL phase noise, because noise of the counter is cancelled.

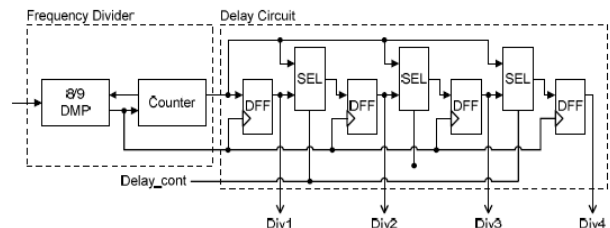


Figure 5: Frequency Divider and delay circuit

Figure 5 shows the frequency divider and delay circuit. This delay circuit has a function to switch the delay mode by a control signal "Delay_cont", for the measurement of the effect of timing shift operation. When "Delay_cont" is logically high, selector (SEL) transfer the upper input signal, then all output signals Div_i has same output timing, this is "in phase mode". In contrast, if "Delay_cont" is logically low, output timing of Div_i and Div_{i+1} has a delay of Δt , which is called "timing-shifted mode". In each case, output edge is determined by the clock of DFF, therefore output signal has a same noise performance, and strict comparison of noise reduction effect of timing-shifted mode is possible.

c) Self adjusting by VCO_{fb} :

Second input to the PFD is F_{ref} . The delay of F_{div} is generated by frequency divider and DFF. But the delay of reference signal cannot be done by DFF, for the delay of reference signal a different method is used. In addition, the delay of reference signal must be equal to the delay of VCO signal as described above.

Reference signal is adjusted by using a comparator and another VCO_{fb} at the feedback of LF. Control voltage to

VCO_{fb} is given by a comparator at the output of LF as shown in fig 4. Manually the phase of reference signal can be adjusted.

4. Simulation Results

Simulation is performed to verify the effectiveness of proposed PLL design,

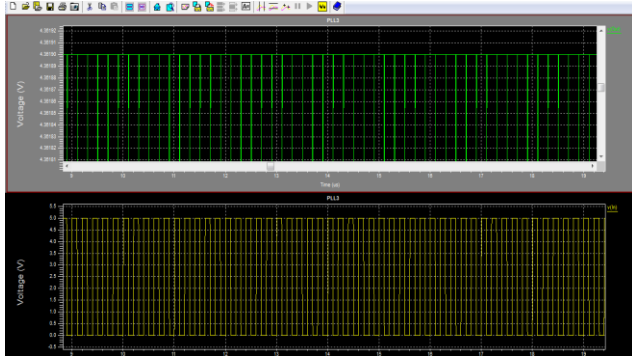


Figure 6: Input output wave form for square wave input

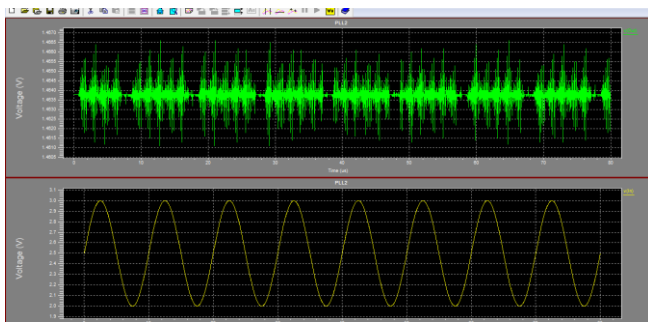


Figure 7: Input output wave form for sine wave input

Figure 6 and figure 7 shows the output of PLL for the two different inputs that is for square wave and sine wave. The simulation is performed on Tanner EDA 14.1 tool using 0.18 μ m integrated circuit.

Table 1: Performance summary of proposed PLL compared with prior published works.

Parameters	Technology			This work
	0.8 μ m HBT	0.13 μ mSiGe BICMOS	0.18 μ mSiGe BICMOS	
Power Consumption (mW)	684	570	720	23
Area (Transistor count)	423	582	454	336
Voltage Supply (V)	1.1,1.5	1.2,2.5,3.3	1.8	1.8
Normalized Noise (dBc/Hz)	-232	-230	-237.7	-238.2

5. Conclusion

There are many applications which require PLL. But the basic problem is phase noise. This project presents a new architecture of PLL with multi-PFD. However, normally the SNR improvement will degrade due to the noise correlation. To avoid the noise correlation of PFDs, the proposed PLL adopt a timing shifted architecture. For a timing shifted

operation of parallelized PFDs, both VCO and reference signal have to be delayed independently. To realize this function, the PLL includes a delay circuit of VCO signal and a mechanism to adjust the phase of reference signal automatically. Also by using this design the power consumption minimized up to 23mW.

References

- [1] D. Murphy, Q. J. Gu, Y. C. Wu, H. Y. Jian, Z. Xu, A. Tang, F. Wang and M. C. F. Chang, "A low phase noise, wideband and compact CMOS PLL for use in a heterodyne 802.15.3c transceiver," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1606–1617, Jul. 2011.
- [2] Z. Xu, Q. J. Gu, Y. C. Wu, H. Y. Jian and M. C. F. Chang, "A 70–78-GHz integrated CMOS frequency synthesizer for band satellite communications," *IEEE Transaction Microwave Theory Technology*, vol. 59, no. 12, pp. 3206–3218, Dec. 2011.
- [3] R. C. H. v. d. Beek, C. S. Vaucher, D. M. W. Leenaerts, E. A. M. Klumperink and B. Nauta, "A 2.5–10-GHz clock multiplier unit with 0.22-ps RMS jitter in standard 0.18-mm CMOS," *IEEE J. Solid-State Circuits*, vol. 39, no. 11, pp. 1862–1872, Nov. 2004
- [4] W. Weber, J. Rabaey and E. Aarts, *Ambient Intelligence*, J. Rabaey, Ed. Springer, 2005.
- [5] X. Gao, E. Klumperink, M. Bohsali and B. Nauta, "A Low Noise Sub Sampling PLL in Which Divider Noise is Eliminated and PD/CP Noise is Not Multiplied by N2," *JSSC*, vol.44, no.12, pp.3253-3263, Jan. 2009.
- [6] S. Kang, J. Dhien, and A. M. Niknejad, "A 100GHz phaselocked loop in 0.13 μ m SiGe-BiCMOS process", *Radio Frequency Integrated Circuit Symposium 2011*, June. 2011.
- [7] E. Klumperink, and B. Nauta, "Systematic comparison of HF CMOS transconductors," *IEEE Transaction Circuits Syst. II, Analog Digital Signal Process*, vol.50, no.10, pp.728-741, Oct. 2003
- [8] X. Gai, G. Liu, S. Chartier, A. Trasser and H. Schumacher, "A PLL with ultra low phase noise for millimeter wave applications," *EuMC 2010*, pp. 69-72, 2010.
- [9] Koji Tsutsumi, Yoshinori Takahashi, Masahiko Komaki, Eiji Taniguchi and Mitsuhiro Shimozawa, "A Low Noise Multi-PFD PLL with Timing Shift Circuit", *IEEE Mitsubishi Electric Corporation*, 5-1-1, Ofuna Kamakura, Kanagawa, 247-8501, Japan, 2012.