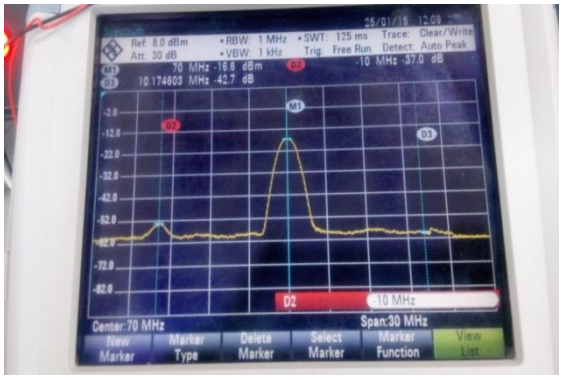

Figure 8: Input data signal without spreading at a rate of 10 Mhz.

The modulated data signal (i.e. spreading of the input data signal) at a rate of 10Mhz is given in below figure 8 and which is observed in power spectrum analyzer.

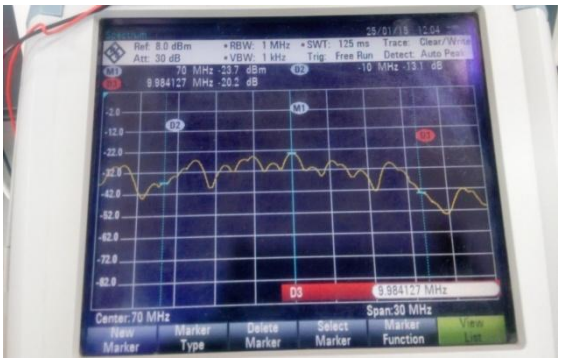

Figure 9: Input data signal without spreading at a rate of 10 Mhz

5. Conclusion

This paper presents the design and FPGA Implementation of Square root raised cosine filter of 29 order. This SRRC filter reduces inter symbol interference by pulse shaping and also reduces channel noise by matched filtering. Shifting and addition method is proposed for designing of square root raised cosine filter.

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