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Area Efficient architecture for 64 bit CSLA using Sum and Carry Generation Unit

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Abstract: ***Design of area efficient data path logic systems are one of the important areas of research to perform arithmetic operations in VLSI design there is a scope for reducing area. The CSLA architecture is simple to design and area-efficient. However, the computation speed is slow because each full-adder can only start operation till the previous carry-out signal is ready. Carry Select Adder (CSLA) is one of the fastest adders to perform arithmetic operations comparing all conventional adders. From the architecture of CSLA there is a scope for reducing the area and delay. Based on the modification of 8 bit, 16 bit, 32bit, and 64 bit Carry Select Adder (CSLA) architectures have been developed and compared with the existing CSLA architecture. A carry-select adder (CSLA) can be implemented by using Ripple carry adder. The proposed design 64-bit CSLA has reduced area as compared with the existing CSLA. Results obtained from proposed carry select adders are efficient in area. This proposed architecture has showed the performance of the proposed design in term of area. ISim simulator is used for simulating the CSLA and synthesized using Xilinx ISE design suit 14.7 and implementation proposed system on FPGA Spartan-6.***

Keywords: CSLA, RCA, VLSI, FPGA, HSG, FSG CG CS.

1. Introduction

Area efficient VLSI systems are widely used in mobile & electronics portable devices. In arithmetic operations adder is a fundamental unit. Advanced digital signal processing & communication system involves several adder will improve performance of complex DSP system. There are different types of adder but RCA is simple design and disadvantage of RCA is more carry propagation delay. The problem of carry propagation delay in RCA is improved by independent generating carries. A carry select adder is divided into sector each perform two addition in parallel, one assuming a carry in of zero and other a carry in of 1. Conventional CSLA has less propagation delay than RCA but in the architecture of conventional CSLA uses two RCA. Proposed CSLA is avoiding the dual RCA [3]. Another modified SQRT CSLA using BEC-1 and Selection unit. It reduces the area but slightly increasing the delay[4]. In both architecture conventional CSLA and modified SQRT CSLA area is increased when number of bit increases. We did analysis on logic operation involved in conventional CSLA & modified SQRT CSLA, we find there is chance to reduce area to modifying the architecture of CSLA. Proposed CSLA based on sum generation unit, carry generation unit and selection unit is involves less logic resources and propagation delay than the conventional CSLA and modified SQRT CSLA.

In Existing CSLA there are two types of CSLA Conventional CSLA and BEC based CSLA. Conventional CSLA consist of dual RCA configuration which generates a pair of sum words and output-carry bits corresponding the i/p carry (cin= 0 and 1), and selects one out of each pair for final-sum and final-output-carry. Conventional CSLA required more area than proposed system, but the design is not attractive, since it uses dual RCA. The BEC-based CSLA consist of one RCA and BEC -1 which replaced by RCA. The BEC unit receives FS0 and FC0 output from the RCA and n bit RCA replaced by n+1 bit BEC. The most significant bit (MSB) of BEC represents Cout in which n least significant bits (LSBs) represent sum. BEC based CSLA requires less logic resources than the conventional CSLA, but it has slightly higher delay than conventional CSLA.

2. Existing CSLA Architecture

The CSLA consists of two RCA (ripple carry adders) and a multiplexer. CSLA is adding two n-bit numbers with a carry select. Two RCA is required in order to perform the calculation twice, one time consider a carry ‘0’ and the other assuming ‘1’. After the two sum and carry out are calculated with respective cin=’0’ and cin=’1’. The correct sum, as well as the correct carry, is then selected with the multiplexer once the correct carry is known. The carry select adder divided into several adder groups, each of which performs two additions in parallel.

2.1 Conventional CSLA

The RCA (Ripple carry adder) consist of the HSG unit, FSG unit selection unit. The structure of conventional CSLA as shown in fig. 1 conventional CSLA consist of dual RCA and carry & sum selection unit, two n bit i/p is applied to RCA. dual ripple carry adders RCA-1 for carry 0 and RCA-2 for carry 1. Selection unit will select result of RCA -1 and RCA-2 depending on Cin=’0’ or Cin=’1’. As stated above each RCA is consist of HSG unit, HCG unit, FCG and FCG unit. Logic expressions of RCA-1 and RCA-2 of the Sum and Carry Generation unit of the n-bit CSLA are given as below. Consider two n-bit operands are added in the conventional CSLA, then RCA-1 and RCA-2 generates n-bit sum FS0 and FS1, carry FC0 & FC1 corresponding to i/p carry (Cin=0 & Cin=1) respectively.

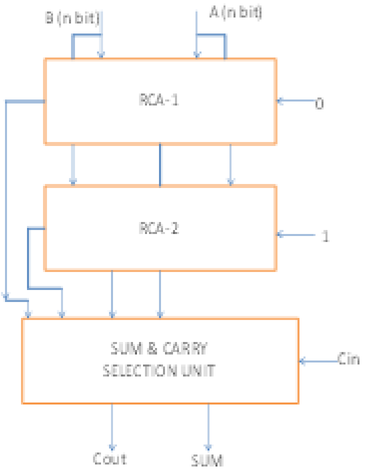

Figure 1: Conventional CSLA

$$HS_0(i) = A(i) \oplus B(i)$$
$$HC_0(i) = A(i) \bullet B(i)$$
$$FS_0(i) = HS_0(i) \oplus FC_0(i-1)$$
$$FC_0(i) = HC_0(i) + HS_0(i) \bullet FC_0(i-1)$$
$$HS_1(i) = A(i) \oplus B(i)$$
$$HC_1(i) = A(i) \bullet B(i)$$
$$FS_1(i) = HS_1(i) \oplus FC_1(i-1)$$
$$FC_1(i) = HC_1(i) + HS_1(i) \bullet FC_1(i-1)$$
$$Cout = FC_1(n-1)$$

2.2 BEC based CSLA

The block diagram of BEC based CSLA as shown in fig. 2. It consists of one RCA and BEC-1means binary to excess one converter and selection unit. There is slightly change in conventional CSLA RCA-2 is replaced by BEC-1in order to reduce area and power consumption. Two n-bit inputs applied to RCA-1 and output of RCA-1 is as input of BEC-1 unit hence n-bit RCA-1 is replaced by (n+1) bit BEC-1. Construction ripple carry adder is same as mentioned in conventional CSLA. Logic expressions of RCA-1 and BEC-1 of BEC based CSLA are given as below. Consider two n-bit operands are added in the BEC based CSLA, then RCA-1 a generate n-bit sum FS0 and FC0 and BEC-1 can generate carry FS1 & FC1. We can find from logic expression of BEC based CSLA, carry FC1 depends on FS0, which otherwise has no dependence on FS0 in the case of conventional CSLA. BEC method increases data dependence in the CSLA.

2.2.1 Binary to Excess-1 Converter.

The logic diagram of a 4-bit BEC-1 is shown in below fig. 3. and logic expression is also mentioned . BEC based CSLA is obtained by using the BEC-1 together with the mux. In this architecture input (B3, B2, B1, and B0) and output (X0, X1, X2, X3). The importance of the BEC logic stems from the large silicon area reduction when the CSLA with large number of bits are designed [1], [3]. The logic expression of the 4-bit BEC as shown in below.

X0 = ~B0
X1 = B0^B1
X2 = B2 ^ (B0 & B1)
X3 = B3 ^ (B0 & B1 & B2).

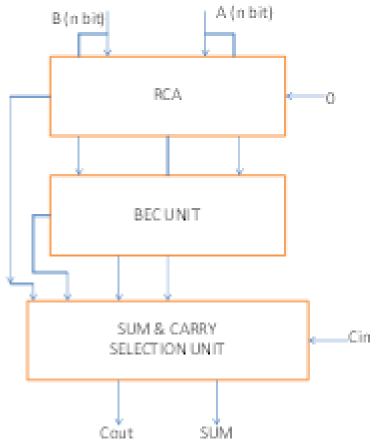

Figure 2: BEC based CSLA

$$HS_0(i) = A(i) \oplus B(i)$$
$$HC_0(i) = A(i) \bullet B(i)$$
$$FS_0(i) = HS_0(i) \oplus FC_0(i-1)$$
$$FC_0(i) = HC_0(i) + HS_0(i) \bullet FC_0(i-1)$$
$$FS_1(0) = \overline{FS_0(0)}$$
$$FC_1(0) = FS_0(0)$$
$$FS_1(i) = FS_0(i) \oplus FC_1(i-1)$$
$$FC_1(i) = FS_0(i) \bullet FC_1(i-1)$$
$$Cout = FC_0(n-1) \oplus FC_1(n-1)$$

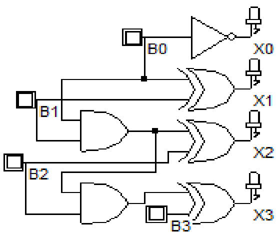

Figure: 3 Logic Diagram of BEC-1

3. Area Evaluation of Basic logic Block

In adder important basic block is XOR gate and XOR gate consist of AND, OR, and INVERTER logic gate as shown in Fig. 4. The area evaluation methodology consider all gate have one unit area. To finding an area of architecture just calculate total number of AND, OR and NOT gate then we can easily finding are.

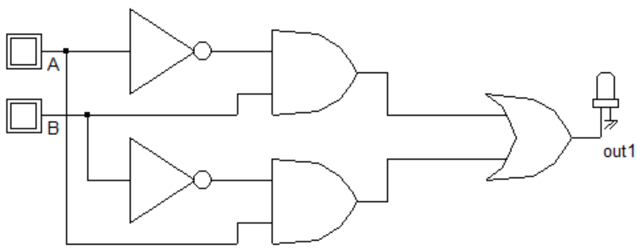

Figure: 4 Area Evaluation of an XOR Gate

The area evaluation is done by finding total number of AND, OR and NOT gate required for each logic block. In the CSLA there are following basic logic block i.e 2:1 MUX, Half Adder, XOR and Full adder. The basic logic block area evaluation are mentioned in Table I as shown in below.

Table 1: Area Count of Basic Logic Block

Logic Block	Area
XOR	5
2:1 MUX	4
Half Adder	6
Full Adder	13

4. Proposed CSLA Architecture

It has been analyzed that the architecture of conventional CSLA and BEC based CSLA have scope to reduce area. The proposed CSLA design is based on the logic expressions shown in below and its block diagram is shown in Fig. 3. It has been find that large amount of logic resources is used for calculating FS0 and FS1 in conventional and BEC based CSLA. It is not an efficient approach to reject one sum word after the calculation. Instead of that to select one carry word from two carry word corresponding '0' and '1' to calculate final sum. Using this method, we can have three advantages calculation of FS0 is not required, n-bit selection unit required than n+1 bit and small output carry delay is required.

It consists of one HSG (half sum generation unit), one HCG (half carry generation unit) , one FSG (full sum generation unit), one CG (Carry generation unit), and one CS (Carry selection unit). The CG unit consist of CG0 & CG1, CG0 is carry generation unit to i/p carry'0' & CG1 for i/p carry '1'. Two n-bit i/p data (A & B) are applied to HSG unit will generate half sum word(HS) and half carry(HC) . both CG0 & CG1 receives HS and HC from HSG unit and generate two n bit FC0 & FC1 words corresponding to i/p carry '1' & '0' respectively. The carry select unit basically consist of AND-OR gate and the gate level design of CG, HSG and CS, as shown in fig. 3. The carry select unit select one carry word from two carry word which generated by CG unit.

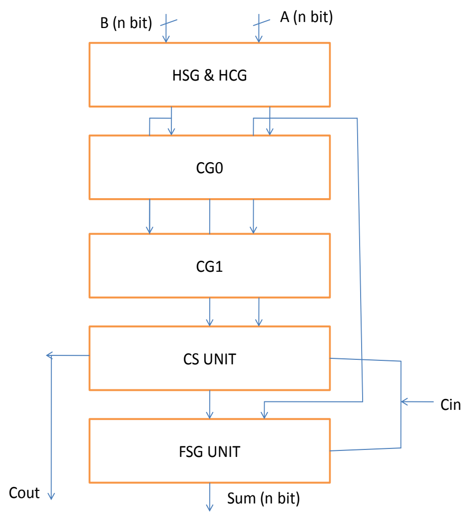

Figure: 5 Proposed System.

Logic expressions of proposed CSLA are given as below.

$$HS(i) = A(i) \oplus B(i)$$
$$HC(i) = A(i) \bullet B(i)$$
$$FC_0(i) = FC_0(i-1) \bullet HS(i) + HC(i)$$
$$FC_1(i) = FC_1(i-1) \bullet HS(i) + HC(i)$$
$$C(i) = FC_0(i)$$
$$C(i) = FC_1(i)$$
$$Cout = C(n-1)$$
$$S(0) = HS_0(0) \oplus Cin$$
$$S(i) = HS_0(i) \oplus C(i-1)$$

Synthesis and Simulation Result

5.1 Synthesis Result

It has been designed logic expression of Proposed CSLA, BEC based CSLA and conventional CSLA in verilog-HDL for 8-bit, 16-bit, 32-bit, 64-bit. ISim simulator is used for simulating the CSLA and synthesized using Xilinx ISE design suit 14.7 then implementation is done on in Spartan-6 FPGA kit. The synthesis result of 8-bit, 16-bit, 32-bitand 64-bit is given in Table II as shown in below.

Table 2: Comparision of Proposed CSLA and Exixting Csla on Area Count

No bit\ area	Conventional CSLA	BEC-based CSLA	Proposed CSLA
8 bit	212	151	133
16 bit	415	295	269
32 bit	836	607	521
64 bit	1657	1215	1085

We have synthesized proposed CSLA, conventional CSLA and BEC based CSLA on target device Spartan -6 in Xilinx 14.7. we observed that count of logic gate for proposed CSLA less than existing CSLA that plotted on graph which shown in fig. 10.

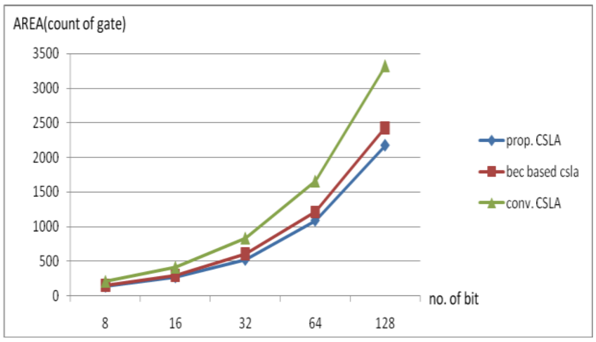

Figure: 6 Comparison of Area for Proposed CSLA and Existing CSLA

It has been synthesized proposed CSLA, Conventional CSLA and BEC based CSLA. We observe RTL schematic of 64 bit proposed CSLA An even higher level describes the registers and the transfers of vectors of information between registers. This is called the Register Transfer Level (RTL).

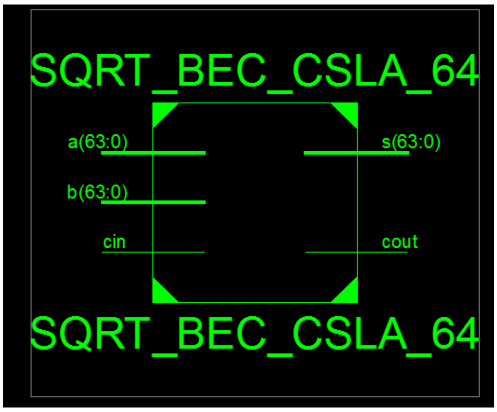

Figure 7: RTL of Proposed 64 bit CSLA

5.2 Simulation Result

We have simulated proposed CSLA for 64 bit. First i/p ' a' (63:0) and second i/p 'b' (63:0) bit and third Cin for input carry and sum result represented by s(63:0) bit and Cout represent final carry as shown in Fig. 7. We gave unsigned decimal input as a=45, b=4,cin=1 then we can observed simulation result sum=50, cout=0 on fig. 7.

Figure 8: Simulation result of proposed 64 bit CSLA

Conclusion

Proposed CSLA has been reduced all redundant logic expression of conventional CSLA and BEC based CSLA. Carry selection operation scheduled before the calculating final sum which different approach from conventional CSLA. From Table II, it can be conclude that proposed CSLA require less number of gate than existing CSLA for 8-bit, 16-bit, 32-bit, 64-bit, 128-bit. Hence The proposed SQRT-CSLA involves significantly less area. Proposed SQRT-CSLA architecture is 10.60% more efficient than BEC based CSLA and 34.65% more efficient than conventional based CSLA in terms of area for 64 bit.

References

[1] Basant Kumar Mohanty, Senior Member, IEEE, and Sujit Kumar Patel "Area-Delay-Power Efficient Carry Select Adder" IEEE Transaction On Circuit And System –Ii Express Briefs. Vol. 61. No.6, June 2014.
[2] B. Ramkumar, H.M. Kittur, and P. M. Karman, "Low Power and Area-Efficient Carry select adder "IEEE Transactions on Very Large Scale Integration System, Vol.20, No.2, February 2012
[3] B. Ramkumar, H.M. Kittur, and P. M. Karman, "ASIC implementation of modified faster carry save adder, " Eur. J. Sci. Res., vol. 42, no. 1, pp.53-58, MAY 2010.
[4] T. Y. Ceiang and M. 1. Hsiao, "Carry-select adder using single ripple Carry adder, " Electron. Lett, vol. 34, no. 22, pp. 2101-2103, Oct. 1998.
[5] Y. Kim and L.-S. Kim, "64-bit carry-select adder with reduced area, " Electron. Lett. vol. 37, no. 10, pp. 614-615, May 2001.
[6] Y. He, C. H. Chang, and J. Gu, "An area efficient 64- Bit square Root carry-select adder for low power Applications, " in Proc. IEEE Int. Symp.Circuits Syst., vol. 4, pp. 4082-4085, 2005.
[7] A. P. Chandrakasan, N. Verma, and D. C. Daly, "Ultralow-power electronics for biomedical applications," Annu. Rev. Biomed. Eng., vol. 10, pp. 247–274, Aug. 2008.
[8] O. J. Bedrij, "Carry-select adder," IRE Trans. Electron. Comput., vol. EC-11, no. 3, pp. 340–344, Jun. 1962.
[9] Y. Kim and L.-S. Kim, "64-bit carry-select adder with reduced area," Electron. Lett., vol. 37, no. 10, pp. 614–615, May 2001.

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