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Efficient Implementation of Digital Receiver on FPGA

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Abstract: ***There is a boast demand for wireless communication technology in present days. All the new wireless technologies are communicated by the Digital receiver. The main aim of this receiver is obtain information from target devices, after receiving information the parameters like speed, distance and angle of target device are calculated in Radars. In this paper introduced a 70 MHz Digital receiver which has high sampling rate for narrow band as well as wide band digital signals. The main key components of this digital receiver are DDC (Digital Down Converter) for frequency translation and ADC interface Unit to convert double rate data in to single rate data (7 bit double rate in to 14 bit single rate data). This receiver has more stability and higher precision of the signal than analogue counterparts. The Architecture of digital receiver implemented on FPGA.***

Keywords: Digital Receiver, Digital down converter, RADAR, FMC daughter card

1. Introduction

The demand for wireless technology has been increasing in recent years. Gradually there is several new wireless technologies have been introduced and develop in to use. With the introduction of these wireless standards, a radio receiver is invented, which is capable of communicating with different standards. The usage of digital receiver are being widely and replacing analog receivers. The digital receivers are compatible with higher precision and stability than analog receivers.

[5] Narrow band digital receiver introduces applications in communication signal processing. This receiver having band width for linear frequency modulation in radar signal processing. [2]-[5] The sampling frequency of the receiver is 240 MHz. Different bandwidths are required by different applications. The design parameters are depends on the bandwidth.

1.1 Applications

[4] Digital receivers are used in a range of applications like tracking receivers, signal intelligence receivers, direction finding system, radar signal processing, and wireless cellular development system. In the previous days, semiconductor devices built these receivers using analog components. Now days, suppliers are shifted to digital and mixed signal designs to ease of integration with other components and reduce the power consumption. In GSM (Global System for Mobile) system, the incoming signal frequency is around 70 MHz. This signal which is having high frequency then passes through a DDC (Digital Down Converter), which is used to perform frequency translation and produces the corresponding base band signal. The base band frequency of GSM is around 270 KHz. The pass band bandwidth of GSM is 80 KHz. The requirements for GSM are three-stage multi-rate filter(DDC),decimation factor 256, less than 0.1 dB of pass band ripple, and 18 dB of stop band attenuation at 100 KHz[4].

1.2 Key Components

This design concentrates on five-stage MultiMate decimation filter, which includes compensated integrated comb (CIC) filter [1] and two decimating finite impulse response (FIR) filters. The first stage filter in this example is CIC filter. Since the CIC filters have the ability to get high decimation factors and its multiplier free structure, it is mainly used for high speed application. The decimation factor for CIC filter in this example is 64. The second decimating filter is 21-tap-CIC-Compensation FIR (CFIR) filter [12]. It is mainly used to flatten the pass band frequency response of CIC filter because its inverse – synchronous pass band response. The decimation factor in this stage is 2. The third stage filer in this example is a 63-tap programmable FIR (PFIR) filter [12], which decimates by 2. For any modification in the filter that we want to change will be configured by using programmable FIR technique. In this design, the intermediate frequency is decided by the RF design engineers.

The ADC daughter card compiled with FMC standard. The FMC standard in this example is a dual channel A/D and dual channel D/A FMC daughter card. This card contains two 14-bit A/D channels and two 16-bit D/A channels which can be clocked by internal clock source or external sample clock. In addition there is one trigger input for customized sampling control. It has 6 MMCX or SSMC connectors available from the front panel [15]. The FMC standard in this example uses high speed LVDS outputs and require +2.5 V power supply. External sampling clock or internal sampling clock depends on the user.

The 70 MHz intermediate frequency signal which is coming from function generator is applied to ADC daughter card [15]. Here the ADC converts analog signal into digital with higher sampling rate 160 Msps. The signal is applied as input to digital down converter.

2. Proposed Digital Receiver

As shown in the figure 1, the block diagram of digital receiver implemented in FPGA. The IF and clock signals are generated by function generator. The output of ADC is double data rate. By using IP primitives in UNISIM library, this double rate data is converted into single rate data. By writing HDL code, the ADC is interfaced to FPGA.

Now, the output of ADC interface which is digitized signal is taken as input by digital down converter (DDC) which performs frequency translation and decimation factor. IP cores are used to implement this DDC. The main reason for using DDC is we can able to change the code as per our requirement.

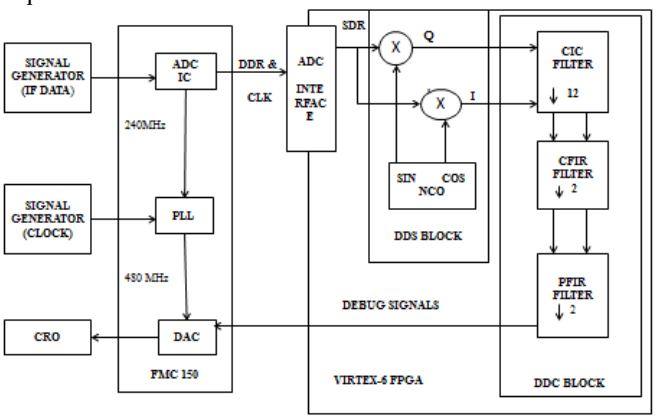

Figure 1: Digital Receiver implemented in FPGA

The DDC mainly consists of four blocks which are IP cores. Those are DDS, CIC filter, CFIR filter, PFIR filter. To obtain the base band signal, the signal is filtered and decimated at each stage of filtering section.

The micro blaze is a virtual and soft core microprocessor that is built by combing blocks of code which is cores inside a Xilinx Field Programmable Gate Array (FPGA). It has a 32-bit Harvard Reduced Instruction Set computer (RISC) architecture suitable for implementation in Xilinx FPGA. And it has separate 32 bit instruction an data buses running at full speed to execute programs and can able to access data from both on-chip and external memory at the same tie. The architecture of micro blaze have 3-stage pipeline with a32 bit general purpose registers, an Arithmetic Logic Unit(ALU), a shift register, and two interrupts. This design can be extended with more advanced features for some embedded application such as barrel shifter, divider, multiplier, single precision floating-point unit (FPU), instruction and data caches, exception handling, debug handling, fast simplex links (FSL) interfaces and others.

The micro blaze [11] has a parallel pipeline processing which are divided into three stages: fetch, decode, execute. One clock cycle is requiring completing each stage. For the completion of instruction it takes three clock cycles (ignoring delays or stalls). Each clock cycle can be activated by each stage so three instructions can be execute simultaneously. The impact of multi-cycle instruction memory latency is reduced by the instruction pre fetch buffer which is implemented by micro blaze. The instruction pre fetch buffer continues to load sequential instructions while the pipe line is stalled by multi-cycle instruction in the execution stage. It is a part of back bone of the micro blaze architecture.

3. Results

Test bench is used to verify the design code. The results of this design which are shown in figure 2 are observed by integrated software environment (ISE) software.

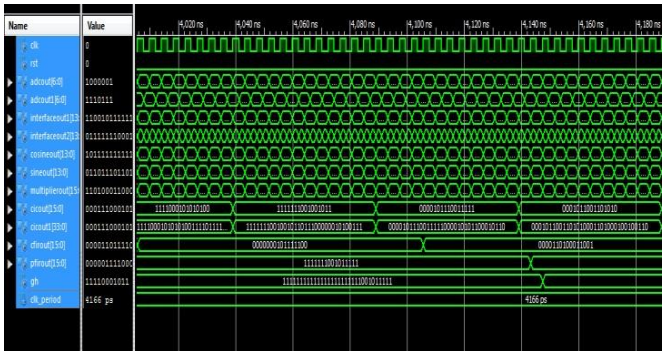

Figure 2: Results of Digital receiver

Here, the IP primitives are used to convert two ADC signals of double rate data in to single rate data. Then the 14 bit single data obtained. Finally got the required digital data by this signal is passed through filter sections.

Results are observed in MATLAB which are shown in from figures 3 to 7. Here, the Fast Fourier Transform (FFT) technique is used to check the frequency component of the signal and verify the individual part of the design. Different signals are used to verify the response of different filters.

The output of the generated input signal which is applied to multiplier is shown in figure 3.

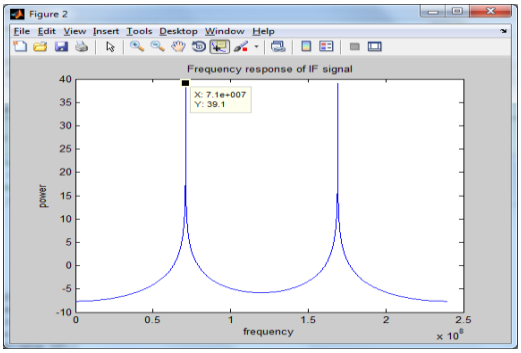

Figure 3: Input of Multiplier

Here, the input signal generated using MATLAB and is applied to multiplier. Using FFT technique, frequency of 71 MHz is generated which is required frequency of the signal. The output of the DDS is shown in figure 4.

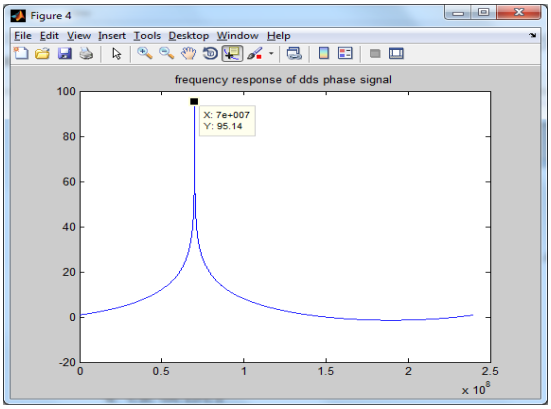

Figure 4: Output of DDS

The output frequency of 70 MHz signal is generated by DDS or numerically controlled oscillator. The output of multipier is shown in figure 5.

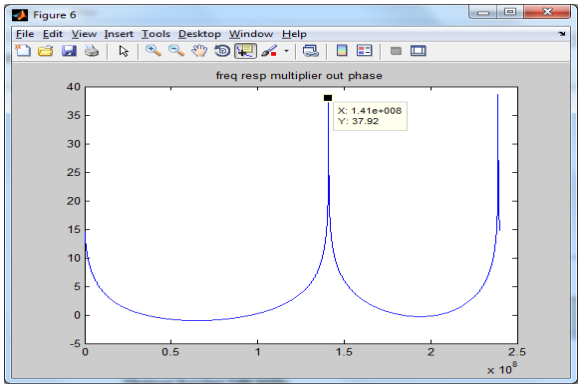

Figure 5: Output of Multiplier

Output is having 141 MHz components.Now this signal is going to be filtered. The output of CIC filter is shown figure 6.

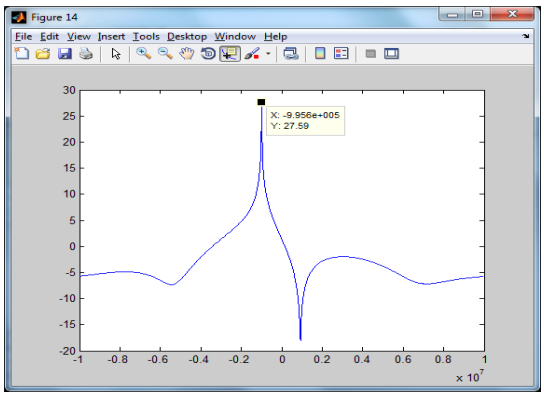

Figure 6: Output of CIC Filter

After getting base band there is some droop in the CIC output. The output of CFIR filtr is shown in figure 7.

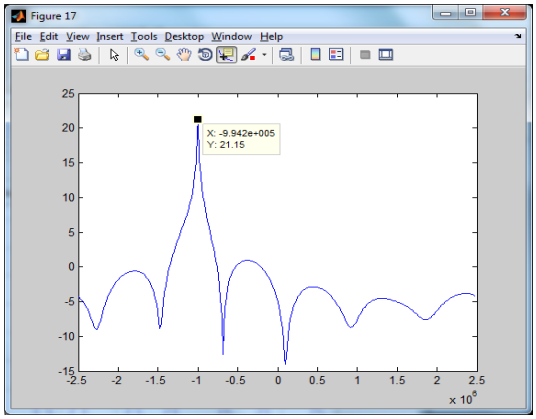

Figure 7: Output of CFIR Filter

Here, by using compensation FIR technique the droop is reduced which is occurred in CIC filter. Finally,we have 0.99 MHz signal at the output, which is expected output. Results shown in figures 8 to 12 are observed by CRO. Here the function generator is used to generate the IF signal which is input as shown in figure 8.

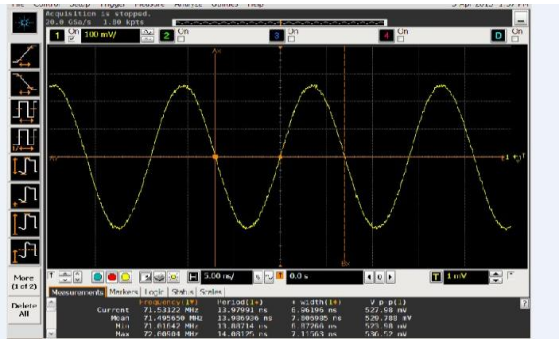

Figure 8: ADC Output

The input is beaten with the 70 MHz frequency which is generated by using DDS as shown in figure 9.

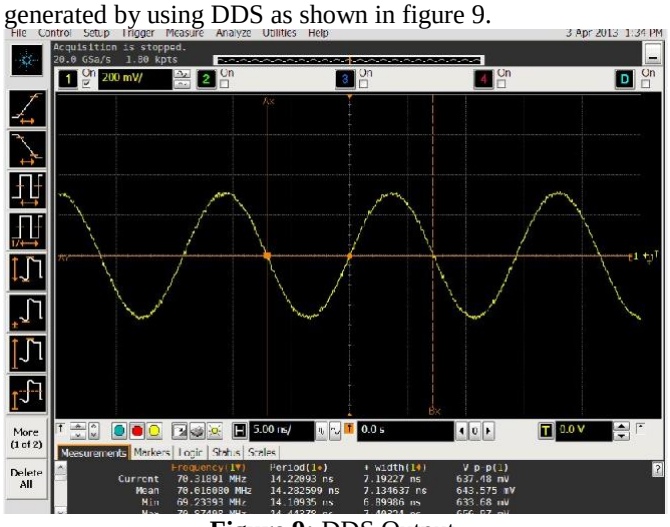

Figure 9: DDS Output

The IF input signal and DDS signal are applied as input to the mixer circuit which is shown in figure 10, that is base band signal.

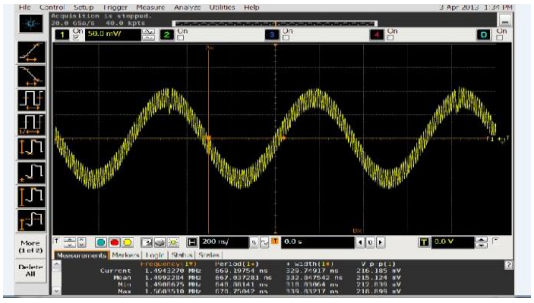

Figure 10: Mixer output

The CIC filter filtered this base band signal and obtained some droop in the signal as shown in figure 11.

Figure 11: CIC Filter Output

The droop which is obtained in the CIC filter as shown in figure 12.

Figure 12: CFIR Output

4. Conclusions

In this paper, implemented a digital receiver having band width 5 MHz with intermediate carrier frequency of 70 MHz using Xilinx IP cores. This IF signal is decimated and filtered through different filtering sections in DDC and got base band signal. Finally, obtained the base band signal with minimum noise and more spectral density.

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