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Low Noise & High Speed Domino Logic Circuit

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Abstract: ***Dynamic logic style is used in high performance circuit designs due to its high speed. But during cascading of dynamic gates, problem arises due to charge sharing, charge redistribution and charge leakage. To avoid these problems, domino logic design is used in the circuit due to their advantages such as their high speed and less noise immunity. In this paper we have proposed a new domino circuit which has very small speed power product as compared to previous designs of domino logic circuits. Simulation are carried out for 90nm technology with Vdd = 1 Volt, for the case of OR gate.***

Keywords: Domino logic, Dynamic Logic, Diode Footed Logic, Pull down Network, Charge redistribution.

1. Introduction

Dynamic logic such as domino logic is widely used in many applications to achieve high performance, which cannot be achieved with static logic styles [1]. However, the main drawback of dynamic logic families is that they are more sensitive to noise than static logic families. On the other hand, as the technology scales down, the supply voltage is reduced for low power, and the threshold voltage (*V*th*)* is also scaled down to achieve high performance. Since reducing the threshold voltage exponentially increases the sub threshold leakage current, reduction of leakage current and improving noise immunity are of major concern in robust and high-performance designs in recent technology generations, especially for wide fan-in dynamic gates [2]

The exponential increment of current Integrated Circuit Design Techniques is due to its utilization in portable and wireless systems with in the form of low budgets and high performance microprocessor. To achieve this high performance the technology has been scaled down with its transistor size, area and supply voltage. But this approach increases the density of interconnection on reduced size chip. The use of clock in Dynamic Logic circuits also increases the density of the circuit in terms of interconnection. This High Clock frequency increases the capacitive coupling of the circuit. Therefore this leads to crosstalk and which is the main cause of logic failure and delay of the circuit. There are other issues such as sub-threshold leakage current. Sub-threshold leakage current occurs when there is supply voltage is scaled then threshold voltage will also scaled which increased the leakage current. Due to continuous demand of high speed and small area devices the Dynamic logic are used in wide variety of applications because dynamic logic style is better than static logic style in terms of area and speed.[3]

A dynamic Logic style contains a pull down network which realizes the desired logic function. The Dynamic logic works in two modes know as pre-charge and evaluation phase. The dynamic circuits pre-charged at every low edge of the clock and evaluates on every high edge of the clock. Therefore this clock is one of the sources of noise in dynamic logic circuit because of its high frequency, which also increases the power dissipation of the overall circuit.

Because of fast speed and less number of transistors count compared to complementary CMOS, dynamic logic circuits are used in variety of applications such as in microprocessors and dynamic memories [4]. However due to its less noise immunity and high power consumption as compared to static CMOS circuits, it is not widely used . Fan-out of domino gate is driven by an inverter which has low output impedance due to which noise immunity of gate is increased [5].

The basic domino gate is shown in Fig. 1. When clk is low, PMOS transistor Mp is turned ON, dynamic node charges to Vdd and circuit is in pre-charge state. Because NMOS transistor Mn is turned OFF, there does not exist any path to the ground. When clk is high, transistor Mp is turned off and Mn turns on, and the circuit is in evaluation phase. During evaluation phase, there are two conditions for the output voltage. If inputs IN1 and IN2 are equal to one, the dynamic node discharges to ground and output of the circuit will be equal to one. If both input values are equal to zero, dynamic node voltage should be maintained at high value and output of the circuit should be zero. However charge stored at dynamic node is leaked to ground due to charge leakage, charge redistribution and charge sharing problems. Domino logic circuit is used to avoid these problems[4].

Domino logic circuits are advantageous for smaller area and higher speed compared to static CMOS design, due to this it has been widely used in high speed processors; however average power consumption of domino logic circuit is larger than static CMOS. Voltage of the circuit has to be reduced to achieve high speed operation. But on reducing threshold voltage, sub threshold current of the circuit is exponentially increased, because sub-threshold current has exponential relation with threshold voltage. Leakage current and noise immunity are very crucial points of concern, in domino logic circuits.

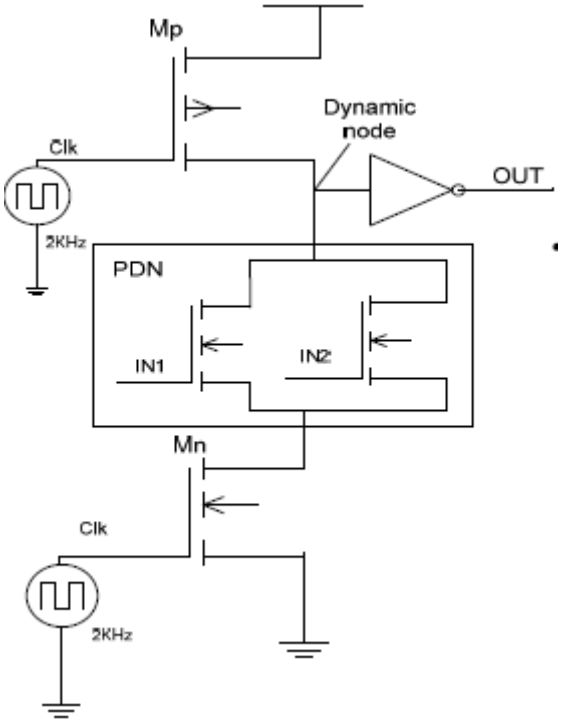

Figure 1: Basic domino logic circuit

In this paper we have proposed a new domino logic circuit scheme for improving power-delay product and noise immunity. The remaining paper is organized as follows. Section II presents the problem definition related to noise immunity. Section III presents background work related to domino logic. Section IV presents pervious domino logic circuit and Section V presents new proposed domino logic circuit scheme and simulation results and comparisons are discussed in section VI, conclusion is presented in section VII.

2. Problem Definition

Major problem arises in domino logic circuit during evaluation phase, when both the inputs of pull down network are zeros. During this period, charge leakage phenomenon takes place in the circuit and sub-threshold leakage current becomes very dominant in the pull down network. To reduce leakage current in pull down network, either threshold voltage of NMOS of PDN should be increased or size of NMOS pull down network should be increased. Fig. 2 [4] shows the basic footless domino logic circuit. When clock is low, PMOS will turn ON, and dynamic node will be charge up to Vdd and circuit is in pre-charge phase. When clock is high, PMOS will turn OFF, and there exists two conditions of output depending on the inputs: (1) If inputs are high, charge stored at dynamic node will be discharge through ground.

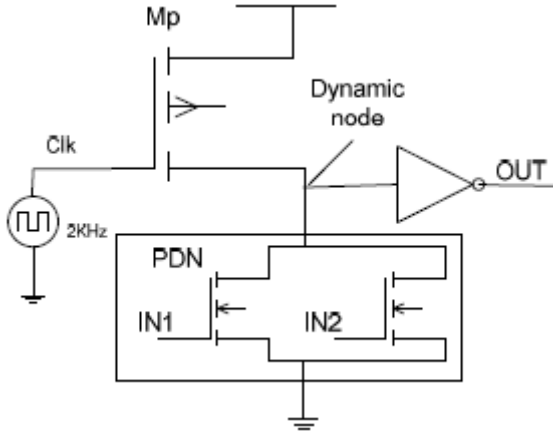

Figure 2: Footless domino logic

(2) If inputs are low, charge stored at dynamic node must be maintained at the dynamic node. Because of charge redistribution problem, NMOS pull down network leaks the charge stored in capacitance at dynamic node. This problem is further improved by PMOS keeper circuits. The basic goal of adding keeper circuit is to store charge at dynamic node during evaluation phase, when inputs of pull down network are equals to zero. When a noise voltage impulse comes at input of any gate, the keeper cannot store the voltage level of the dynamic node. There is exponential relation between sub-threshold leakage current and Vgs. So that, when noise impulse occurs at the gate input, gate voltage increases, which leads to increase in Vgs and the dynamic node gets discharged [6]. In domino logic, noise is important factor than power, area and delay issues. To improve noise, several techniques are used but there are many disadvantages regarding area, power and delay [4]-[7]. To ignore these problems, new domino logic circuit is proposed in further section

3. Related Background Work

Keeper circuit is used in domino logic to eliminate sub threshold leakage current at dynamic node. When pull down network is turned OFF, keeper circuit prevents the charge stored at dynamic node in evaluation phase [8]. Domino logic circuit with keeper PMOS transistor is given below in Fig. 3[4]. Keeper PMOS store the charge at dynamic node when pull down network is turned OFF during evaluation phase. When clock is low, dynamic node will be charge up to V_{dd} and output of the circuit is zero that means circuit is in precharge phase. When clock is high (during evaluation phase) and inputs of pull down network are zeros, then with the help of keeper charge will be maintained at dynamic node and the output of the circuit will be zero. However, when clk is high and inputs of pull-down network is equals to one, charge stored at dynamic node will be leak away through footer transistor M_n. Noise impulses at the input of

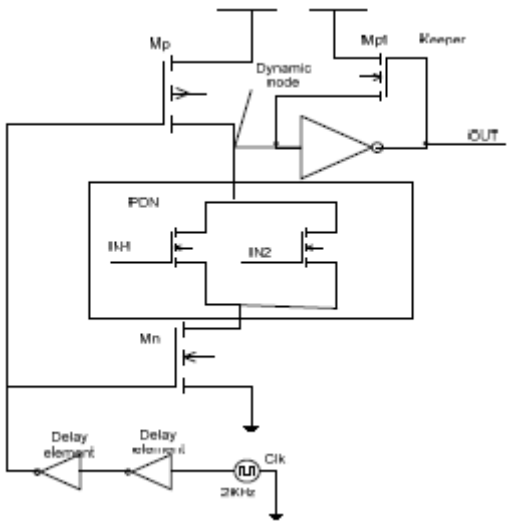

Figure 3: Footer domino logic

NMOS pull down network increases the gate to source voltage. So that sub-threshold current increases the charging of dynamic node [8].

4. Pervious Domino Logic Circuit

The domino logic scheme is shown in Fig.4[4]. In this circuit in place of footer transistor current mirror circuits are used in stack. Purpose of current mirror circuits is such that, if any noise signal occurs at M1 it will be leak to ground via M4 and M5. Transistors M3 and M4 also forms current mirror, due to both current mirror circuits gate to source voltage of NMOS pull down network decreases rapidly. This effect is called as stacking effect. The purpose of M4 and M5 in the proposed circuit to create stacking effect, due to which voltage drop across M2 reduces [9]-[10].

The presence of current mirrors in the proposed circuit causes increase in delay. To overcome this problem size (W/L ratio) of PDN should be increased. Because of stacking effect circuit dissipates power and becomes less noise robust. In this proposed circuit there will be voltage drop in evaluation phase due to stacked current mirrors. Due to negative Vgs, there will be exponential reduction in subthreshold current in the circuit. In order to improve power-delay product more and more, size of PMOS transistor should be four times that of NMOS transistor in invertor circuit at the output node. Purpose of transistor Mp3 is to provide strong vdd to the lower PMOS Mp2, Because PMOS transistor are used to provide strong one logic to the circuit.

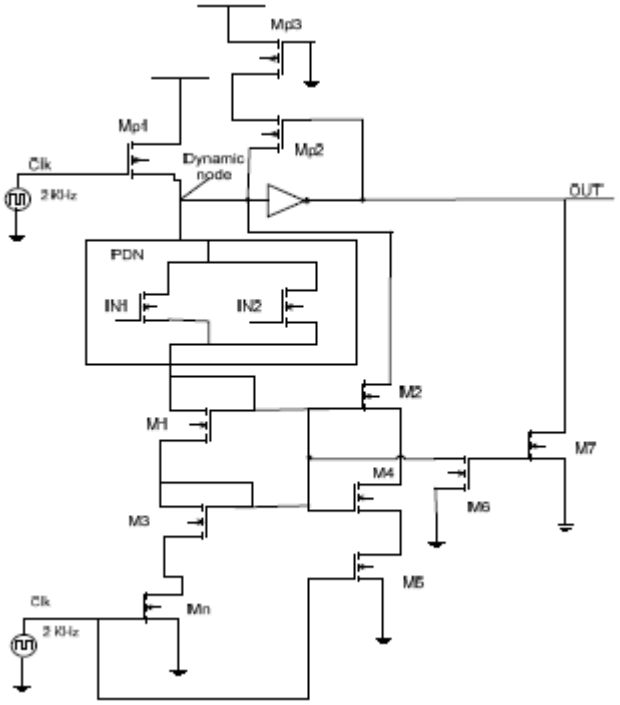

Figure 4: Pervious domino logic

5. Proposed Domino Logic Circuit

The proposed domino logic scheme is shown in Fig.5. In this circuit in place of current mirror circuits are used the stack of PMOS transistor in footer logic. The modified circuit of domino logic contains the stack of PMOS transistor in footer logic, the schematic and configuration of this approach work in a manner so it can reduce the leakage to ground and indirectly reduces the power dissipation novel low-leakage-power design is described. The transistors are held in reverse body bias. This reverse body biasing increases their threshold. This increased threshold voltage results in low leakage current and hence low leakage power. As we know the leakage current is the main cause of power dissipation we have reduce the leakage power using a stack of PMOS transistor in Footer circuits. PMOS degrades the low logic level. As we know that static power is relative to the voltage apply, through the reduced voltage the power decreases and we get the advantage of less degradation of logic. This approach contains another advantage during off mode if we increase the threshold voltage PMOS Transistors in Footer Circuits.

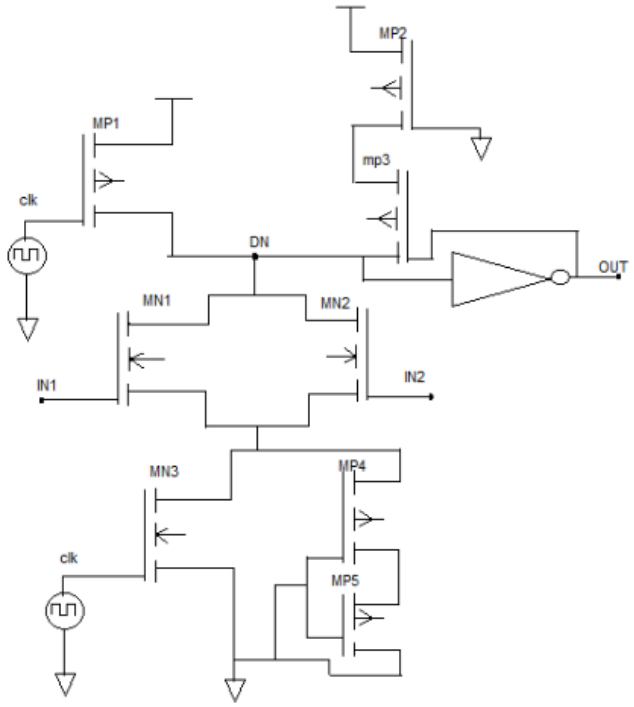

Figure 5: Modified circuit using PMOS Stack in footer circuit

The transistors are held in reverse body bias. Because as result their threshold is high, higher threshold voltage causes low leakage current and therefore low leakage power. If we use minimum size of transistors, i.e. aspect ratio of 1, we yet again get low leakage power due to low leakage current. As a result of stacking, PMOS footer transistor will get less drain voltage.

6. Simulation Results

Simulation results of the circuits, given in this paper are represented by table I. These results show that the power and delay of the proposed circuit is very less among the domino logic circuits mentioned in this paper. On comparing the PDP (power-delay product) of proposed circuit with basic domino logic, footless domino logic, and footer domino logic circuits, the results of table I shows that proposed domino logic circuit has very small value of power-delay product. power delay are very important factor for improving the the capacity of a circuit in dominocircuit technology.

Table 1: Power, Dealy and Power Delay product Comparision of Previous and Modified Design

	Basic Domino Logic	Footless Domino Logic	Footer Domino Logic	Previous Domino Logic	Modified Domino Logic
Supply Voltage(V)	1	1	1	1	1
Power(uW)	13.3	78.4	3.19	0.074	0.056
Delay($X10^{-10}$)	338	155	103	2.55	0.63
PDP($X10^{-19}$)	4495.4	1215.2	328.5	118.3	35.4

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Table 2 represent the power-delay product of previous circuit for supply voltage of 1v, 0.9v, 0.8v, 0.7v, and 0.6v.

Table 2 Previous Design Power Delay Product With Different Supply Voltages

Supply Voltage(V)	1	0.9	0.8	0.7	0.6
Power(uW)	0.074	0.059	0.044	0.030	0.023
Delay($X10^{-10}$)	2.549	4.129	9.612	19.793	33.669
PDP($X10^{-19}$)	188.38	243.831	414.800	591.410	773.930

Table 3 represents Power-delay product of previous circuit is influenced by size of transistors M6 and M7. The variation of power-delay product with the size of transistors M6 and M7 is given in table III. III.

Table 3: Effect of Transistor Size of M6 AND M7ON Power Delay Product

Size of m6 & m7(nm)	180nm	240nm	480nm	500nm
PDP (×10-19)	118	84	19.5	1.6

Table 4: Modified Design Power Dealy Product With Different Supply Voltages.

Supply Voltage(V)	1	0.9	0.8	0.7	0.6
Power(uW)	0.056	0.047	0.033	0.025	0.018
Delay($X10^{-10}$)	0.628	0.750	0.907	1.371	2.333
PDP($X10^{-19}$)	35.4	33.5	30.2	34.2	41.2

Results given in table IV shows that the proposed circuit gives minimum value of power-delay product for supply voltage of 1, 0.9,0.8,0.7, & on 0.6 volts. In the modified circuit of domino logic contains the stack of PMOS transistor in footer logic, the schematic and configuration of this approach work in a manner so it can reduce the leakage to ground and indirectly reduces the power dissipation novel low-leakage-power design is described. The transistors are held in reverse body bias. This reverse body biasing increases their threshold. This increased threshold voltage results in low leakage current and hence low leakage power. As we know the leakage current is the main cause of power dissipation we have reduce the leakage power using a stack of PMOS transistor in Footer circuits. Modified circuit gives best value of power-delay production with the help of reverse body bias. As we know that static power is relative to the voltage apply, through the reduced voltage the power decreases and we get the advantage of less degradation of logic

7. Output Waveform of Various Circuit

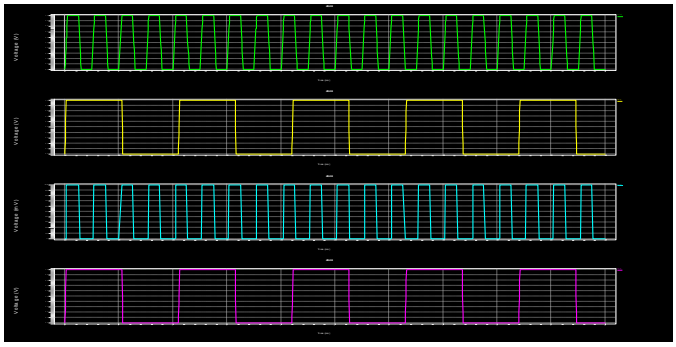

Figure 5: (a) Basic domino logic circuit

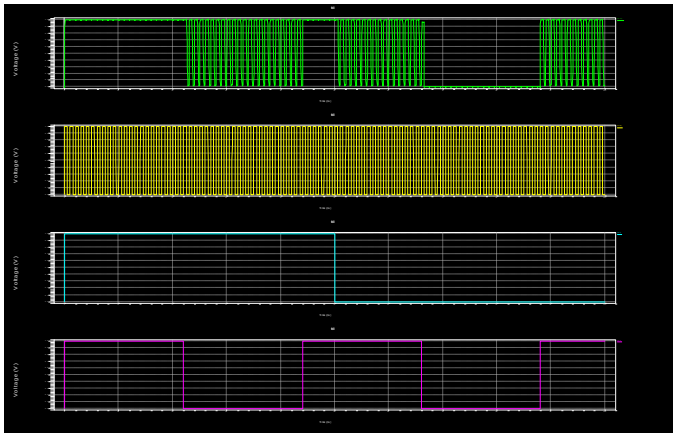

Figure 5: (b) footless domino logic circuit

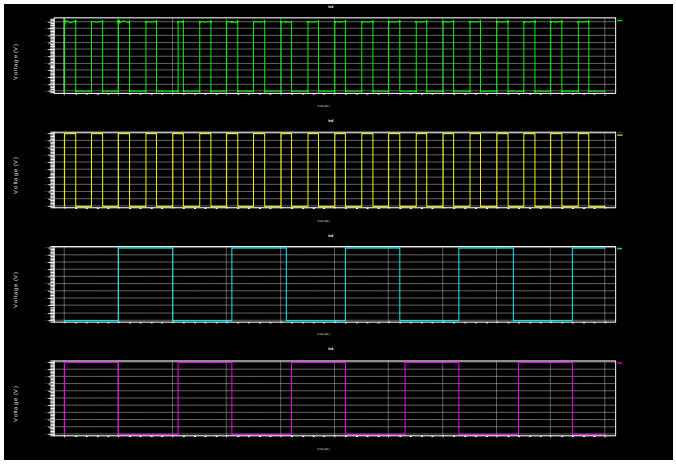

Figure 5: (c) Footer domino logic circuit

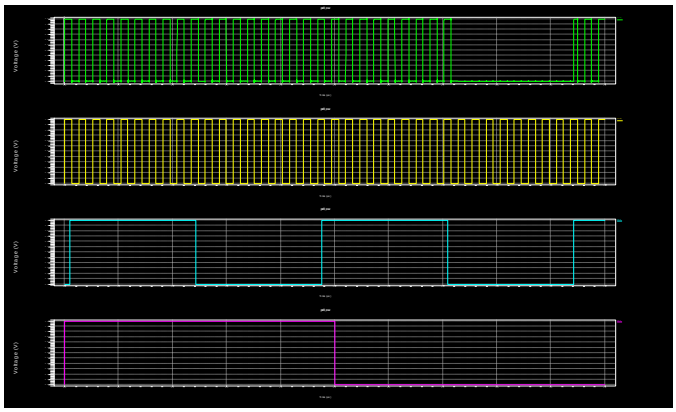

Figure 5: (d) Pervious domino logic circuit

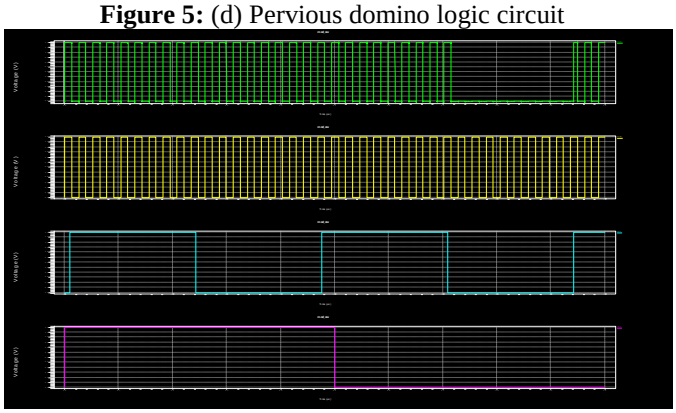

Figure 5: (e) Modified circuit using PMOS Stack in footer circuit

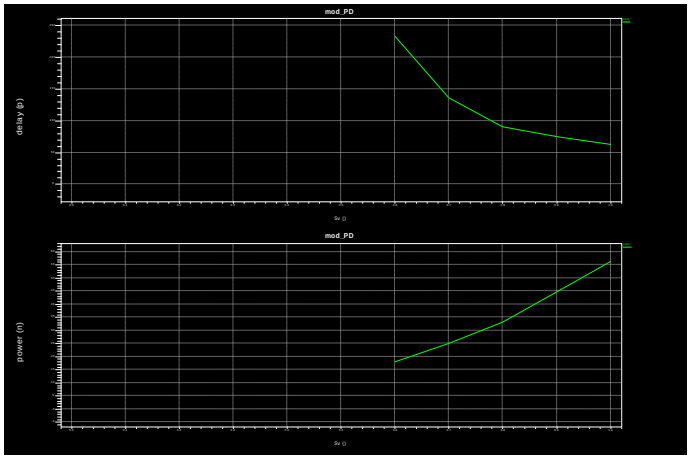

Figure 5: (f) Modified Design Power and Delay for different supply voltages

8. Conclusion

In this paper a new domino logic contains the stack of PMOS transistor in footer logic, the schematic and configuration of this approach work in a manner so it can reduce the leakage to ground and indirectly reduces the power dissipation novel low-leakage-power design is described. The proposed circuit is simulated on tanner tool 90nm technology. Proposed circuit when compared to previous domino logic scheme, shows reduction in speed-power product, as well as improved nois immunity. The proposed scheme is used in recent embedded processors where low power and high speed is required.

References

[1] J. M. Rabaey, A. Chandrakasan, and B. Nicolic, *Digital Integrated Circuits: A Design Perspective*, 2nd ed. Upper Saddle River, NJ:Prentice-Hall, 2003.

[2] L. Wang, R. Krishnamurthy, K. Soumyanath, and N. Shanbhag, "An energy-efficient leakage-tolerant dynamic circuit technique," in *Proc. Int. ASIC/SoC Conf.*, 2000, pp. 221–225.

[3] F. Frustaci M. Lanuzza P. Zicari S. Perri, and P. Corsonello, "Lowpower split-path data-driven dynamic logic," *IET Circuits Devices Syst.*,vol. 3, no. 6, pp. 303–312, 2009.

[4] Shiksha and Kamal Kant Kashyap "High Speed Domino Logic Circuit for Improved Performance" 2014 IEEE.

[5] Ali Peiravi and Mohammad Asyaei " ieee transactions on very large scale integration (vlsi) systems", vol. 21, no. 5, may 2013.

[6] Meher P, and K. K. Mahapatra "a low power circuit technique for Domino CMOS logic," *International Conference on ISSP*, 2013, pp.256-261.

[7] H. Mahmoodi-Meimand, and K Roy, "Diode-footed domino: a leakagetolerant high fan-in dynamic circuit design style," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 51, no. 3, pp. 495–503, 2004.

[8] Fang Tang, and KEe Zhu, Quan Gan, and Jian Guo Tang, " Low-noise and power dynamic logic circuit design based on semiconductor dynamic logic," *2nd International conference on Anti counter feiting, security and identification*, August 2008, pp. 20-23.

[9] J. T Kao, "Subthreshold Leakage Control Techniques for Low Power Digital Circuits," *Ph. D. Thesis, Massachusetts Institute of Technology*, USA, May 2001.
[10] S. Mukhopadhyay et al, "Gate Leakage Reduction for Scaled Devices Using Transistor Stacking," *IEEE Trans. on Very Large Scale Integration (VLSI) Systems*, vol. 11, no. 4, August 2003.