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A Hierarchical Design of High Performance Carry Select Adder Using Reversible Logic

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Abstract: ***Adders are the basic functional unit of arithmetic operations. Due to the quickly growing mobile industry not only the faster arithmetic unit but also less area and low power arithmetic units are needed. The CMOS carry select adder (CSLA) consists of two sets of ripple carry adder (RCA) and the modified CSLA replaces one set of RCA with a binary to Excess One (BEC) converter. The modified CSLA architecture has developed using Binary to Excess-1 converter (BEC). This paper presents a performance analysis of reversible, VLSI implementations of 16 bit carry select adders suitable for multi-digit addition. The Reversible logic (RVL) provides the key benefit of a higher data processing capability per unit chip area. This paper present design of 16 bit CSLA using Tanner EDA tool & simulated using T-spice simulator. With the help of Reversible technique 16 bit Reversible Carry Select Adder has been proposed in this paper. The Proposed CSLA has reduced transistor count as well as power consumption as that of CMOS CSLA.***

Keywords: Area Efficient, CSLA, Low Power, BEC

1. Introduction

In recent years, the increasing demand for high-speed arithmetic units in micro-processors, image processing units and DSP chips has paved the path for development of high-speed adders as addition is an indispensable operation in almost every arithmetic unit, also it acts as the basic block for synthesis of all other arithmetic computations .To increase portability of systems and battery life, size and power consumption are the critical factors of concern. Even in servers and personal computers (PC), power dissipation is an important design factor. Now a days, Design of area-efficient and power-efficient high-speed logic systems are the one of the crucial areas of research in VLSI design. Addition is one of the basic arithmetic operations and nearly 8.72 % of all the instruction in a typical processor is addition.. Low power area-efficient and high-performance VLSI systems are increasingly used in portable and mobile phones, multi-standard wireless receivers, and biomedical instrument. An adder is the main component of an arithmetic unit. A complex digital signal processing (DSP) system involves several adders. An efficient adder design essentially improves the performance of a complex DSP system Amongst the different building blocks of a DSP system, a adder is an essential component that has a significant role in both speed and power performance of the entire system. Therefore, to enhance the performance of DSP SoCs, designing of high performance and power efficient as well as delay efficient adder is crucial. So Carry Select Adder (CSLA) is one of the fastest adders used in many data-processing processors to perform fast arithmetic functions.

Since, addition dominates the execution time of most DSP algorithms therefore high-speed adder is much desired .With an ever-increasing quest for greater computing power on battery-operated mobile devices, design has shifted from optimizing practical delay time, gate count to minimizing power dissipation while still maintaining the high performance. The low power and high speed adder can be implemented with different logic style. As we know millions of instructions per second are performed in microcontrollers. So, speed of operation is the most important constraint to be considered while designing adder. The demand of low power high speed circuits are in demand with the increasing universal growth in electronic system and the loss of information is not acceptable as with single loss of a bit information the energy loss is equal to kTlog2 joules/bit. Reversible logic can be of major interest to design low power arithmetic and data path units for digital signal processing applications, such as the architecture of low power adder, multipliers etc.

Reversible logic has make great attention in the recent years due to its ability to reduce the power dissipation Reversible logic circuits find wide application in low power digital design Reversible logic is very essential for the construction of low power, low loss computational structures which are very essential for the construction of arithmetic circuits used in quantum computation, nano technology and other low power digital circuits.

2. Literature Review

Bedriji 1962 proposes [3] that the problem of carry propagation delay is overcome by independently generating multiple radix carries and using these carries to select between simultaneously generate sum. Akhilash Tyagi 1993 develop a scheme to generate carry bits with block carryin 1 from the carries of a block with block carry in 0 [8]. Chang and Hsiao 1998 [4] propose that instead of using dual carry ripple adder a carry select adder scheme using an add one circuit to replace one carry ripple adder. Youngioon Kim and Lee Sup Kim 2001 [6] introduces a multiplexer based

add one circuit is proposed to reduce the area with negligible speed penalty. Yajuan He et al 2005 develop an area efficient square root carry select adder scheme based on a new first zero detection logic [5]. Ramkumar et al 2010 proposed a BEC method to reduce the maximum delay of carry propagation in final stage of carry save adder [2]. Ramkumar and Harish 2011 propose [11] BEC technique which is a simple and efficient gate level modification to significantly reduce the area and power of square root CSLA. Padma Devi et al 2010 proposed [7] modified carry select adder designed in different stages which reduces the area and power consumption.

3. Carry Select Adder

CMOS carry select adder consists of two sets of ripple carry adders. Ripple-carry adders are the simplest and most compressed full adders, but their recital is limited by a carry that must propagate from the least -significant bit to the most- considerable bit. The various 16, 32, 64 and 128-bit CSLA can also be developed by using ripple carry select adders. The speediness of a carry- select adder can be improved upto 40% to 90%, by performing the additions in equivalent, and reduce the maximum carry delay. Fig shows the Regular structure of 16-bit CSLA. It includes many ripple carry adders of variable sizes which are separated into groups. Group 0 contain 2-bit RCA which contains only one ripple carry adder which adds the input bits and the input carry and results to sum [1:0] and the Cout. The cout of the Group 0 which acts as the selection input to mux which is in group 1, select the end result from the corresponding RCA (Cin=0) or RCA (Cin=1). Similarly the remaining groups will be selected depending on the Cout from the earlier groups. In CMOS CSLA, there is simply one RCA to perform the addition of the least significant bits[1:0]. The remaining bits (other than LSBs), the addition is perform by via two RCAs corresponding to the one assuming a carry -in of 0, the other a carry-in of 1 inside a group. In a group, readily available are two RCAs that receives the same data inputs but altered Cin. The upper adder contain a carry-in of 0, the lower adder contain a carry-in of 1. The actual Cin from the prior sector selects one of the two RCAs. That is, as shown in the Fig.3, if the carry-in is 0, the sum and carry-out of the upper RCA is certain, and if the carry-in is 1, the sum and carry-out of the lower RCA is fixed. For this CMOS CSLA structural design, the functioning code, for the Full Adders and Multiplexers of different sizes (6:3, 8:4, 10:5 up to 24:11) were designed initially.

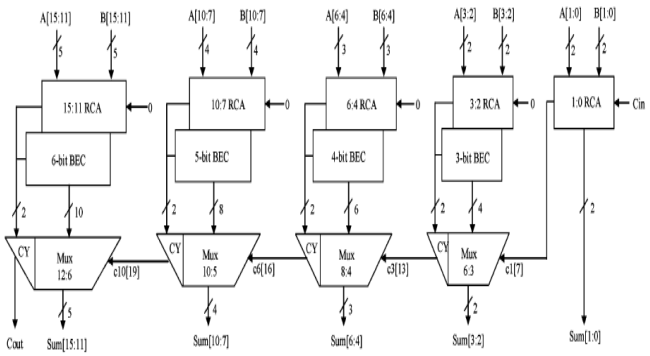

Figure 1: Regular 16- bit CSLA (Ref-1)

- The trouble in CSLA design is that if the number of full adders are greater than before then the circuit complexity also increases.
- The number of full adder cells are sadditional thereby power consumption of the design also increases
- Number of full adder cells doubles the area of the design also increased.

Figure 1 is a single bit carry sum generator with 28 mosfet designed with pass transistor logic. The circuit is designed with nmos & pmos. Device is having width 2.5um and length 250nm. Design is having two inputs A and B and corresponding output is Sum and carry.

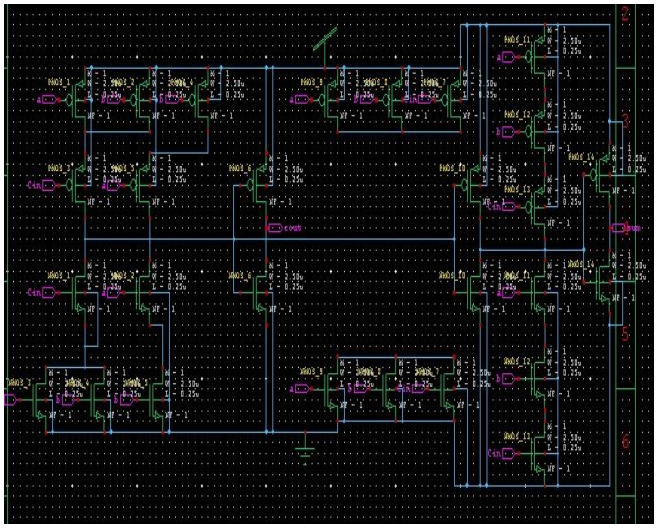

Figure 1: Schematic of Carry sum generator for 1 bit CMOS csla

Figure 2 is a schematic of single bit carry sum generator of Reversible Carry select Adder with 14 mosfet designed with pass transistor logic. Reversible schematic comprise of Reversible gates, which is also designed with nmos & pmos. Device is having width 2.5um and length 250nm. Design is having two inputs A and B and corresponding output is Sum and carry.

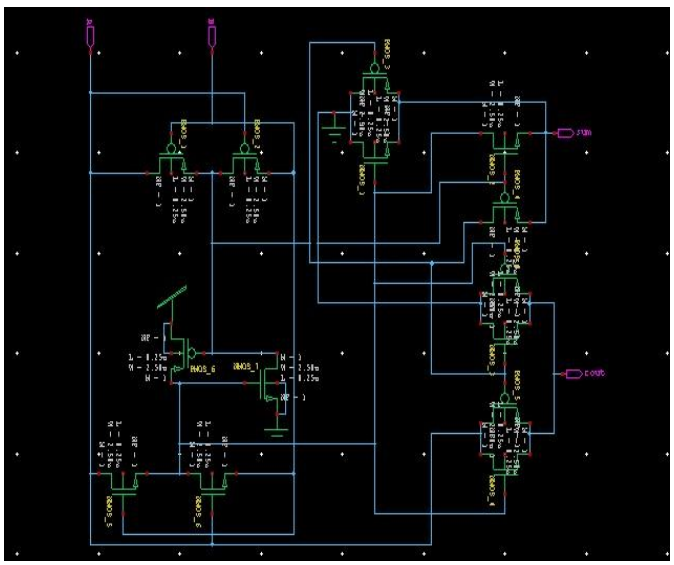

Figure 2: Schematic of Carry sum generator for 1 bit Reversible csla

Fig. 3 illustrates basic function of the CSLA is obtained by using the 4-bit BEC together by means of the mux. One key in of the 8:4 mux gets as it input (B3, B2, B1, and B0) and another key in of the mux is the BEC output. This produce the two probable partial results in equivalent and the mux is used to select either the BEC output or the direct inputs according to the control signal Cin. The significance of the BEC logic stems from the large silicon area reduction when the CSLA with large number of bits are designed.

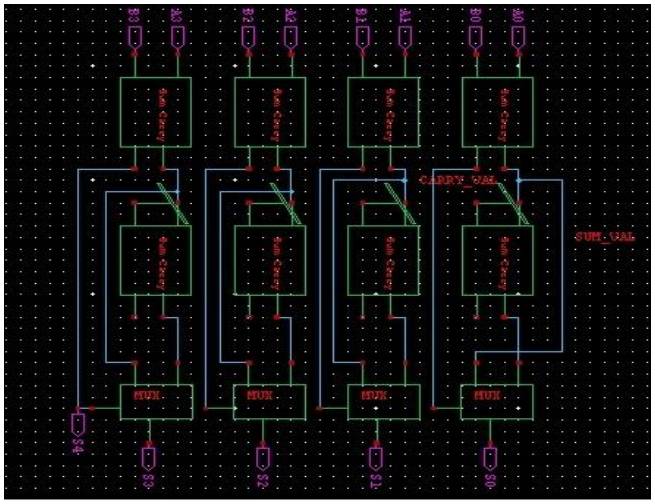

Figure 3: Block Diagram of 4 bit csla

Figure4 shows the mux design using pass transistor logic. It will be used in further stage of CSA. Mux is used for selection of bits using the select lines It has two input Ain & Bin and one select lines Design require 6 Mosfet having width 2.5um and length 250nm.

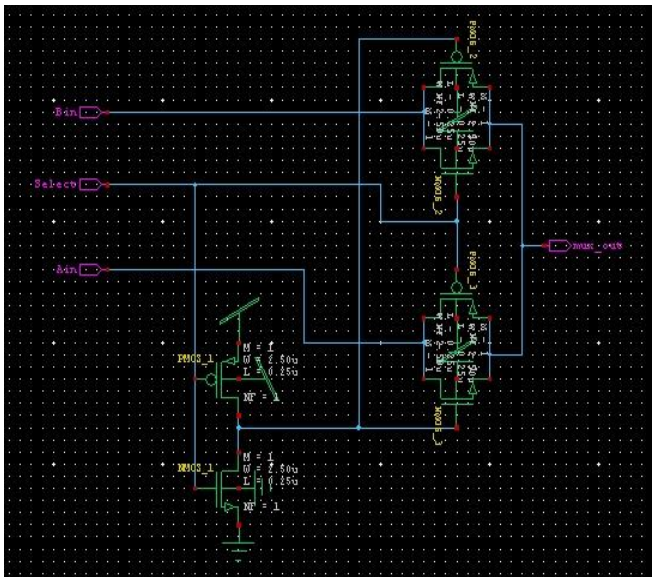

Figure 4: Schematic of MUX for 4bit CSLA

Figure5 shows the architecture of 4bit CSA with A[3:0] and B[3: 0] with corresponding output of 4 bit i.e Out S[3:0]. 4 bit csla is designed by cascading 1 bit csla in parallel and carry is shifted to next block.

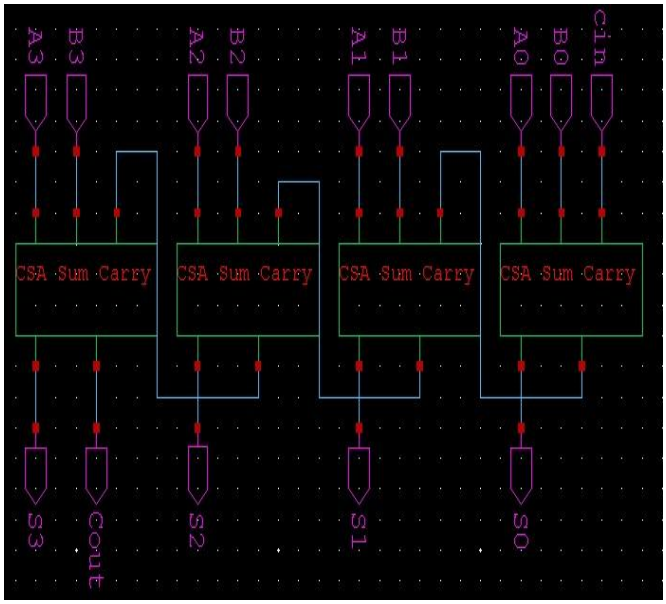

Figure 5: Architecture of 4 bit CSLA

Figure 6 shows 16bit CSA with A [15:0] and B[15: 0] with corresponding output of 16 bit i.e Out S[15:0]. Now the Adder 16 bit is designed by cascading 4-4 bit csla in parallel. Simulation result of 16 bit csla of CMOS as well as reversible is shown below.

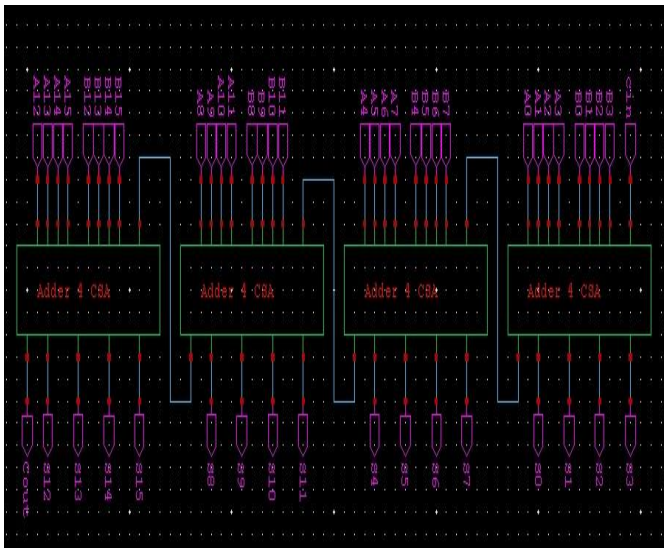

Figure 6: Architecture of 16 bit CSLA

4. Results

The proposed 16 bit CSLA has been successfully tested and synthesized in Tanner EDA Tools using 180nm, 90nm & 65 nm technology with a supply voltage of 5.0v. The power consumption , total number of gate count and delay is noted down for CMOS & reversible CSLA.

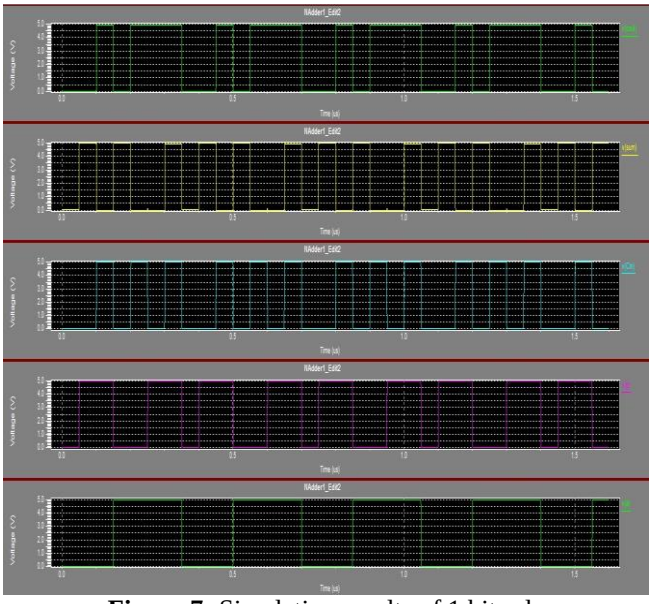

Figure 7: Simulation results of 1 bit csla

Figure 8 is the output waveform for 4 bit CSLA structure. Input is varied from 0000 to 1111 and corresponding output is observed at each instant of time. Waveform is seen in W-edit window of tanner.

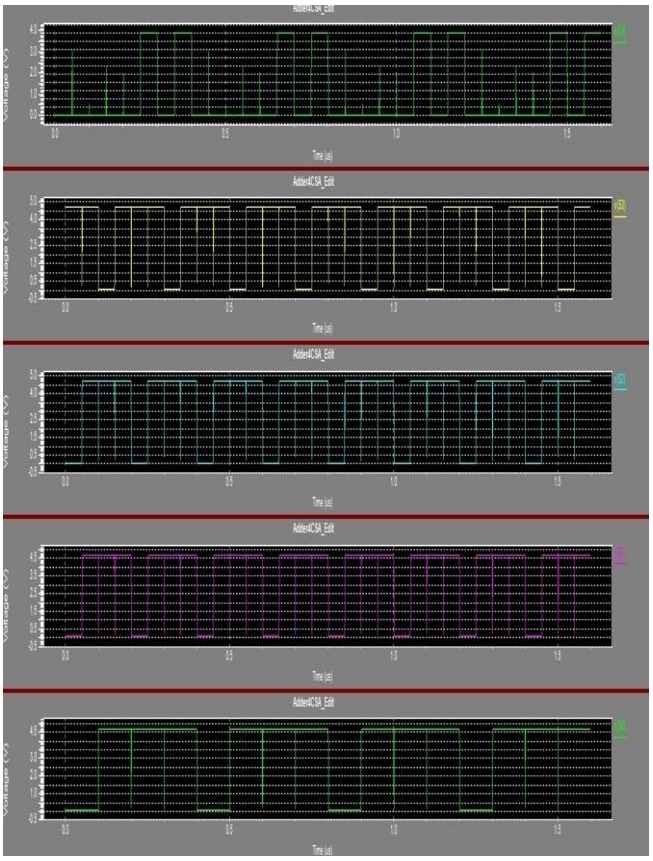

Figure 8: Simulation results of 4 bit csla

Figure 9 is the output waveform for 16 bit CSLA structure. Input is varied from "0h0000" to "0h1111" and corresponding output is observed at each instant of time. Waveform is seen in W-edit window of tanner.

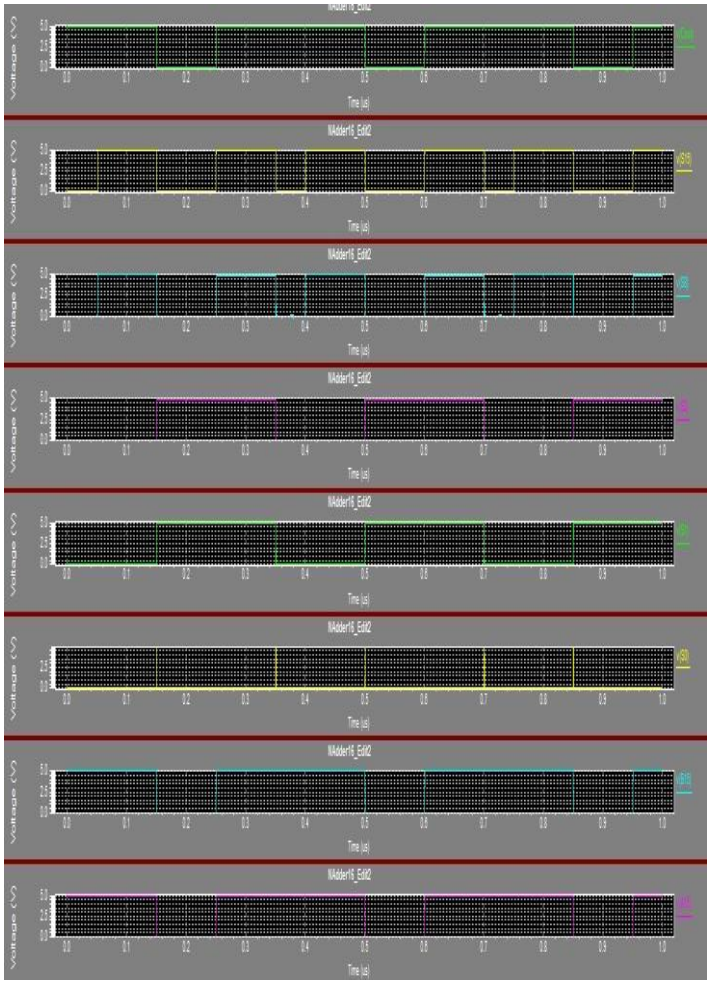

Figure 9: Simulation results of 16 bit csla

Table 1: Result Comparison of CMOS Carry select Adder at different CMOS process Technology

Type of Adder	Technology	Power (Watt)	Total Nb of Gate Count	Delay (ns)
1 Bit CSA	180nm	2.131×10^-4	28	0.957
	90nm	7.690×10^-6	28	0.619
	65nm	1.703×10^-6	28	0.676
4 Bit CSA	180nm	8.130×10^-4	112	0.80
	90nm	1.998×10^-5	112	0.704
	65nm	5.906×10^-6	112	0.963
16 Bit CSA	180nm	3.42×10^-3	448	0.998
	90nm	7.817×10^-5	448	0.601
	65nm	2.363×10^-5	448	0.653

Table 2: Result Comparison of Reversible Carry select Adder at different CMOS process Technology

Type of Adder	Technology	Power (Watt)	Total Nb of Gate Count	Delay (ns)
1 Bit CSA	180nm	3.367×10^-5	14	0.996
	90nm	2.158×10^-6	14	0.957
	65nm	4.280×10^-7	14	0.983
4 Bit CSA	180nm	1.373×10^-4	56	0.864
	90nm	7.991×10^-6	56	0.729
	65nm	1.437×10^-6	56	0.998
16 Bit CSA	180nm	8.451×10^-4	224	1.01
	90nm	3.255×10^-5	224	0.740
	65nm	6.201×10^-6	224	0.88

5. Conclusion

It can be concluded that Reversible Logic is better in all respect like speed, delay, area, complexity, power consumption. However CMOS adder requires more power consumption and more number of components but delay for this Reversible adder is just a bit larger than CMOS adder. Hence for low power requirement and for less number of gate count requirement Reversible adder is suggested. Further the work can be extended for optimization of said adder to improve the speed or to minimize the delay.

6. Scope of Future Work

An improvement in addition speed by using new techniques can greatly improve system performance. This project can be extended for the reconfigurable architecture.

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