5. Conclusion

It can be concluded that Reversible Logic is better in all respect like speed, delay, area, complexity, power consumption. However CMOS adder requires more power consumption and more number of components but delay for this Reversible adder is just a bit larger than CMOS adder. Hence for low power requirement and for less number of gate count requirement Reversible adder is suggested. Further the work can be extended for optimization of said adder to improve the speed or to minimize the delay.

6. Scope of Future Work

An improvement in addition speed by using new techniques can greatly improve system performance. This project can be extended for the reconfigurable architecture.

7. Acknowledgement

I wish to Prof. R. N. Mandavgane and other contributor to give their contribution for developing this topic related search. I also thankful to all the authors of different books which guide me a lot.

References

[1] "Low-Power And Area-Efficient Carry-Select Adder", B. Ramkumar And H.M. Kittur, / IEEE Transaction Very Large Scale Integration (VLSI) System, vol. 20, no. 2, PP. 371–375, February-2012.
[2] "Area–Delay–Power Efficient Carry-Select Adder", Basant Kumar Mohanty, Sujit Kumar Patel / IEEE Transactions On Circuits And Systems-II, Vol. 61, No. 6, June-2014.
[3] "Speed Efficeint Carry Select Adder For Mac Implementations",Arun.M.Thomas, Raghavendra Reddy / IJAERT, ISSN No.: 2348, March 28-29 2014.
[4] "Design Of 16 Bit Carry Look Ahead Adder Using Reversible Logic",Shailja Shukla, Tarun Verma, Rita Jain, / International Journal Of Electrical, Electronics And Computer Engineering ISSN No. (Online): 2277-2626 83-89 March-2014.
[5] "Low-Geometry High Speed Feyman Toffoli 8 Bit Carry Skip Adder D. P. Bala Subramanian, K.Kalaikaviya, S.Tamilselvan / Journal Of Global Research In Electronics And Communication, Volume 1, No. 1, November-December 2012.
[6] "Analysis Of Low Power, Area Efficient And High Speed Multiplier Using Fast Adder", Krishna Naik Dungavath, Dr V. Vijayalakshmi, / IJISET, Vol-1, Issue-4, June 2014.
[7] "Carry-select adder", O. J. Bedrij, IRE Transaction Electron Comput., pp. 340–344, 1962.
[8] "ASIC Implementation Of Modified Faster Carry Save Adder", B. Ramkumar, H.M. Kittur, And P. M. Kannan / Eur. J. Sci. Res.Vol. 42, No. 1, PP. 53–58, June 2010.
[9] "Carry-select adder using single ripple carry adder", / T. Y. Ceiang and M. J. Hsiao Electron. Lett., vol. 34, no. 22, pp. 2101–2103, October 1998.
[10] "Design Of 16 Bit Carry Look Ahead Adder Using Reversible Logic", Shailja Shukla, Tarun Sharma And Rita Jain / International Journal Of Electrical, Electronics And Computer Engineering 83-89, ISSN No.(Online):2277-2626, 2014.
[11] "Low Power, Area and Delay Efficient Carry Select Adder Using Bec-1 Converter" , Shaik Jabeen, K.Upendra Raju / International Journal of Engineering Research and Development, ISSN: 2278-067X, P-ISSN: 2278-800X, Volume 8, Issue 2PP. 01-07, August 2013.
[12] "Improved Carry Select Adder With Reduced Area And Low Power Consumption", Padma Devi, Ashima Girdher, Balwinder Singh/ International Journal Of Computer Application, Volume-3, June-2014.
[13] "A Low Power Carry Select Adder With Reduced Area", K. Rawwat, T.Darwish, M.Bayoumi / Proc. Of Midwest Symposium And Circuit On Systems, 2001.
[14] "Carry Select Adder", O.J.Bedrij/ IRE Trans. Electron. Computer. Pp.340-344, 1962.
[15] "Carry–Select Adder Using Single Ripple Carry Adder", I Electron. Lett, Vol-34, No-22, pp.2101-2103, Oct-1998.

Author Profile

Mr A. D. Rewatkar received the Bachelor of Engineering degree in Electronic Engineering from R.T.M. Nagpur University, Wardha in 2013 and pursuing his M.Tech in Electronic Engineering (communication) from S. D. College of Engineering, Wardha, R.T.M. Nagpur University. He is working towards M.Tech research project at R.T.M. Nagpur University. He is currently working as a Lecturer in Electronics Engineering Department at S. D. College of Engineering, selukate Wardha. His area of interests include VLSI design and optimization.

Mrs. Rajashree N. Mandavgane received her B.E degree and M.Tech degree from R.T.M.N.U University, Maharashtra, India. She is presently working as Associate Professor and Head in the department of Electronics and Tele-Communication Engineering, at B. D. College of Engineering, sewagram Wardha. She is having a total 23 years of teaching experience. With a subject specialization in general and digital electronics.

Mr. S. R. Vaidya received his Bachelor of Engineering degree and M.Tech degree from R.T.M.N.U University, Maharashtra, India. He is presently working as Assistant Professor and M-Tech Co-ordinator in department of Electronics Engineering, at S. D. College of Engineering, selukate Wardha, He is having a total 6 years of teaching experience. His areas of interest include High performance VLSI Design and VHDL based system design..