International Journal of Science and Research (IJSR)
ISSN (Online): 2319-7064
Index Copernicus Value (2013): 6.14 | Impact Factor (2013): 4.438

Analysis of Modified Hybrid Full Adder with High Speed

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Abstract: ***In digital CMOS design, power consumption has been a major concern for several years advanced IC fabrication technology allows the use of nano-scale devices so inability to get power to circuits, power leakage or to remove the heat they generate. By optimizing the transistor size in each stage power and delay can be minimized. This paper presents the analysis of full adders having efficient parameters like PDP, power, delay by mean of power consumption and speed. These full adders were designed by various designs. Although these full adders were more efficient and better than the standard full adder but these adders are stimulated using 90nm, 180nm CMOS technologies by using various tools like TSPICE tool, cadence virtuoso, and synopsis. This purposed circuit reports with better performance parameters like low delay (213.78 ps), high speed better PDP (0.642fj) with lesser power consumption(3.007μW) at 180nm CMOS technology using TPL(transmission pass logic) and CMOS(complementary metal oxide semiconductor) logic designs. The circuit is first implemented at 1bit full adder and then extended to 32 bit ripple carry adder also on tanner EDA tool.***

Keyword: advanced VLSI, TPL, High speed, full adder, PDP, CMOS, ALU, RCA

1. Introduction

Today demand and popularity of portable devices is increasing that depends on high speed, small size, high reliability, low power consumption and longer battery life that demand for VLSI. Number of transistor is the primary concern in the complex devices as it affects the area and speed directly.
Full adder is a basic building block for every arithmetic circuit and is essential in digital signal processing, microprocessors or ALUs. Almost every complex computational circuit requires full adder circuit

1.1 Classification of full adder

Designs classified may be static and dynamic full adders. Static full adders are reliable, require less power but on the cost of area. Where dynamic full adders have high driving capability, low power, low input capacitance and high speed operation but power dissipation due to higher switching activities [27] they require N+2 transistors for N input logic function instead of 2N transistors required by
standard adder as they engage only NMOS transistors and due to absence of PMOS input capacitance is lower but dynamic full adder suffer from charge sharing ,complexity and high power[4],[5] requirement due to high switching so a hybrid style will embed the both static and dynamic full adder to get better results.

1.2 Standard 1 bit full adder

Two binary inputs A,B taken to get their sum as output by using XOR gate and carry is taken out by using AND,OR gates. This block diagram can be represented in circuitry form as given in fig 2.

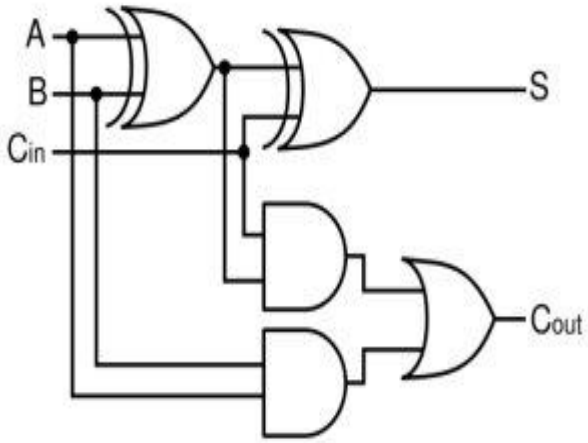


Fig1: block diagram of full adder

Formulas for the calculation of sum and carry for full adder can be defined as: [28]

Where A, B, Cin are the inputs and Sum and Carry are the outputs of the full adder

$$Sum=A\oplus B\oplus Cin, \quad (1)$$

$$Cout=A\cdot B+Cin\cdot(A\oplus B). \quad (2)$$

Standard CMOS based 28transistor full adder have a ability to work against voltage scaling and transistor sizing but its demerits are requirement of buffers and high input capacitance to overcome this with less number of transistor a new design is required to be proposed.[4]

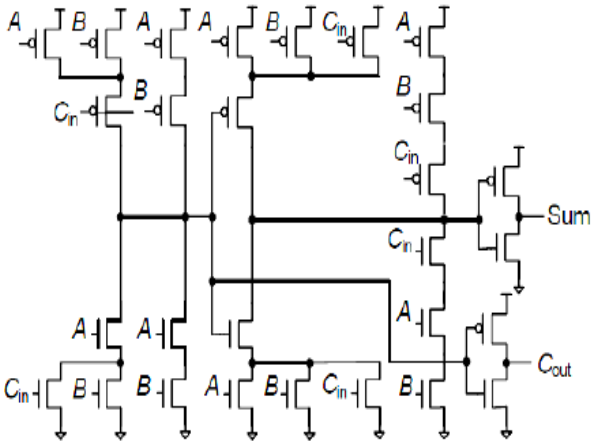


Figure 2: Standard CMOS adder with 28 transistors

1.3 Existing designs:

Different technologies are used those have their own merits and demerits. There is always a trade of between performance parameters to improve overall performance as standard static CMOS [4], dynamic CMOS [5], CPL complementary pass transistor logic [6] [7], transistor gate full adder [8] [9], hybrid logic design [10]. standard CMOS based adder with 28 transistor is capable of rousting against voltage scaling and transistor sizing while its high input capacitance require buffer [4] so to overcome smart design is mirror adder[5] with the approximately same power consumption and transistor count as of [4] but the advantage over [4] is low delay . On the other hand CPL with 32 transistors shows good voltage swing resonation but it have more transistors, slow speed and it could not be used for low power application[6][7] because of overloading of its input and voltage degradation that was overtaken by TGA, with 20 transistors but still high power consumption and area requirement are the major concern to be overcome so it was done by hybrid full adder that was based on merging the two existing technologies to improve the performance led to evolution of hybrid pass logic with static CMOS output drive full adder circuit (HPSC) [12] where XOR and XNOR functions were simultaneously generated by PTL module by the use of 6 transistors and passed to CMOS module to get voltage swing on the trade off with increased number of transistors and decreased speed.

2. Design Approach for the Proposed Circuit

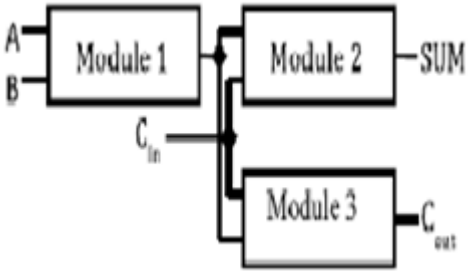


Figure 3: block diagram of full adder

The proposed full adder circuit is represented by three blocks as shown in Fig.3. Module 1 is complementary CMOS logic for the XOR gate functioning and module 2 is the TPL logic for XNOR functioning that generate the sum signal (SUM) and module 3 generates the output carry signal (Cout) by using TPL logic. Each module is designed and stimulated individually such that the entire adder circuit is optimized in terms of power, delay, and PDP.[25]. Now this new purposed circuit is configured with a complementary CMOS logic for XOR gate functioning that is been followed by inverter again followed by TPL design logic.

The design implementation for the modified 1bit hybrid full adder at 180 nm CMOS technology for the average power and delay reduction at Tanner EDA tool and then further extending this work to 32 bit hybrid full adder at 180 nm CMOS technology. For this results are shown by bar graph in table 1-3 and figures 4, 5 are shown for the modified circuit. Table 5 shows the comparison of modified design with respect to other different designs technologies of CMOS for performance factors like number of transistor used, PDP, average power consumption and delay.

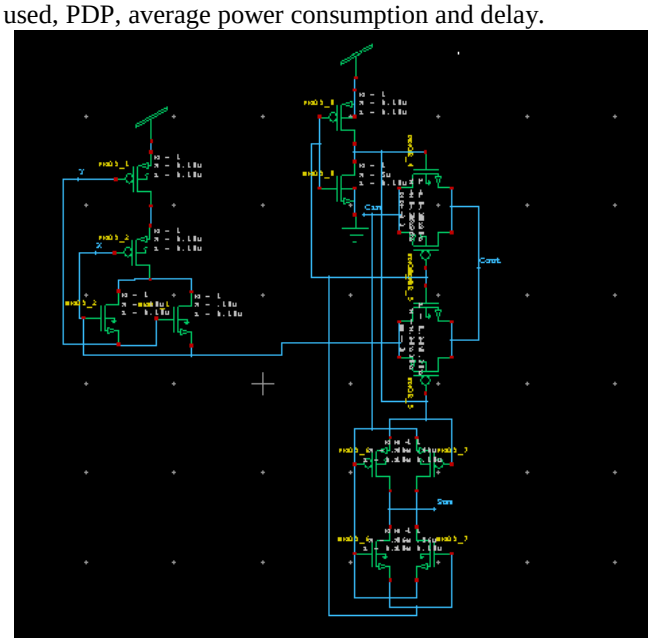
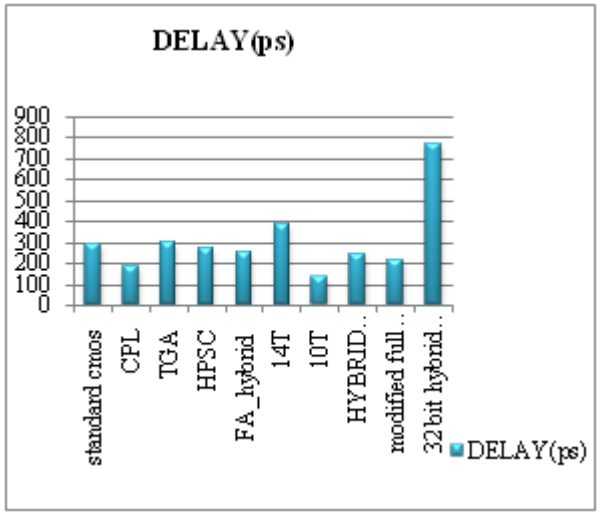


Figure 4: Modified full adder at 180nm CMOS technology

Delay had been reduced to (213.78 ps) by modified new circuit a graph has been shown to represent the delay with different designs and our design

Table 1: Representing delay for different designs at 180nm technologies of full adder



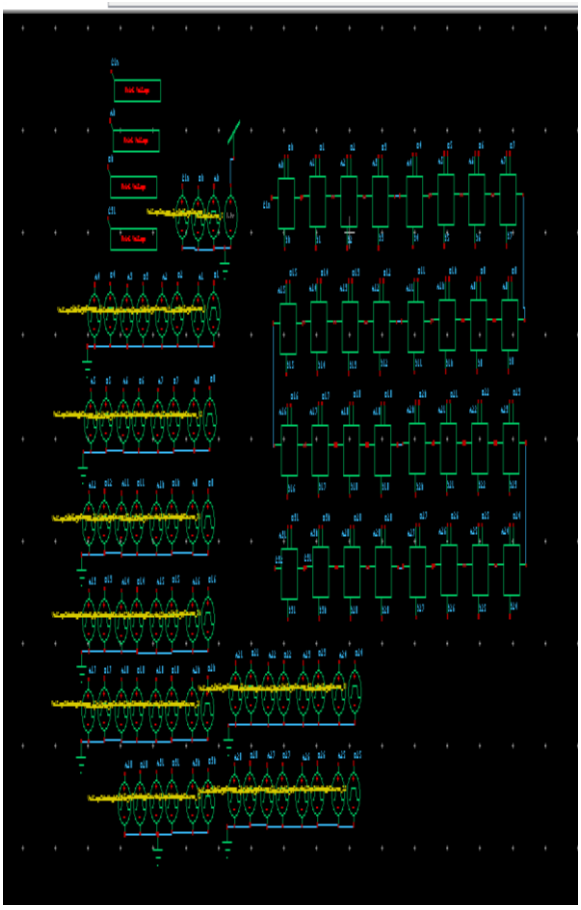
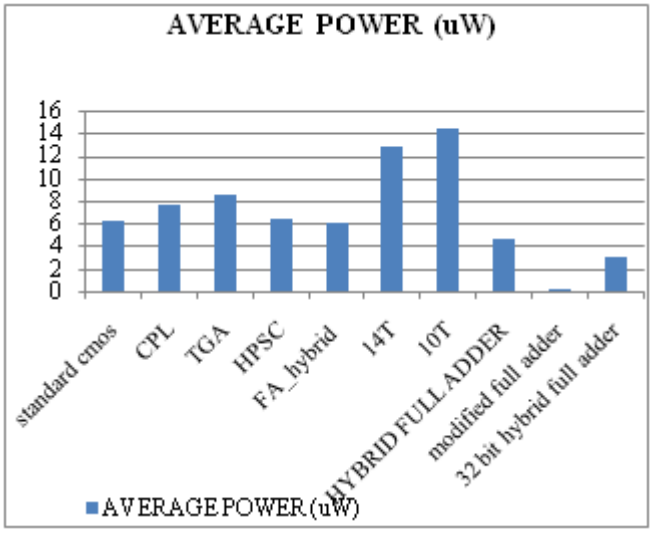


Figure 5: Implementation of modified 1bit full adder to 32 bit RCA full adder at 180nm CMOS technology

2.1. Reducing Power Consumption

The power consumption can be reduced by implementing low power techniques on full adder circuit with less transistor logic have widely used to reduce power consumption [1-2].such design suffer with output signal degradation and cannot sustain low voltage operations[3].At device level, reducing the supply voltage and threshold voltage accordingly would reduce the power consumption but low supply voltage increase the circuit delay and degrades the drivability of circuit whereas by selecting proper W/L ratio we can minimize the power dissipation without decreasing supply voltage. Power dissipation could be static dissipation or dynamic dissipation. Static dissipation occurs due to the leakage current or current drawn continuously from power supply and dynamic dissipation that occurs due to charging and discharging of load capacitance. So we calculated the average of both the powers static and dynamic too by changing W/L ratio. Average power consumption for the circuit at 180nm technology is 3.007µW.

Table 2: Representing the comparison of average power of different designs



Tables have been shown to represent the average power reduction and PDP reduction of different technologies

Table 4: Representing the comparison of performance parameters of different designs for full adder

Technologies	*Delay (ps)*	*Avg Power (µW)*	*PDP (fj)*	*Tran. used*
Standard CMOS	292.1	6.2199	1.816	28
CPL	183.97	7.7198	1.42	32
TGA	293.9	8.4719	2.8989	20
HPSC	273.7	6.378	1.746	22
FA_hybrid	252.3	5.978	1.508	24
14T	381.7	12.72	4.855	14
10T	132	14.344	1.902	10
Hybrid full adder	241.25	4.6	0.931	16
32 bit RCA modified	765.33	0.17	0.13	448
Modified full adder 180nm	213.78	3.007	0.642	14

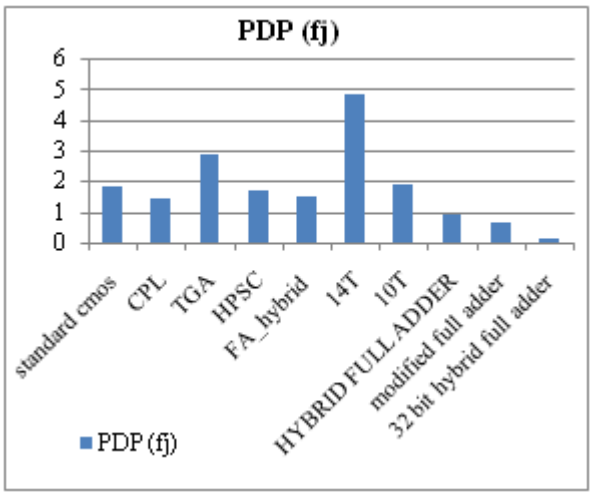


Table 3: Representing the comparison of PDP of different designs

3. Performance of Modified Hybrid Full Adder

Delay improvement of 11.16% for modified 1 bit full adder as compared to best design for hybrid full adder [25] and average power consumption reduction to 34.63% due to removal of ground . as a ground always waste the power .A

32-bit carry propagation adder is implemented as an extension of the proposed 1-bit full adder. It is a non carry look-ahead adder structure where the carry propagation takes place every time till the last adder block.

4. Conclusion

In this paper, a low-power high speed modified hybrid 1-bit full adder has been proposed the design has been extended for 32-bit ripple carry adder also. The simulation was carried out using Tanner EDA tool with 180nm technology and has been compared with other standard design approaches like CMOS, CPL, 14T, TGA, and other hybrid designs. The simulation results established that the proposed modified adder offered improved PDP, delay, power consumption compared with the earlier reports. The efficient coupling of strong transmission gates driven by TPL complementary CMOS logic and removal of ground lead to fast switching speeds (213 ps at 1.8-V supply) in 180 nm technology) excluding buffer. The proposed full adder offered 24.14% improvement with respect to the best reported design [25] in terms of PDP (180-nm technology at 1.8 V). The proposed full adder was further used to implement a 32-bit ripple carry propagation adder at 180nm technology at 1.8V.

5. Acknowledgement

The author would like to thank the Om institute of technology, Hisar, India for providing guidance.

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