32-bit carry propagation adder is implemented as an extension of the proposed 1-bit full adder. It is a non carry look-ahead adder structure where the carry propagation takes place every time till the last adder block.

4. Conclusion

In this paper, a low-power high speed modified hybrid 1-bit full adder has been proposed the design has been extended for 32-bit ripple carry adder also. The simulation was carried out using Tanner EDA tool with 180nm technology and has been compared with other standard design approaches like CMOS, CPL, 14T, TGA, and other hybrid designs. The simulation results established that the proposed modified adder offered improved PDP, delay, power consumption compared with the earlier reports. The efficient coupling of strong transmission gates driven by TPL complementary CMOS logic and removal of ground lead to fast switching speeds (213 ps at 1.8-V supply) in 180 nm technology) excluding buffer. The proposed full adder offered 24.14% improvement with respect to the best reported design [25] in terms of PDP (180-nm technology at 1.8 V). The proposed full adder was further used to implement a 32-bit ripple carry propagation adder at 180nm technology at 1.8V.

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