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Software Defined Radio Signal Detector Implementation using FPGA

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Abstract: ***Signal detection is the very critical task upon which the entire operation of the radio device rests. Software-Defined Radio (SDR) is a technology that most of traditional radio applications are implemented in software. It has the advantages like re-configurability and flexibility, SDR system has to face a critical challenge of realtime processing due to high sampling rates and latency. Signal detection methods in radio signal detection has gained new aspects with awareness of cognitive radio systems. The requirement of spectrum sensing has been eliminated recently by FCC. The objective is to increase the bandwidth, keep low latency and reduce the power consumption without reducing the flexibility of a software radio. The implementation of signal detector on FPGA would reduce the power consumption due to signal processing done on a software defined radio by a host computer and increase data rate of a software radio. This is justified by developing application of aircraft tracking and FM.***

Keywords: FPGA, SDR, Cognitive radio, Low power.

1. Introduction

Spectrum scarcity is a serious worldwide concern today. The majority of RF spectrum is already allocated and obtaining new blocks of frequency at affordable costs is often infeasible. While these frequencies are actually licensed, the licensed users or primary users (PUs) do not continuously transmit in their respective bands [1]. This is an opportunity for the reuse of the licensed but vacant spectrum, for which new techniques and tools must be devised. The rapidly emerging field of cognitive radio (CR) is one enabling technology that allows secondary or cognitive radio users to transmit when the spectrum is judged to be available, without interfering with the ongoing transmission of the PUs [2]. In figure 1, we show a representative diagram of five PU's and the time / frequency map of the RF transmissions of this PU. It can be observed that there are "white spaces" where the PU's are not emitting RF energy, which we call spectrum holes. An interesting and challenging responsibility of a CR is locating and cataloging PUs. This is achieved by spectrum sensing already. In 2008 the requirement of spectrum sensing has been eliminated recently by FCC [4]. To the best of our knowledge this is the first paper presenting hardware implementation of spectrum sensing algorithm which makes it possible to achieve appreciable reduction in power dissipation without compromising the performance and sensing ability of a radio device.

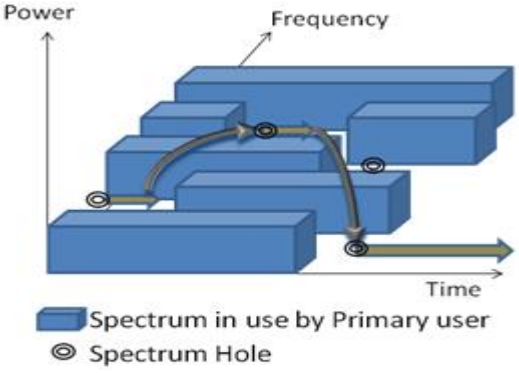

Figure 1: Spectrum allocation map

The power consumed by a software defined radio is enormous, as all the signal processing and detection is done on the host computer.

This power minimization problem can be solved by developing signal detection and identification algorithm which can be totally be implemented on a hardware. This can be achieved by implementing a combined algorithm, energy detector [5] for detection of spectrum occupancy and cyclostationary detector for detection of pattern of the wave received and its type of user detection (Primary or secondary).

The newly available RTL-SDR devices have low latency, consume low power and the loss of data is also low. However the band width and the available features can be improved without changing the features of the RTL-SDR device.

This algorithm is hardware implementation for signal detection and further communication process to be done by the host computer as represented in fig 2.

This paper is divided into three parts initially the implementation on a FPGA, Secondly aircraft tracking application and lastly the combined process and its power and silicon area usage on a FPGA.

2. Implementation

Most of the power in a software defined radio is utilized for the spectrum sensing and signal detection algorithms on the host computer. Usually these devices have high end processors consuming high power. Utilizing these devices for signal detection and signal processing is not appreciable. Developing a dedicated hardware for signal detection will be an appropriate solution. The available algorithms can be implemented on a FPGA or by using a DSP. FPGA's have fine granular advantage and reconfigurable capability,

allowing more simplification and speed to the signal processing.

The signal to be detected is sensed by energy detector algorithm for an initiated signal in the spectrum. This sensed signal may be of any radio service irrespective of the service we desire. This distinguishing of required service and received service is done by the cyclostationary algorithm [6]. The patterns for a certain service consists of a cyclic prefix etc.; the ideal patterns can be stored in LUT's on a FPGA, used for autocorrelation with the received signal and the service can be distinguished from unnecessary services and the spectrum user type can be easily determined. This combined algorithm implementation on a FPGA allows further upgrade of the more pattern for different environments of radio service.

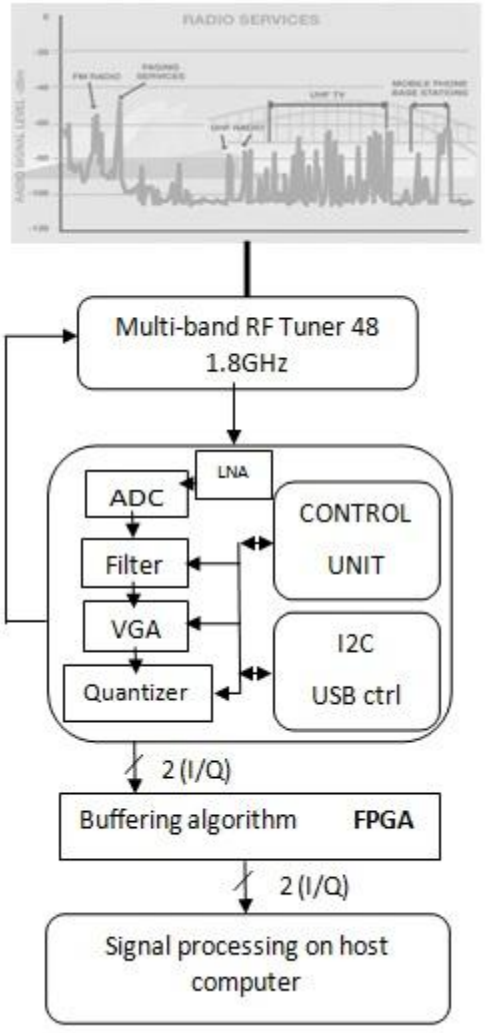

Figure 2: Signal detector block diagram

A. Energy detection on a FPGA.

The energy detection algorithm [5] block diagram which can be implemented on a FPGA is presented in Fig. 3 It consists of two multipliers to perform operations on both real and imaginary signals and a digital integrator (summation product). The energy detector is the simplest signal detection algorithm on hardware and less complex then other implementations. Its power consumption is maximum contributed by the multipliers for computing the square of the absolute value of the input signal in equation 1.

$$PE = \frac{1}{N}\sum_{n=0}^{N-1}|x(n)|^2 \quad \text{..... Equation 1}$$

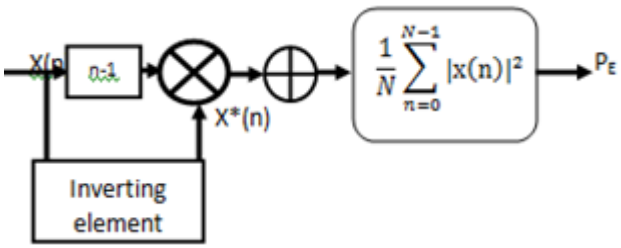

Figure 3: Energy detector block.

B. Cyclostationary pattern reorganization on a FPGA.

The typical structure of an OFDM symbol is as shown in Fig. 4 The OFDM symbol with a length Ns, consists of the actual data contents having a length N_D and a cyclic prefix having length N_{CP}. This cyclic prefix is a copy of N_{CP} denoted as 'A' in the figure. Samples from the end of the symbol are added to the front of the symbol in order to reduce inter-symbol-interference and improve the system performance in a multipath propagation environment. The cyclic prefix can also be used for synchronization [7].

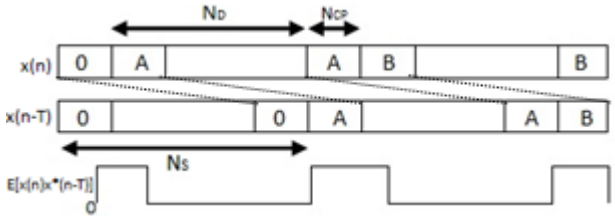

Figure 4: General OFDM symbol structure with data and cyclic prefixes

The resemblance of the signals between available ideal signal pattern and the received signals can be done by using cross-correlation between the signals. The correlation function can be computed as,

$$A_{x(n)x_i(n)} = \frac{1}{N}\sum_{\tau=0}^{n} x(n)x_k^*(n-\tau) \text{.. Equation 2}$$

K = 0, 1, 2, 3…k

This algorithm is most suitable for implementation on FPGA. We need to have database of the prefix of the various services this can be done by the LUT's banks available on FPGA. The signal rate is high for the received signal; this has to be in a FIFO for successive samples of the signal of neighboring frequencies.

The signal x(n) is then cross correlated with signals $x_1(n)$, $x_2(n)$, $x_3(n)$, $x_4(n)$,…$x_T(n)$; respectively as represented in Figure 5. This is achieved by using matrix convolution method as the signals have both real and imaginary components. The imaginary components can be further derived from equation 2 as,

$$A_{x(n)x_i(n)} = \frac{1}{N}\sum_{n=0}^{N-1} x(n) + j\, y_k(n) \text{ ..... Equation 3}$$

$$= X + jY_k \text{ ..... Equation 4}$$

A complex matrix can be formed by using the above equation, with opposite elements the conjugate of each other i.e; $A_{ij} = -A_{ji}$. Output of the cyclostationary block is the signal whose correlation is below threshold point (ideally = 0).

The service of the signal can be detected by this cyclostationary block. For a dedicated service application the service for which the signal has to be detected is the only correlation factor for the detected signal.

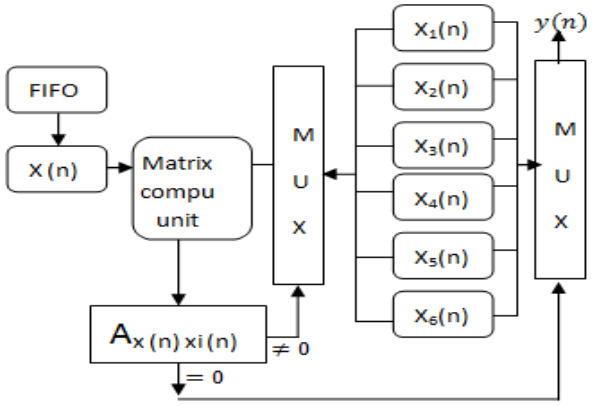

Figure 5: Cyclostationary block.

C.Power consumptions and logical hardware resource utilization.

The implementation of the signal detection algorithm on a FPGA reduces power consumptions as power consumed by high end processors on a software radio device is high [8]. This hardware implementation is simplified and simulated Spartan 6 FPGA on Xilinx.

D. Experimentation.

The device contains three components
(1) The Tuner (Raphael Micro R820T radio tuner) and
(2) An 8-bit ADC and USB data pump (Realtek RTL2832U)
.
(3) FPGA spartan 6 board.

The tuner chip serves as the radio frequency (RF) front-end for the SDR. Following a miniature coax connector for the antenna is a low noise amplifier (LNA) providing a noise figure (NF) of about 3.5 dB. The tuning range of the R820T is 24 MHz to 1850 MHz. In the RTL2832U digital signal processing (DSP) takes place this includes additional filtering and down sampling of the IF signal initially delivered by the R820T. The ADC on RTL2832U produces 8-bit real/inphase (I) and imaginary/quadrature (Q) interleaved sample values, in an unsigned format. The sample they are finally converted to signed 8-bit values and parallel I and Q streams are available at the Output. The signal conversion, detection and buffering implementation is done on the FPGA. The RS232 HDL module available at http://www.ics.uci.edu/ is used to communicate with the host computer.

	Current	Aircraft ID	Flight ID	Latitude(deg)	Longitude(deg)	Altitude(ft)	Speed(knots)	Direction	U/D
1		800400	AIC513	18.4106	73.8407	12150	336	S (162)	1344
2		8005DE	IGO134	18.8247	74.0095	13025	352	NE (33)	3072
3		80074D					427	S (176)	0
4		70C0AD	OMA822	17.7146	73.2353	41000	470	NW (297)	0
5	✓	80068B	IGO407	18.5912	73.8101	5300	261	W (275)	1728
6		896211					514	NW (297)	0

Figure 6: Aircraft beacon decoding results

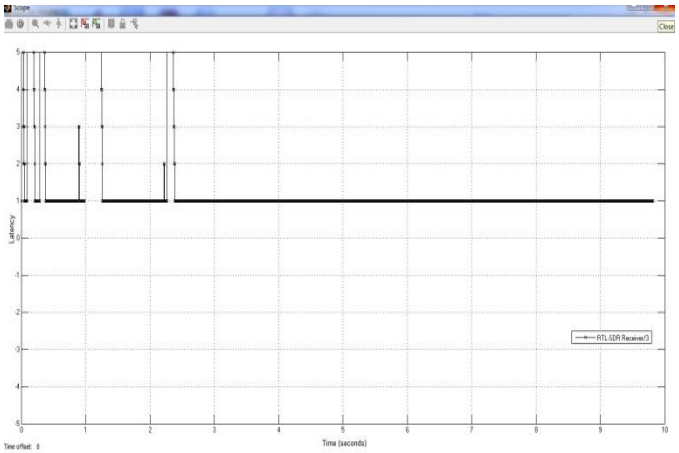

Figure 7: Latency w.r.t. time plot.

To verify the theory aircraft deacon detection and decoding application is developed for an S-mode beacon. The decoding of s-mode signal have a fixed signal pattern as defined in aircraft collision avoidance system (ACAS).
Mode-S signaling scheme has the following properties:
Transmit Frequency: 1090 MHz
Modulation: Pulse Position Modulation
Data Rate: 1 Mbit/s
Short Message Length: 56 microseconds
Long Message: 112 microseconds
Short messages contain the information like Message Type (Short or Long), Aircraft ID (Unique 24-bit sequence), CRC Checksum. Long messages contain all the information in a short message and optional information such as Altitude, Position, Direction and Velocity

synced_fifo Project Status (05/13/2015 - 12:29:09)			
Project File:	fifo_sdr.xise	Parser Errors:	No Errors
Module Name:	synced_fifo	Implementation State:	Synthesized
Target Device:	xc6slx45t-3fgg484	• Errors:	No Errors
Product Version:	ISE 13.2	• Warnings:	No Warnings
Design Goal:	Balanced	• Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:	
Environment:	System Settings	• Final Timing Score:	

Device Utilization Summary (estimated values)			[-]
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	25	54576	0%
Number of Slice LUTs	54	27288	0%
Number of fully used LUT-FF pairs	25	54	46%
Number of bonded IOBs	22	296	7%
Number of BUFG/BUFGCTRLs	1	16	6%

Figure 8: Design summary.

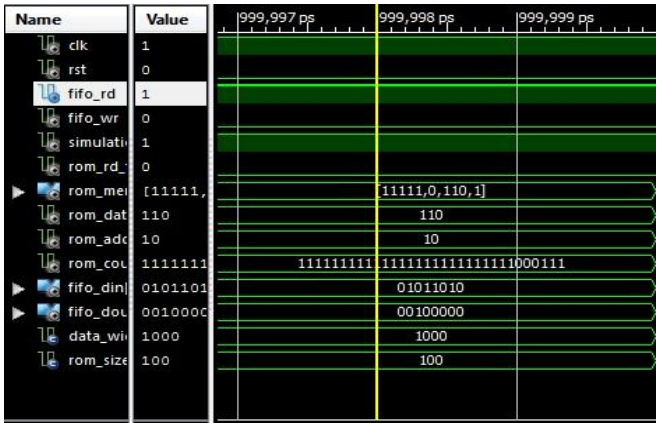

Figure 9: VHDL design simulations.

Table 1: Result obtained by VHDL design tools

Implementation	Power	Logic	Registers
Energy detector	2.82mW	612	290
Cyclostationary	32.38mW	6779	1060
FIFO	0.46mW	79	25

3. Conclusion and Result

The complexity of logic is based on the numbers reported by the design tool, includes the amount of a four-input LUT. The design tool reports the power consumed by the algorithm on watt. Table 1 shows the results obtained by VHDL design tools. Figure 6 shows the decoded aircraft beacon signals in real time which includes aircraft ID, Flight ID, latitude longitude, altitude, etc.

The latency is much higher than the traditional SDR for 2.5sec due to the use of FPGA in the path, after which the latency is constant and low as in the traditional SDR. The bandwidth is increased by 12 percent and the loss of packet is negligible and can be ignored.

4. Future Work

This device that is used for spectrum sensing in present applications merging this signal detection method will reduce device complexity and the power consumed by traditional SDR and the host computer together. With this implementation, software device independent signal detection standalone hardware can be developed as ready to use board for any cognitive radio communication device.

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