



Figure 9: VHDL design simulations.

Table 1: Result obtained by VHDL design tools

Implementation	Power	Logic	Registers
Energy detector	2.82mW	612	290
Cyclostationary	32.38mW	6779	1060
FIFO	0.46mW	79	25

3. Conclusion and Result

The complexity of logic is based on the numbers reported by the design tool, includes the amount of a four-input LUT. The design tool reports the power consumed by the algorithm on watt. Table 1 shows the results obtained by VHDL design tools. Figure 6 shows the decoded aircraft beacon signals in real time which includes aircraft ID, Flight ID, latitude longitude, altitude, etc.

The latency is much higher than the traditional SDR for 2.5sec due to the use of FPGA in the path, after which the latency is constant and low as in the traditional SDR. The bandwidth is increased by 12 percent and the loss of packet is negligible and can be ignored.

4. Future Work

This device that is used for spectrum sensing in present applications merging this signal detection method will reduce device complexity and the power consumed by traditional SDR and the host computer together. With this implementation, software device independent signal detection standalone hardware can be developed as ready to use board for any cognitive radio communication device.

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Author Profile



Rohan Antony Fernandes received B.E. from Dr.JJMCOE, Jaysingpur, India. Having teaching experience of 02 Years. Currently research fellow at Department of electronics, MIT Academy of engineering, Pune.



Mrs. S. M. Mahamuni, received M.E. from J. N. E. C. Aurangabad, India. Having teaching experience of 11 Years. She is currently assistant professor at MIT Academy of engineering, Pune. Registered for Ph.D. in wireless communication at SVNIT, Surat, Gujrat. Currently working on BCUD funded Research project 11EG000378 titled "Spectrum Sensing in Cognitive Radio Network".