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Analysis of Low Power Pulse Triggered Flip Flop

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Abstract: ***Flip Flops are critical timing elements in digital systems which has large impact on circuit speed and power consumption. The performance of flip flop is an important parameter to determine performance of whole synchronous circuit. In this paper, comparison of existing flip flops with different parameters is calculated. A new design a low power pulse triggered flip-flop (FF) has been proposed having a structure of explicit pulse triggered flip flop with a modified true phase single latch based on single feed through scheme. Pulse Triggered FF has a simple circuit which lowers the power consumption. The simulation is done on TANNER EDA using 90nm technology which verifies that Setup time, Hold time, D to Q delay, Average Power and optimal PDP has been reduced when compared with existing systems. P-FF gives a higher toggle rate for high-speed operations. The flip flop has shortened the delay, power etc which improves the speed, efficiency and power of the system.***

Keywords: Flip Flop (FF), low power pulse triggered flip flop, explicit pulse data close to output (ep-DCO)

1. Introduction

Flip Flops are basic memory elements used in sequential circuits. FFs are basic storage elements extensively used in all digital designs. In the present world, power consumption is a major challenge in digital design. FF is divided into two stages clock system and latch which stores data. Clock system consumes 50% of the total power which is due to the fact that dynamic power in MOS circuit is directly proportional to the switching activity. To overcome this problem Pulse triggered flip flop is introduced because single latch is better than conventional master slave flip flop and transmission gate (TG). P-FF is simple in circuit complexity. This leads to a high toggle rate for high speed operations. P-FF allows time borrowing across clock boundaries and features a zero or even negative setup time. Several flip-flop designs have been proposed for power reduction. The power, delay, and reliability of the flip-flops directly affect the performance and fault tolerance of the electronic system [1]. Therefore, it is necessary to carefully design flip flops for minimum area, delay, power, and maximum reliability. Several flip-flop designs have been proposed for power reduction. Some of these designs require a large number of transistors for implementation, resulting in a large area not necessarily suitable for small, low-priced systems. Some of these designs require a large number of transistors for implementation, resulting in a large area, not necessarily suitable for small, low-priced systems. It is important to reduce the power dissipation in both clock distribution networks and flip-flop[2][3]. Master-slave flip-flops, sense amplifier based flip-flops and pulsed-triggered flip-flops are used in many existing microprocessors. Master-slave flip-flops consist of two stages, one is master and other is slave and they are characterized by their hard-edge property [4]. Master-slave flip-flops and sense amplifier based flip-flop are characterized by positive setup time, causing large D-to-Q delays. Pulse-triggered flip-flops reduces the above two stages into one stage and is characterized by the soft edge property and a negative setup time, resulting in small D-Q delay. In this paper, a new high performance, low power, low D to Q delay and with average power pulse triggered flip-flop is devised. The proposed pulse edge triggered flip-flop is compared with the conventional designs. For all circuits, simulations will be carried out in 90nm CMOS layout technology using Tanner tool EDA.

2. Existing Design

Flip-Flops and latches are the basic elements for storing information. The main difference between latches and flip-flops is that for latches, their outputs are constantly affected by their inputs as long as the enable signal is asserted. Flip-flops change their content at either at the rising or falling edge of the enable signal. This enable signal is used to control the clock signal. Pulse-triggered FF (P-FF) has been considered a popular alternative to the conventional master–slave based FF in the applications of high-speed operations [5]. Besides the speed advantage, its circuit simplicity is also beneficial to lowering the power consumption of the clock tree system. The circuit complexity of a P-FF is simplified since only one latch, as opposed to two used in conventional master–slave configuration, is needed. Pulse-triggered flip-flops can be classified into different types of flip-flops. Based on the pulse generators used, pulse-triggered flip-flops can be categorized into two types as: implicit-pulsed and explicit-pulsed. Pulse triggered flip-flops can be static, semi static, dynamic and semi-dynamic Pulse-triggered flip-flops can also be classified into single-edge triggered flip-flops and double-edge triggered flip-flops. In implicit-pulse triggered flip-flops (ip-FF), the pulse is generated inside the flip-flop. For example, hybrid latch flip-flip (HLFF), semi-dynamic flip-flop (SDFF), and implicit-pulsed data-close-to-output flip-flop (ip-DCO). Whereas, in explicit-pulse triggered flip-flops (ep-FF), the pulse is externally generated. For example, explicit-pulse data-close-to-output flip-flop (ep-DCO).

The three existing pulse Triggered flip flops are implicit data close to output (ip-DCO), Master Hybrid Latch Level Triggered flip flop (MHLLF), Single Ended Conditional Capture Energy Recovery (SCCER).

Fig.1 shows a classic explicit P-FF design, named data-close to- output (ep-DCO) [6]. It contains a NAND-logic-based pulse generator and a semi dynamic true-single-phase-clock (TSPC) structured latch design. In this P-FF design, inverters I3 and I4 are used to latch data, and inverters I1

and I2 are used to hold the internal node X. The pulse width is determined by the delay of three inverters. This design suffers from a serious drawback, i.e., the internal node X is discharged on every rising edge of the clock in spite of the presence of a static input "1." This gives rise to large switching power dissipation. To overcome this problem, many remedial measures such as conditional capture, conditional prechage, conditional discharge, and conditional pulse enhancement scheme have been proposed Fig. shows a conditional discharged (CD) technique. An extra nMOS transistor MN3 controlled by the output signal Qfdbk is employed so that no discharge occurs if the input data remains "1."

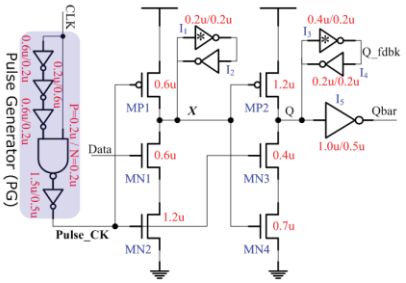

Figure1: ep-DCO

A figure 2 show a P-FF revised design and is named as Master Hybrid Latch Level Triggered Flip-flop (MHLLF) it is so called because a static latch structure is being employed. [14]. A pull-up transistor P1 is controlled by the FF output signal Q and is used to maintain the node level at high when Q is zero. This design eliminates the unnecessary discharging problem at node. However, it encounters a longer Data-to-Q delay during "0" to "1" transitions because node is not pre-discharged. Larger transistors N3 and N4 are required to enhance the discharging capability. Another drawback of this design is that node becomes floating when output Q and input Data both equal to "1" Node X is not precharged by the clock signal.

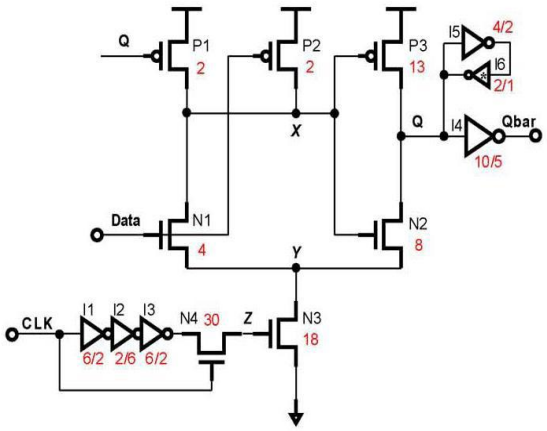

Figure 2: MHLFF

Fig 3 shows SCCER design, the discharge control signal is driven by a single transistor. Parallel conduction of two nMOS transistors (N2and N3) speeds up the operations of pulse generation. Thus the number of stacked transistors along the discharging path is reduced. To enhance the discharging condition, transistor P3 is added [9] When the FF output Q changes from 0 to 1 the conditional pulse enhancement technique effectively takes place. Thus this leads to the better power performance compared to the indiscriminate pulse enhancement approach.

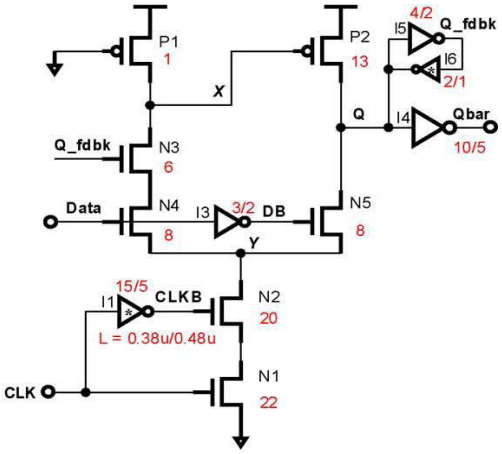

Figure 3: SCCER

Fig. 4 shows a conditional discharged (CD) technique. An extra nMOS transistor MN3 controlled by the output signal Q_fdbk is employed so that no discharge occurs if the input data remains "1[10] In addition, the keeper logic for the internal node X is simplified and consists of an inverter plus a pull-up pMOS transistor only."

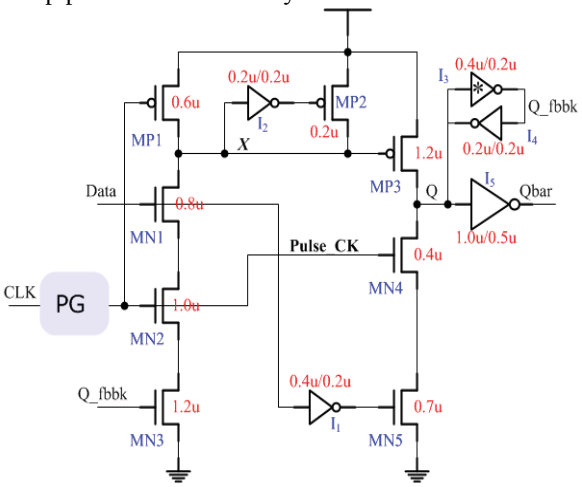

Figure 3: CDFF

3. Modified FF Design

The modified proposed P_FF design is shown in figure below. In previously proposed design the worst case timing occurs at 0 to 1 data transitions. Refer to figure 14, the proposed design also adopts a single feed through scheme to improve the delay. Similar to SCDFF design, the proposed design also employs a static latch structure and conditional discharge scheme to avoid switching at internal node. The proposed design consists of an extra pMOS to avoid 1 to 0 transitions and thus reducing parameters like D to Q delay, Average power, PDP Setup and Hold time etc. A conventional CMOS NAND-logic-based pulse generator design with a three-stage inverter chain as show in Fig. 1(a)] is used for all P-FF designs except the MHLFF design, which employs its own pulse generation circuitry. The amount of energy spent during the realization of a determined task related to PDP and stands as the more fair

performance metric when comparing optimizations of a module designed and tested using different technologies.

The target technology is CMOS 90nm. Since, pulse width design is crucial to the correctness of data capture as well as power consumption. The sizing also ensures that the pulse generators can function properly in all process corners. With regard to the latch structures, each P-FF design is individually optimized subject to the product of power and D-to-Q delay. To mimic the signal rise and fall time delays, input signals are generated through buffers. Since the proposed design requires direct output driving from the input source, for fair comparisons the power consumption of the data input buffer (an inverter) is included. Six test patterns, each representing a different data switching probability, are applied in simulations. Five of them are deterministic patterns, with 0% (all-0 or all-1), 12.5%, 25%, 50%, and 100% data transition probabilities, respectively.

Table 1: Comparison of various FF parameters

FF Design	*ep-DCO*	*Previously Designed*	*Modified*
No. of transistors	28	24	24
Setup Time	-149.15 ps	-196.63 ps	-64ps
Hold Time	195 ps	307 ps	323 ps
Minimum D to Q Delay	144 ps	106.78 ps	98 ps
Average Power (100% activity) uW	30.96 uW	32.58 uW	27.43 uW
Average Power (50% activity) uW	27.77 uW	24.01 uW	21.85 uW
Average Power (25% activity) uW	27.63 uW	19.72 uW	18.10 uW
Average Power (0% all-0) uW	16.22 uW	15.49 uW	14.24 uW
Average Power (0% all-1) uW	29.45 uW	14.56 uW	13.86 uW
Optimal PDP	3.43fJ	2.11 fJ	1.77 fJ

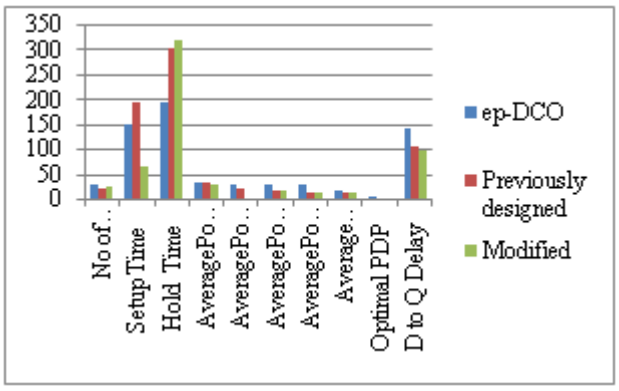

Figure 5: Comparison Chart of various FFs

4. Simulation Results

To evaluate the performance, FFs discussed in this paper is designed using 90nm CMOS technology. All simulations are carried out using Tanner EDA at nominal conditions. The schematic design of modified proposed design, Setup & Hold time using Tanner EDA is shown in figure 4, 5 & 6. From the simulation results, the advantage of the proposed design is obvious in all simulation trials.

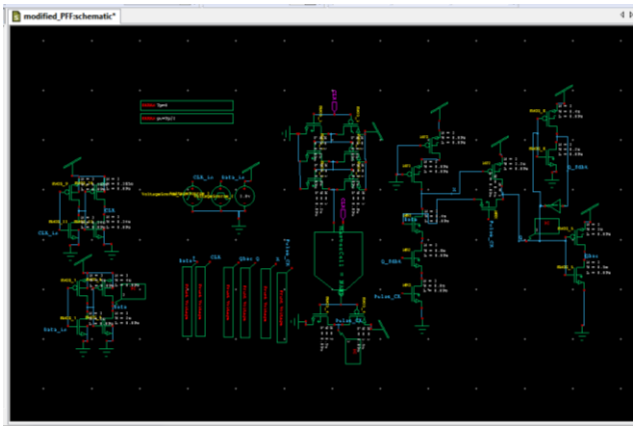

Figure 5: Modified Design P_FF Schematic using Tanner EDA

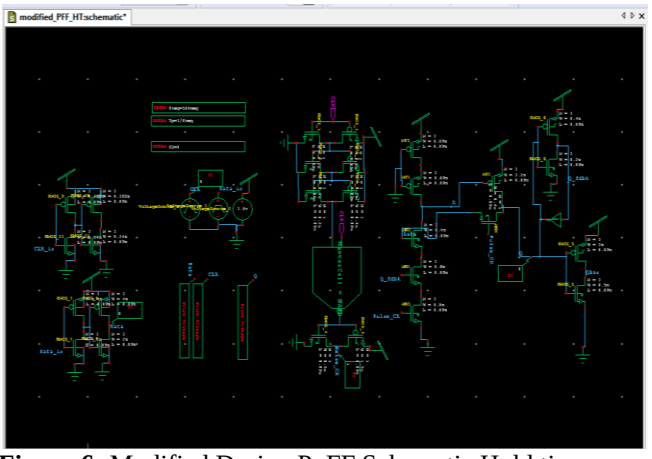

Figure 6: Modified Design P_FF Schematic Hold time

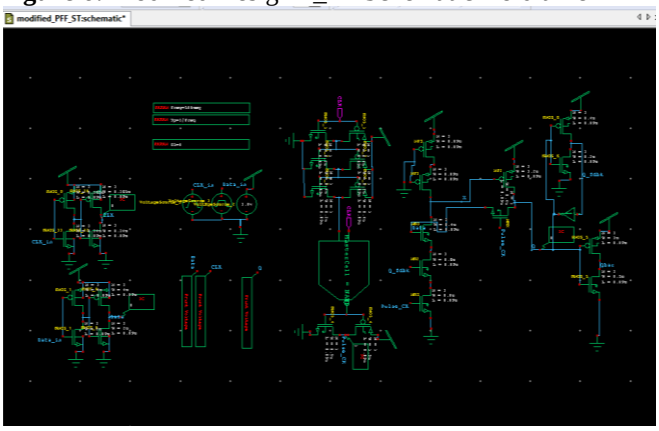

Figure 7: Modified Design P_FF Schematic Setup Time

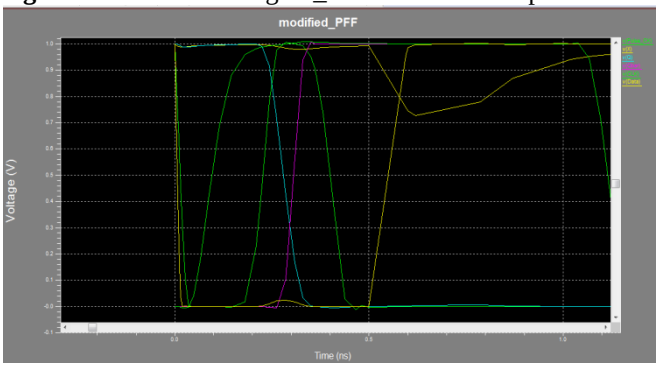

Figure 8: Waveform of Modified Design Schematic

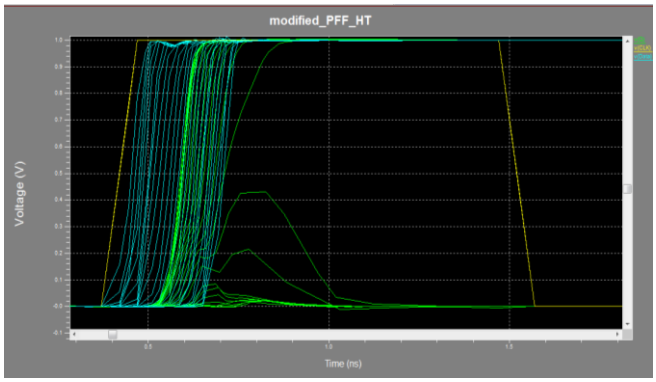

Figure 9: Waveform of Modified Design P_FF Hold time

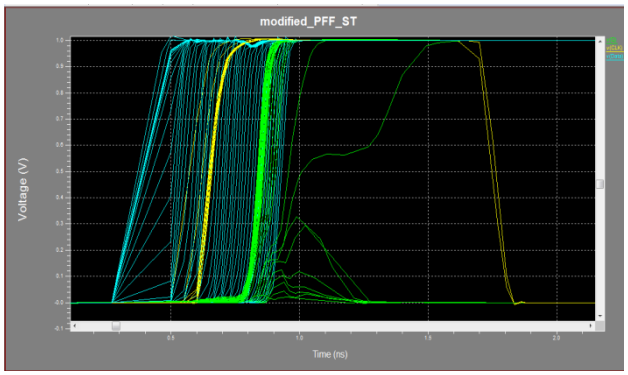

Figure 10: Waveform of Modified Design P_FF Setup time

The setup time of the modified design is -64 ps which is less from all other existing designs. From the simulation results, the advantage of modified design in obvious in all simulation trials.

5. Conclusion

This paper presents a new type of Pulse Triggered Flip Flop using 90 nm CMOS technology. A novel P-FF design employing modified TSPC latch structure incorporating a mixed style design consisting of pass transistor and pseudo nMOS logic. The combination of pass transistor and pseudo nMOS logic provides a short delay and fastest transition from 0 to 1 and 1 to 0 from data to output i.e. shortened transition time. The simulations results prove that it is far better than the designed discussed in the paper. The parameters like average power, delay, PDP, setup and hold time are reduced to an extent. The new design uses an additional pMOS in the system. It provides better D to Q delay. Setup time is better than many other flip flops and hold time is better than other explicit flip flops.

Future Work can be can be extended by working on parameters like area by reducing the number of transistor count also we can work on technology below 90nm.

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