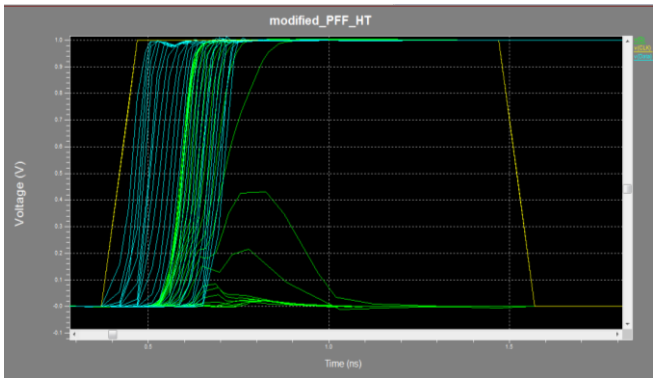

Figure 9: Waveform of Modified Design P_FF Hold time

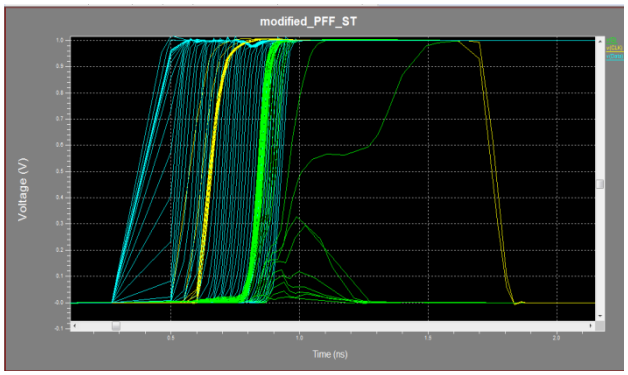

Figure 10: Waveform of Modified Design P_FF Setup time

The setup time of the modified design is -64 ps which is less from all other existing designs. From the simulation results, the advantage of modified design in obvious in all simulation trials.

5. Conclusion

This paper presents a new type of Pulse Triggered Flip Flop using 90 nm CMOS technology. A novel P-FF design employing modified TSPC latch structure incorporating a mixed style design consisting of pass transistor and pseudo nMOS logic. The combination of pass transistor and pseudo nMOS logic provides a short delay and fastest transition from 0 to 1 and 1 to 0 from data to output i.e. shortened transition time. The simulations results prove that it is far better than the designed discussed in the paper. The parameters like average power, delay, PDP, setup and hold time are reduced to an extent. The new design uses an additional pMOS in the system. It provides better D to Q delay. Setup time is better than many other flip flops and hold time is better than other explicit flip flops.

Future Work can be can be extended by working on parameters like area by reducing the number of transistor count also we can work on technology below 90nm.

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