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Grid Synchronizing Method Using 3-Level SVPWM of Grid Connected VSI

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Abstract: ***Renewable energy sources like wind, sun, and hydro are seen as a reliable alternative to the traditional energy sources such as oil, natural gas, or coal. Distributed power generation systems (DPGSs) based on renewable energy sources experience a large development worldwide. Due to the increasing number of DPGSs connected to the utility network, new and stricter standards in respect to power quality, safe running and islanding protection are issued. This paper analyzed the operation of synchronization grid connected VSI with the grid using SVPWM method. The paper also gives an overview of synchronization methods and a discussion about their importance in the control.***

Keywords: distributed generation;SVPWM; phase locked loop; utility synchronizaton;utility interface

1. Introduction

The injected current into the utility network has to be synchronized with the grid voltage. Therefore grid synchronization algorithms play an important role for distributed power generation systems. The synchronization algorithm mainly outputs the phase of the grid voltage vector which is used to synchronize the control variable, e.g. grid currents with the grid voltages using different transformation modules.

Various phase angle detecting methods have already been developed and reported in [1]-[7], [9], [10]-[12], [13]. Among these technique the voltage zero-crossing is the simplest one and the phase-locked loop (PLL) based technique are the state of art technique in detecting the phase angle of the grid Voltages.

2. Material and Methods

A. Filtering Algorithms

Filtering the grid voltages in a α-β stationary reference frame or in a d-q synchronous rotating reference frame is a simple way to detect the phase angle of the grid voltage.

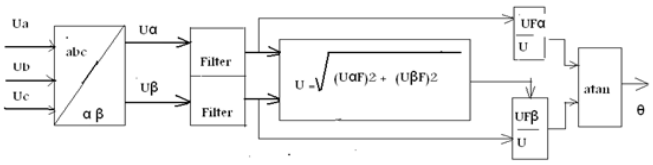

Figure 1: Synchronization method using filtering on α-β stationary frame

Three phase voltages are transformed to the α-β reference frame and filtering is as low pass filter (LPF), notch filter, space vector filter, etc. It is a well-known fact that filtering causes delay which is unacceptable especially for detecting the grid voltage angle [1]. Therefore care must be taken into consideration when designing such filters. When design the filters a trade-off should be made between the robustness and the transient convergence speed. A smaller cut-off frequency results in less distortion in the estimated angle. However this results in a slower rate of convergence. Filtering techniques in the d-q reference frame are easier to design since voltage components are dc variables Figure2. Various filtering techniques including notch filter, LPF, band-stop filter, etc. have been introduced in the rotating d-q reference frame. Major deficiencies of filtering methods include their bad performance in case of grid frequency deviations or voltage unbalance situation [1].

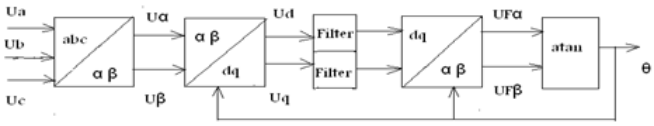

Figure 2: Synchronization method using filter on d-q synchronous reference frame

B. The Adaptive Notch Filter (ANF)

ANF is a basic adaptive structure that can be used to extract the desired sinusoidal component of a given periodic signal by tracking its frequency variations [2], [12]. For three-phase applications, three ANFs can be employed to provide the fundamental component, its phase angle and its frequency for each voltage phase [12].

The ANF is composed of simple adders, multiplier and integrators. The output provides the fundamental frequency of the input signal and the amplitude of the fundamental component is calculated using two additional multipliers, a summer and a square-root function. The sin/cos functions of the phase angle are obtained by dividing the fundamental component and its 90 degree phase-shift by the amplitude the fundamental component.

C. PLL – based Methods

The phase-locked loop (PLL) is a fundamental and conceptual tool that has been used in various disciplines of electrical technology [1], [3]-[7], 7[1], [10].The principal idea of phase locking is to generate signal whose phase angle is adaptively tracking variation of the phase angle of a given signal [5]. The conventional strategy for phase

locking is to estimate the difference between phase angle of the input signal and that of a generated output signal and drive this value to zero by means of a control loop. A block diagram of a single-phase PLL is shown in figure 3.

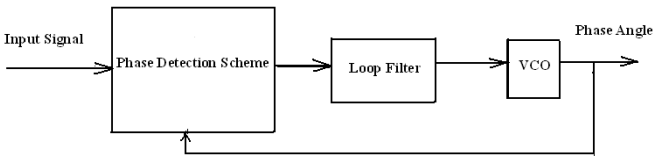

Figure 3: PLL Structure

The phase difference between the input and the output signals is measure using a phase detector (PD). The error signal is then passed through a loop filter (LF). The output of the filter drives a voltages-controlled oscillator (VCO) which generates the output signal. Several works mainly on the PD block have been done using PLL [1], [3]-[7]. An intuitive structure for the PD block is multiplier.

Figure 4 display the single phase power-based PLL (Ppll) where its PD is a single multiplier [14]. The PD dynamics rely entirely on the filter structure. The main issue that has hampered the utilization of the single phase PLL is that a single phase design normally generates second-order harmonic which has to be filtered out. At first sight the low pass filter (LPF) should have a low cutoff frequency which degrades system speed response. Thus a careful design of LPF and compensator must be performed in order to provide good dynamic response and disturbance rejection.

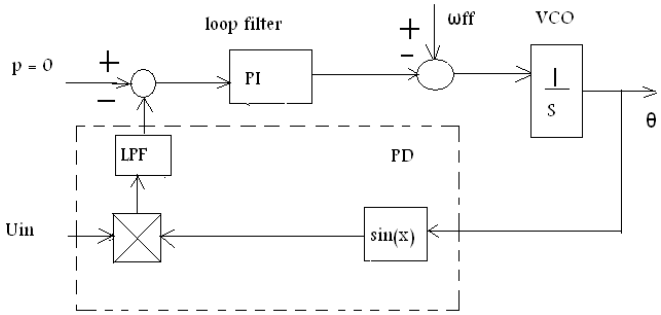

Figure 4: Single phase power PLL structure

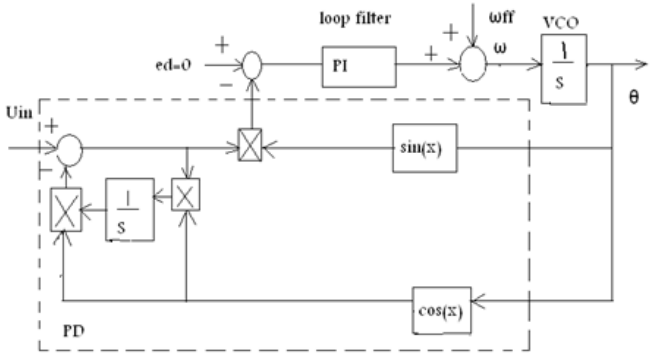

Figure 5: EPLL structure

In [14] an enhanced PLL (EPLL) is introduced that is shown in Figure5. The major advantage of EPLL system is its special PD mechanism. The conventional PD is replaced by a new mechanism that allows more flexibility and provides additional information such as the amplitude and the phase angle of the input signal. The governing equations of the EPLL are derived based on defining and minimizing an instantaneous cost function by means of the gradient-descent algorithm. Operation of the EPLL is based on estimating amplitude and phase angle of the fundamental component.

Another structure for the PLL so called the quadrature PLL (QPLL), is based on estimating in phase and quadrature-phase amplitudes of the fundamental component of the input signal [11]. The process of the phase detection in QPLL is somehow similar to the EPLL. Amplitude and phase angle are not directly estimate by QPLL. However they can simply be calculated from available output. Thus the QPLL is expected to have a superior performance over the conventional PLL particularly it is capable of following large and abrupt variation of the frequency [11].

A common structure for grid synchronization in three-phase systems is a phase locked loop implemented in the d-q synchronous reference frame as illustrated in Figure6. This structure uses an abc/dq coordinate transformation and the lock is realized by setting the U^*_d to zero. A regulator usually a PI regulator regulates the error to zero. The VCO integrates the grid frequency and outputs the utility voltage angle that is fed back into the α-β to d-q transformation module. This structure of PLL consists of two major parts, the transformation module and the PLL controller. The transformation module has no dynamics. In fact the PLL controller determines the system dynamics. Therefore the bandwidth of the loop filter determines the filter's filtering performance and its time response. As a consequence the loop filter parameters have a significant influence on the lock quality and the overall PLL dynamics.

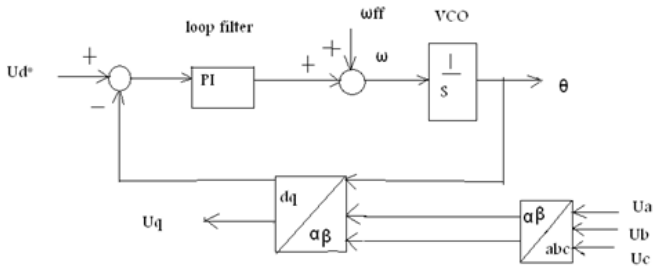

Figure 6: General structure of dq PLL method

The method in Figure6 is also called the synchronous reference frame PLL (SRF–PLL) [1], [3]. Under ideal utility conditions, i.e. balanced system with no distortion a loop filter of a wide band-width yields a fast and precise detection of the phase angle and the amplitude of the utility voltage vector. This method will not operate satisfactory if the utility voltage is unbalanced distorted by harmonics or frequency variations. Several works have been published based on the SRF-PLL of Figure6 to improve its performance [3], [14]-[16]. In general improved versions of the SRF-PLL use specific "filtering" techniques to deliver a non distorted signal to the conventional SRF-PLL structure. Synchronous reference frame PLL with positive sequence filter (PSF-PLL), synchronous reference frame PLL with sinusoidal signal

integrator (SSI-PLL) and double second order generalized integrator PLL(DSOGI-PLL) are among the newly developed solution to improve SRF-PLL performance[3]. These techniques employ sinusoidal signal integrator (SSI) as a positive sequence filter to improve system's robustness against the utility voltage distortions and unbalances.

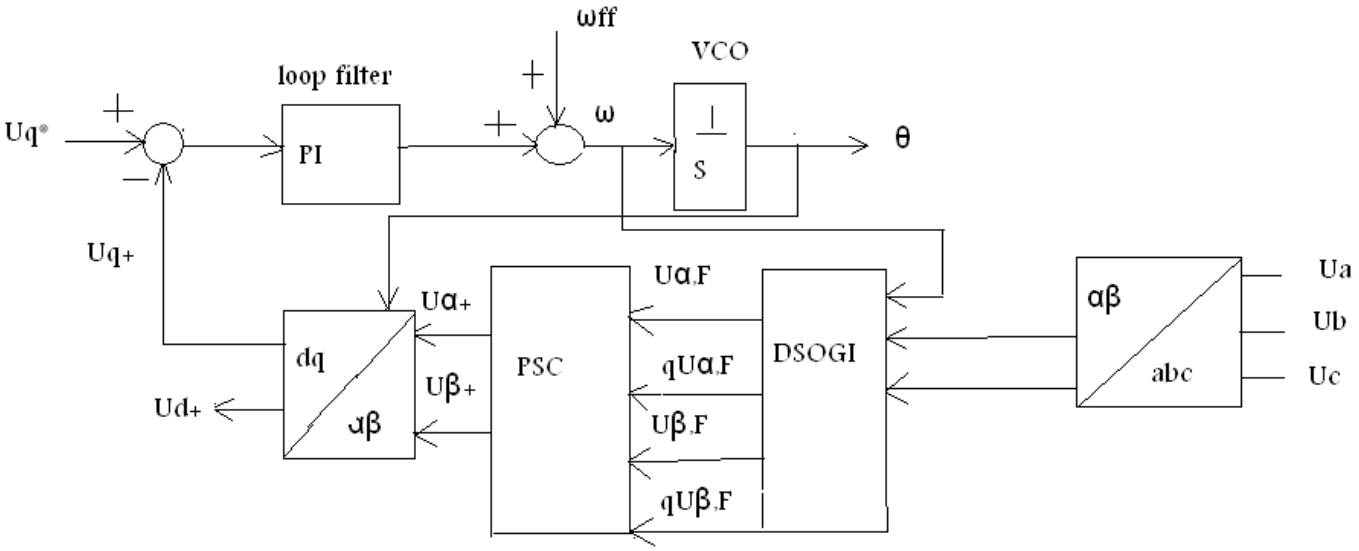

Figure 7: The structure of double second order generalized integrator PLL

In [15] notch filters are add to the SRF-PLL structure to remove the double frequency ripple caused by input unbalance. To handle unbalance situations a decoupled double synchronous reference frame PLL (DDSRF-PLL) was introduced in [3], [13]. In DDSRF-PLL an unbalanced voltage vector consisting of both positive and negative sequence components is expressed into a double synchronous reference frame to detect the positive sequence component. This system when combined with a proper decoupling procedure enables a fast and accurate phase angle and amplitude detection of the utility voltage positive sequence component under unbalanced utility conditions.

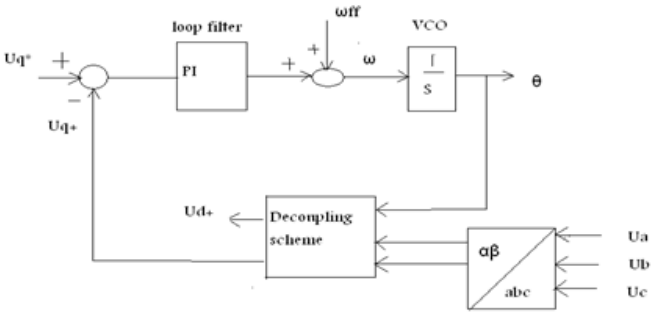

Figure 8: The Decoupled Double Synchronous Reference Frame-PLL (DDSRF-PLL)

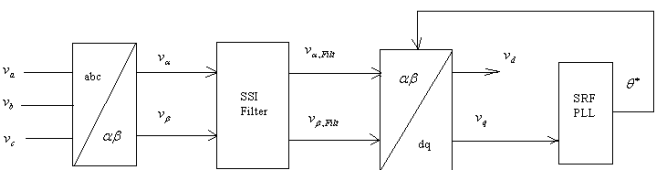

Figure 9: Positive Sequence Filter (PSF-PLL) Scheme

It uses digital resonant elements as sinusoidal signal integrators (SSI). The SSI was introduced in to improve the PLL characteristics. It is basically formed by an SSI filter and the SRF-PLL. The use of SSI filters allows delivering the fundamental positive sequence to the SRFPLL avoiding problems related to voltage distortions and imbalances. [3] Show that the performance of the method degrades when the input signal is distorted with harmonics. To attenuate the harmonics the PLL bandwidth can be reduced at the expense of increasing its time response. In general many grid-connected converters use a three-phase PLL configuration that measures a three-phase signal (voltages or currents) and derives a single phase-reference signal. The distinct phase-references for individual phases are obtained by adding or subtracting $2\pi/3$ radians to the measured phase angle. Such a three-phase design has the advantage of triple harmonic cancellation however in case of unsymmetrical transients the system is unable to correctly measures the phase angle of each individual phase. In fact such a PLL will give an average phase angle over three phases that poorly represents the individual phase angles [10].

Another technique employs all-pass 90° phase-shifters for each phase and uses in-phase and quadrature-phase waveforms for phase angle estimation [9]. The phase voltages and their 90° phase-shifted values can be used by the instantaneous symmetrical components (ISC) method to detect the positive-sequence voltages of the three-phase system [8].

D. Other Methods

Other techniques have also been introduced to perform grid synchronization. One of the simplest methods detects the zero crossing of the utility voltages [1]. However the zero crossing points occur only at every half cycle of the utility voltage thus the dynamic performance of this technique is quite low. In addition disturbances in the

input signal such as voltage sags and harmonics influence the accuracy of this technique.

The Extended Kalman Filter (EKF)-Based methods estimate the amplitude, frequency and phase angle vectors of the input voltage [6]. The EKF can estimate these vectors provided that the state-space model of the system sufficiently model actual variations of the state vectors. However it is not a trivial task to develop such adequate model that can follow vector variations due to mostly indeterminist changes in the utility voltages. In addition the EKF-based method is not able to cope with unbalanced input conditions.

Accuracy of the synchronization method based on the voltage zero crossing influenced by disturbances such as voltage sags and harmonics. Filtering techniques in different reference frames such as d-q or α-β encounter difficulties in detecting the phase angle when unexpected variations in the grid voltage occur due to the appearance of faults or disturbances in the utility network. Although the PLL-based algorithms can successfully reject harmonics, voltage sags, notches and other kind of disturbances. SRF-PLL topology is presented is simple but is sensitive to voltage distortions/unbalances. For this reason, improved versions of SRF-PLL are presented with the objective of overcome these improved versions uses specific "filtering" techniques in order to deliver a non distorted signal to the SRF-PLL. Some of these techniques employ sinusoidal signal integrators to get robustness against utility voltage distortions and imbalances. [3], [13] give analysis and comparison of PLL techniques. The study reveal that the combined filter approach using a DSOGI pre-filter and a SOLC extended loop-filter seems to be the best choice in terms of the achievable dynamics and the disturbance rejection performance in comparison to the other presented PLL methods[13]. While [3] stated that The DSOGI-PLL presents a good performance under tested conditions. This topology uses one more resonant filter related to SSI-PLL and is not able to detect the angle in single phase systems. The strong points of this PLL technique are the capacity of calculate precisely the amplitude of fundamental voltage and the structural simplicity. Instead of it authors present the DSRF-PLL as an optimal solution for utility grids with unbalanced voltages.

3. Simulation and Results

C. Synchronization Analysis

Figure10 shows a schematic diagram of synchronization techniques used in this work. We extract the magnitude and phase angle from the utility by means of meter and PLL then calculate the modulation index. SVPWM received modulation index m^* and reference angle θ^* and send switching signal to VSI. We can control magnitude, frequency and phase angle of output of inverter voltage by controlling the modulation index, phase angle and frequency of the input signal. For this synchronization method we used the PLL to extract the reference phase angle. The inverter is connected to the grid and star-connected RL local load. The resistance of load is 253 Ω and the load inductance of the load is 70 mH.

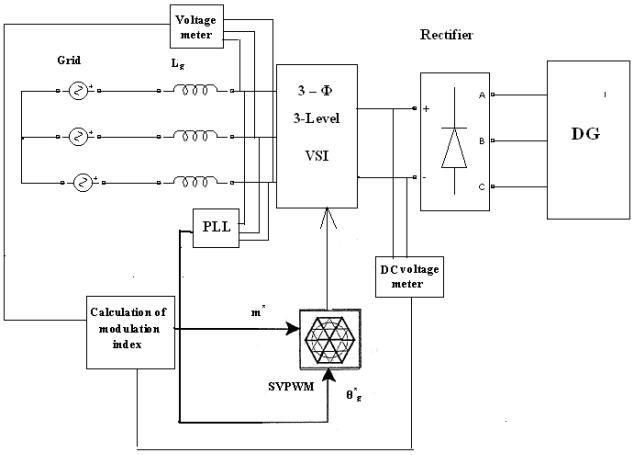

Figure 10: Block diagram of grid synchronization

D. Space Vector PWM for a 3-level Inevter

Multilevel inverters are being increasingly used in high power medium voltage applications due to their compatibility for medium voltage and improved output performance at that voltage as compared to two-level inverters. Among various modulation techniques for a multilevel inverter Space Vector PWM (SVPWM) is an attractive candidate technique. The basic idea of space vector modulation is to compensate the required volt-seconds using discrete switching state and their on-times produced by an inverter. An important parameter associated with modulation is modulation index m_i. It is defined as $u_1/u_{1six-step}$, where u_1 is the fundamental voltage generated by the modulator and $u_{1six-step} = (2/\pi)V_{dc}$ is the fundamental voltage at six-step.

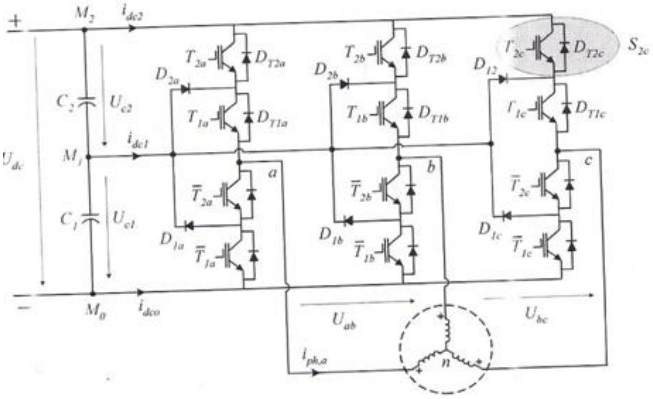

Figure 11: Three-level neutral point clamped inverter topology

The main modulation task is to achieve control of the system by switching converter power components i.e. determining which discrete vectors should be applied and for how long within a switching period. A typical modulation provides average voltage value equal to the voltage reference thus making a direct dc-ac conversion.

In order to produce three levels, the switches are controlled so that only two of the four switches in each phase leg are turned on at any time. In summary each

phase node (a, b, or c) can be connected to any node in the capacitor bank (M0, M1, and M2). Thus the number of different converter switch states calculates to

$$n_{sw} = N^{ph} = 3^3 = 27 \quad (1)$$

The operation of each switching inverter leg can be represented by three switching states P (1), O (0) and N (-1).

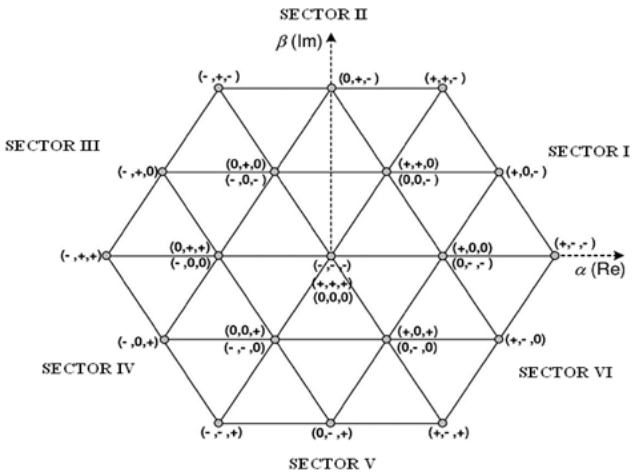

Figure 12: Space vector diagram of a 3-level inverter

In our work we did the same technique as in [18]

4. Results and Discussion

A. Steady State

The angle and speed of rotation are obtained precisely from the PLL simple Controller shown in Figure 13. PLL use a simple error detection from a negative feedback loop and then use filters and PI controllers in order to achieve close tracking of the demanded angles.

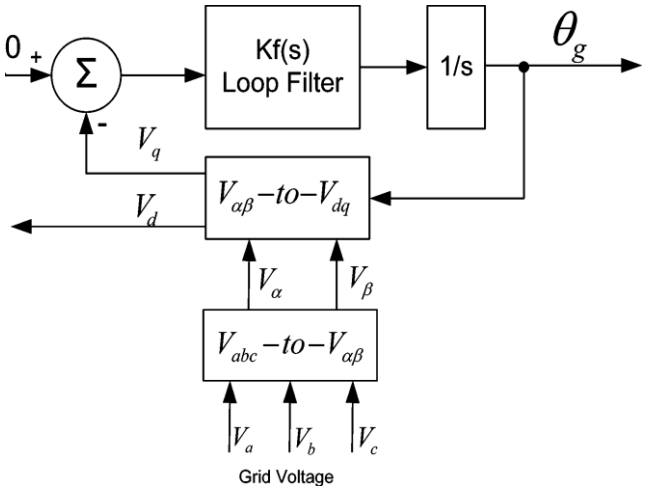

Figure 13: Three-Phase PLL Algorithm

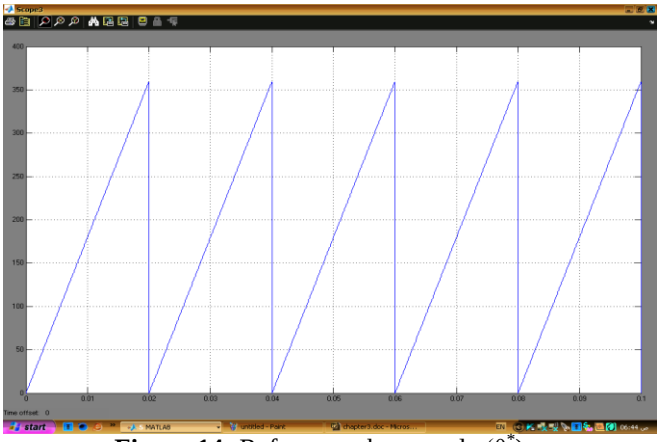

Figure 14: Reference phase angle (θ^*)

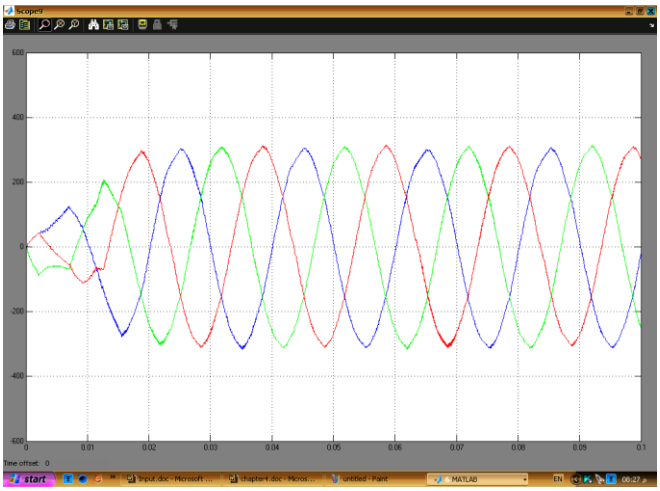

Figure 15: Output voltage of the inverter

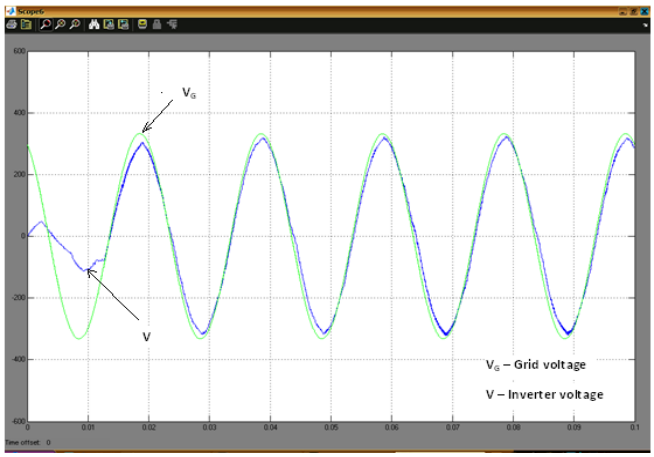

Figure 16: Output voltage of inverter and the grid voltage when the frequency and phase angle is f_g = 50 Hz , θ_g = 0

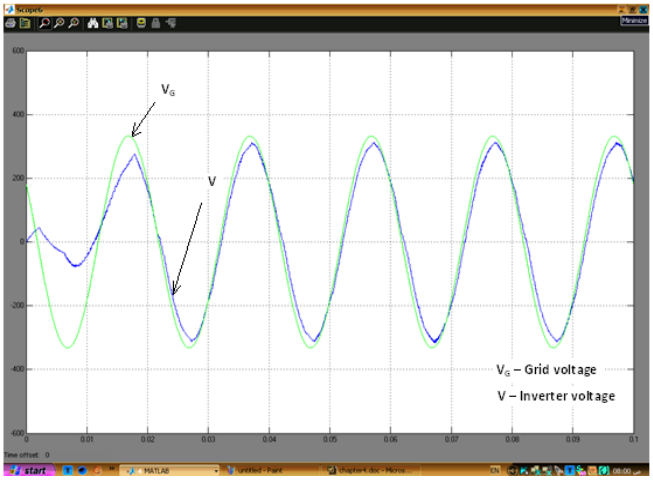

Figure 17: Output voltage of inverter and the grid voltage when the frequency and phase angle is f_g = 50 Hz , θ_g = $\frac{\pi}{6}$

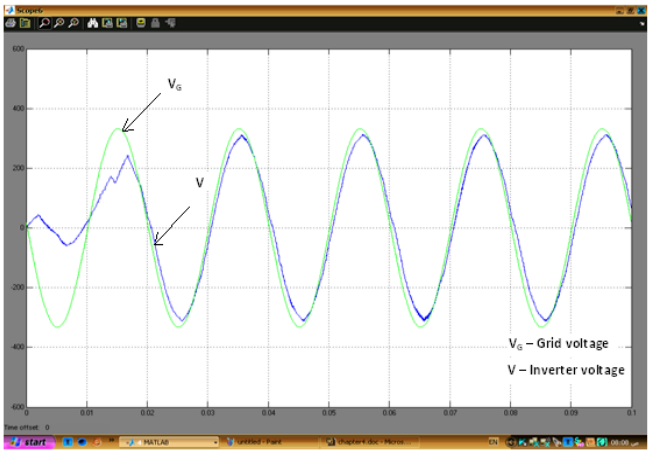

Figure 18: Output voltage of inverter and the grid voltage when the frequency and phase angle is f_g = 50 Hz , θ_g = $\frac{\pi}{3}$

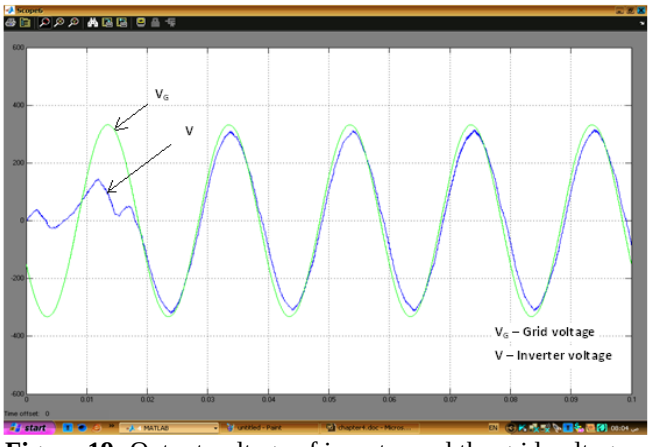

Figure 19: Output voltage of inverter and the grid voltage when the frequency and phase angle is f_g = 50 Hz , θ_g = $\frac{\pi}{2}$

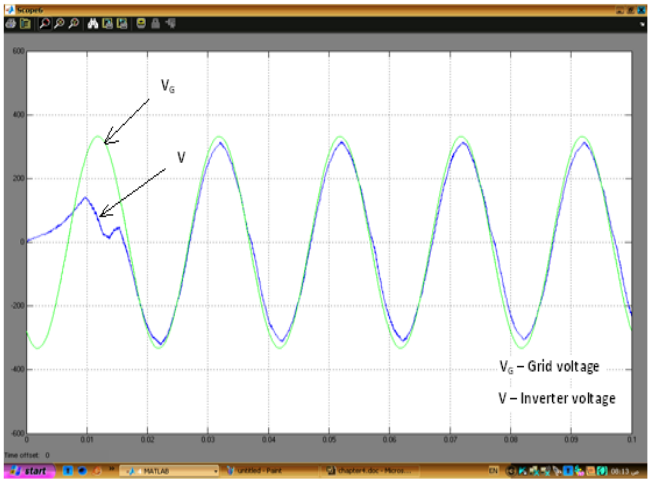

Figure 20: Output voltage of inverter and the grid voltage when the frequency and phase angle is f_g = 50 Hz , θ_g = $\frac{2\pi}{3}$

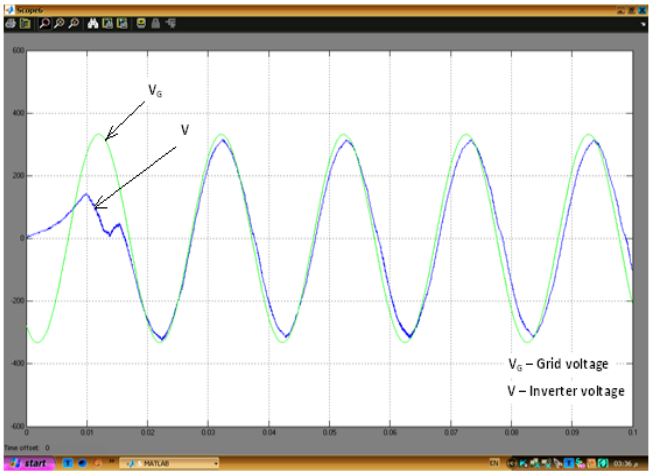

Figure 21: Output voltage of inverter and the grid voltage when the frequency and phase angle is f_g = 49.5 Hz , θ_g = $\frac{2\pi}{3}$

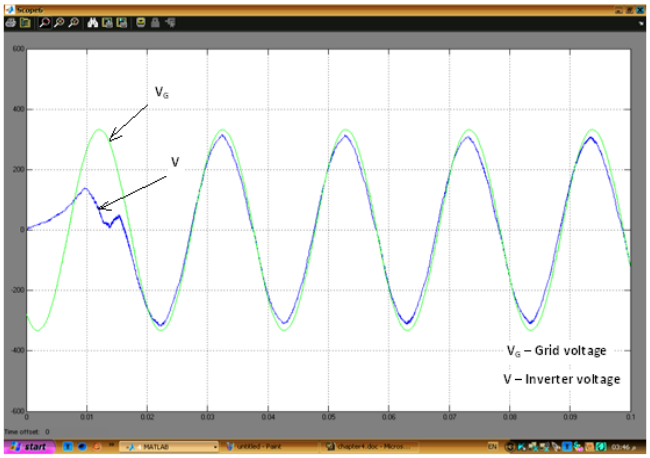

Figure 22: Output voltage of inverter and the grid voltage when the frequency and phase angle is f_g = 49 Hz , θ_g = $\frac{2\pi}{3}$

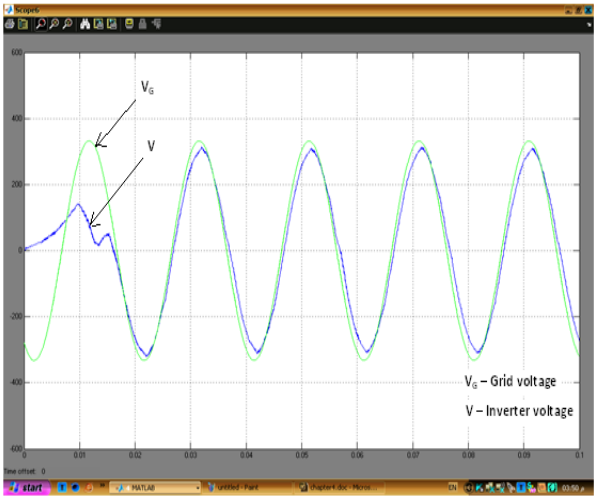

Figure 23: Output voltage of inverter and the grid voltage when the frequency and phase angle is f_g = 50.5 Hz , θ_g = $\frac{2\pi}{3}$

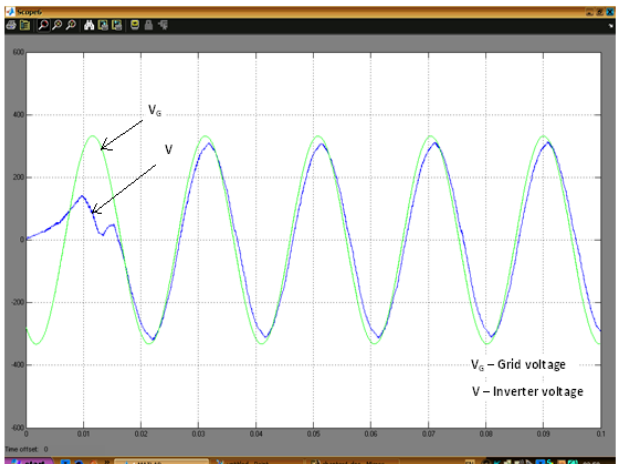

Figure 24: Output voltage of inverter and the grid voltage when the frequency and phase angle is f_g = 51 Hz , θ_g = $\frac{2\pi}{3}$

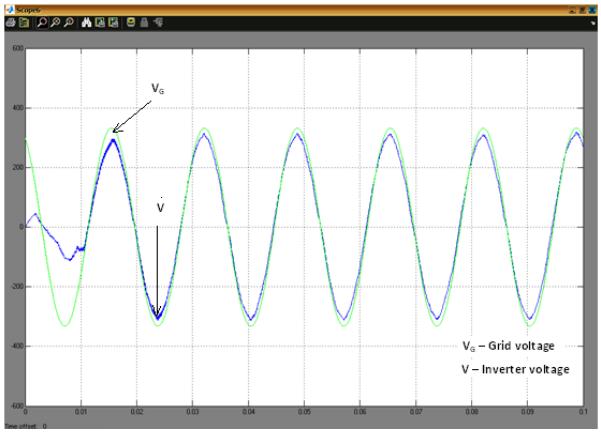

Figure 25: Output voltage of inverter and the grid voltage when the frequency and phase angle is f_g = 60 Hz , θ_g = $\frac{2\pi}{3}$

Figure14 give the output of PLL namely the reference phase angle. Figure15 represent the output voltage of the inverter. Figure16 shows output line voltage of inverter and the grid voltage when we put the frequency of the grid f_g = 50 Hz and phase angle of the grid θ_g = 0 as the reference to inverter. The result is almost identical output voltage of the inverter. Figure17 to Figure20 change the phase of the grid with θ_g = $\pi/6$, $\pi/3$, $\pi/2$ and $2\pi/3$ respectively and the results is the same. In Figure21 to Figure25 we put the phase angle of the grid θ_g = $2\pi/3$ and varies the grid frequency f_g = 49.5, 49, 50.5, 51 and 60 Hz. And the result is also the same. This means that this inverter can easy be connected and synchronized to the grid with help of phase angle and modulation index. From the figures we see that the waves is pure sinusoidal. This scheme easy tracked the system frequency, phase and voltage amplitude. It is very simple and accuracy.

B. Transient Response

The grid frequency used in all above tests was fixed frequency. In practice the frequency of the grid supply fluctuates slightly about the specified standard. If the synchronization process is not precise, the connection of the inverter to the grid would immediately produce serious damage to the system. In order to test the reliability of the scheme and its ability to withstand grave swings of the grid frequency, a programmable 3-phase voltage source was used in place of the fixed frequency power source used in the other tests. The programmable voltage source was set to a 415 V line to line voltage, with a phase voltage of 240 V and an initial frequency of 50 Hz. The frequency of power source is then by a step from 50 Hz to 55 Hz. If the scheme is unable to track this sudden change, synchronization would be lost, and the inverter will have to be disconnected from the grid line.

The transient response of the inverter terminal voltage (after the filter) and phase current which subjected to a step change of frequency is shown in Figure 26. It is seen that the output voltage of the inverter stays reasonably constant. If the voltage across the filter is subtracted as vector, then the voltage at the terminals of the inverter (before the filter) is also constant having the same frequency as the grid supply. This proves that the scheme is working quite satisfactorily in harmony with the PLL in order to keep the inverter perfectly synchronized with the grid supply during the transient and steady state periods subsequent to the step changes in grid frequency and inverter currents. It is also noticed that there is a small increase in the magnitude of the line to ground phase voltage. This small increase is necessary in order to produce the step increase in current.

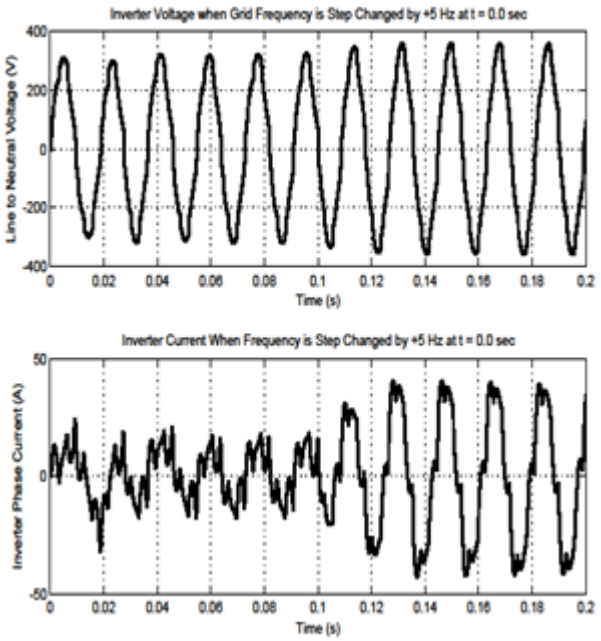

Figure 26: Transient response of Output Voltage and phase current for step change in frequency and Reference Currents

5. Conclusion

It is noticed that the performance of the scheme is outstanding, and synchronization was maintained precise, allowing the inverter to continue tracking the phase angle even when the frequency changed by the large step of 5 Hz. This means that this inverter can easy be connected and synchronized to the grid with help of phase angle and modulation index. This scheme easy tracked the system frequency, phase and voltage amplitude. It is very simple and accuracy

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