International Journal of Science and Research (IJSR)
ISSN (Online): 2319-7064
Index Copernicus Value (2013): 6.14 | Impact Factor (2013): 4.438

Convolutional Encoder

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Abstract: ***Data transmission over wireless channels is affected by attenuation, distortion, interference and noise that affect the receiver's ability to receive correct information. Convolution codes are used in many communication systems due to their excellent error-control performance. This paper presents the convolution encoder of constraint length 9 and code rate 1/3.***

Keywords: Convolution encoder, Data transmission, Constraint length, code rate, VHDL

1. Introduction

1.1 Convolutional Encoder

Convolutional code is a type of error-correcting code in which each (n≥m) m-bit information symbol (each m bit string) to be encoded is transformed in to an n-bit symbol, where m/n is the code rate (n≥m) and the transformation is a function of the last k information symbols, where K is the constraint length of the code. A Convolution Encoder accepts an input stream of message and generates encoded output streams to be transmitted. In this process for one input bit the encoder generates more than one output bits and these redundant symbols in output bit pattern makes the transmitted data more immune to the noise in the channel. The redundant bits help to decide and correct the errors in received pattern. For the standardization a terminology was generated as summarized:M: Length of the shift registers stage in the encoder Constraint Length (K) = M+1: This number represents the number of input bits required to generate a unique output pattern in the encoder. A constraint length of K=3 means that each output symbol depends on the current input symbol and the two previous input symbols.

Number of States = 2(K-1) : Defines the maximum number of states that is possible to be mapped by the combinations of the K number of input bits for the convolution encoder.
L: Length of Input Message.
R: Convolution Code Rate
R=Number of input bits to create a symbol at the output (m)/ Number of output bits in a symbol at the output (n).For example, 1/2 code rate means each bit entering the encoder results in 2 bits leaving the encoder. The encoder has n modulo-2 adders, and n generator polynomials one for each adder. This process doubles the number of input bits at the output. For example, a 4-bit input is converted into an 8-bit output, 8-bit input into a 16-bit output and so on.

The block diagram of convolution encoder is shown in Fig 1. To generate the output, the encoder uses three values of the input signal, one present and two past. The set of past values of input data is called a state. The number of input data values used to generate the code is called the constraint length.

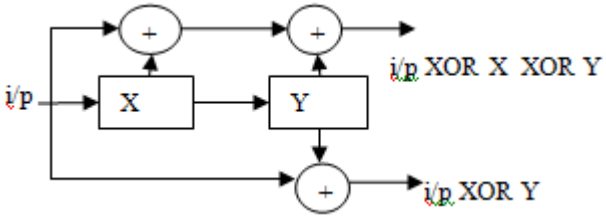

Figure 1: Block Diagram of Convolution Encoder

Each set of outputs is generated by EX-OR ing a pattern of current and shifted values of input data. The pattern used to generate the coded output value can be expressed as binary strings called "Generator Polynomials" (GP). The MSB of the GP corresponds to the input; the LSBs of the GP correspond to the state. The encoder that has been designed is a linear, non – systematic, convolution encoder.

A Viterbi decoder uses the Viterbi algorithm for decoding a bit stream that has been encoded using Forward error correction based on a Convolutional code. The Viterbi decoding algorithm was proposed and analyzed by Viterbi in 1967. It is widely used as a decoding technique for convolution codes as well as the bit detection method in storage devices. Viterbi decoders currently find their use in more than one billion cell phones. The algorithm works by forming trellis structure, which is eventually traced back for decoding the received information. Convolutional encoding with Viterbi decoding is a powerful method for forward error correction. The Viterbi algorithm essentially performs maximum likelihood decoding. However, it reduces the computational complexity by using trellis structure.

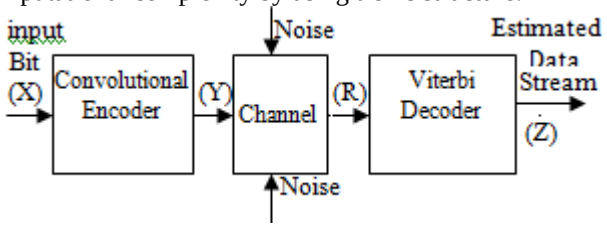

Figure2: Block Diagram of Convolution Encoder

Figure2 shows the convolutional encoder and Viterbi decoder, which is used in the digital communication system. Here, X is the input data steam, which is given into the

convolutional encoder and it produces the encoded data stream (Y). The encoded data stream (Y) is given to the channel in the presence of noise. Hence, it produces the noise added encoded data stream (R). Finally, data stream (R) is given to the Viterbi decoder that produces the estimated data stream (Z) applied at the input.

2. Literature Survey

Previous paper describe the analysis and implementations of a pipelined & reduced-complexity decode approach, the adaptive Viterbi algorithm (AVA). AVA design is implemented in reconfigurable hardware to take full advantage of algorithm parallelism and specialization. Run-time dynamic reconfiguration is used in response to changing channel noise conditions to achieve improved decoder performance. Look ahead technique is studied for extracting vectorized output bits without taking into consideration the hardware cost involved. It improves the throughput rate. Implementation parameters for the decoder have been determined through simulation and the decoder has been implemented on a Xilinx FPGA SPARTAN 3E Kit. This approach has shown significant speedup versus both software implementations on previous FPGA-based implementations. Through experimentation it was shown that dynamic reconfiguration can be used effectively to improve overall performance by at least 20%. Reconfiguration was performed on the basis of channel noise to achieve a consistent bit-error rate. If channel noise increases, a more accurate but slower running decoder is swapped into the FPGA hardware. Reduced channel noise leads to the opposite effect. With a throughput of 20 Mbps, the proposed decoder is suitable for use in receiver architecture of 3G cellular code division multiple access environments.[5]

Wireless devices such as hand phones and broadband modems rely heavily on forward error correction techniques for their proper functioning, thus sending and receiving information with minimal or no error, while utilizing the available bandwidth. Major requirements for modern digital wireless communication systems include high throughput, low power consumption and physical size. This paper presents the design of an efficient coding technique for wireless communication, using FPGA, a four state convolutional encoder and decoder were designed respectively, an efficient decoder with high speed and low power consumption was designed using the memory less decoder design, the maximum frequency of the device clock was recorded as 185 MHz, with a coding gain of 4dB over uncoded BPSK for BER of 10-10 found through MATLAB simulation. The encoder and decoder were implemented on altera DE1 board, with cyclone II FPGA having a maximum frequency of 50MHz.[6]

In this paper, Author presents a Spartan XC3S400A Field-Programmable Gate Array efficient implementation of Viterbi Decoder with a constraint length of 3 and a code rate of 1/3. The Viterbi Decoder is compatible with many common standards, such as DVB, 3GPP2, 3GPP LTE, IEEE 802.16, Hiperlan, and ntelsat IESS-308/309. The proposed solution has proven to be particularly efficient in terms of the required FPGA implementation resources so as Chip Silicon Area, Decoding Time and Power Consumption. We have developed Viterbi Decoder on Spartan 3A FPGA by utilizing both method and Synthesis result shows that Trace back method is more efficient in term of Chip Area Utilization so as will be Power Consumption in comparison with Register Exchanged Method. Also this paper tested the functionality of the Viterbi Decoder Code implemented on FPGA by designing a Test Bench for performing Error Detection and Correction[4]

In a previous paper, A Viterbi decoder uses the Viterbi algorithm for decoding a bit stream that has been encoded using Forward error correction based on a Convolutional code. The maximum likelihood detection of a digital stream is possible by Viterbi algorithm. Author presents a design and implementation of Convolutional encoder and Viterbi decoder with a constraint length of 7 and code rate of 1/2. This is realized using Verilog HDL. It is simulated and synthesized using Modelsim PE 10.0e and Xilinx 12.4i. [1]

The problem of survival memory management of a Viterbi decoder (VD) was solved by introducing a novel pointer implementation for the register exchange method, where a pointer is assigned to each row of memory in the survivor memory unit (SMU). The content of the pointer which points to one row of memory is altered to point to another row of memory, instead of copying the contents of the first row to the second. In this paper, the one-pointer VD is proposed; if the initial state of the convolutional encoder is known, the entire SMU is reduced to only one row. Because the decoded data bits are generated in the required order, even this row of memory is dispensable. The PVD proposed was further improved to reduce its power consumption. The MLVD is a memoryless implementation of the VA, and successfully decodes the continuous data encoded by a WCDMA convolutional encoder. The power reduction is as high as 50% and the latency is only 2 data bits. The new implementation is realized by applying the pointer concept to the RE implementation, and by using trellis truncation for every bits encoded. The BER for the MLVD is estimated to be for a SNR of 4.2 dB with a coding gain of 2.6 dB. The MLVD along with an on-chip convolutional encoder was implemented on a Xilinx 2V6000 chip to demonstrate both the design's functionality and feasible implementation. The hardware and computational overhead of this implementation is only a 256-to-1 decoder, which is switching at the data rate frequency. Increasing the MLVDs performance by increasing the constraint length or by varying the survivor path length is still to be investigated. Thus, the one-pointer architecture, referred to as memoryless VD (MLVD), reduces the power consumption of a traditional traceback VD by approximately 50%, but has some performance degradation. A prototype of the MLVD with a one third convolutional code rate and a constraint length of nine is mapped into a Xilinx 2V6000 chip, operating at 25 MHz with a decoding throughput of more than 3 Mbps and a latency of two data bits.[2]

This paper presents a design and implementation of small Viterbi decoder architecture. Its specifications are coding rates 1/2 and 1/3, with generator polynomial (561, 753)8 and (557, 663, 711) 8 respectively. Both cases are designed with

the constraint length of 9 (256 states). In addition, they comply with 3GPP (3rd Generation Partnership Project) standard. In this work, the serial architecture with four add-compare-select (ACS) combined with the modified register exchange method are proposed. The prototype has been successfully implemented on Xilinx Vertex II FPGA device. As a result, it obtains small resource of FPGA (slices and block RAM). Furthermore, its data rate exceeds 2 Mbps which is suitable for 3G (W-CDMA) mobile system. It also can be applied for other related communication systems. In this paper, a small architecture of viterbi decoder for 3GPP mobile communication system is presented. Four ACS combined with the modified register exchange has been proposed in order to achieve small implemented area. The results show that this design got higher speed than that of 3GPP specification and having less number of slices and block RAM as the outcome.[10]

3. Design Methodology

Convolution code are commonly specified by three parameters k, n, m or L where k is the number of input, n is the number of output , m=L-1 which represent number of shift register and L represent length of convolutional Encoder. The efficiency of convolution code is measured in terms of code rate, which is calculated as k/n.

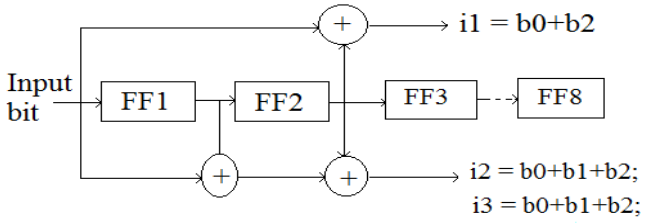

Figure3. : Convolutional Encoder of L= 8 & k/n =1/3

In this diagram at the first clock cycle input bit is enter to flip-flop register 1 ie at FF1 and then it is shifted to next shift register say FF2 and so on. The output is the X-OR combination of input and shift register bit depend on Generator Polynomials . The developed convolutional Encoder's outputs are depends on following equations.

i1 = b0+b2;

i2 = b0+b1+b2;

I3 = b0+b1+b2;

In this dissertation, the convolutinal Encoder is of constraint length(K) 9 and code rate (r) 1/3.

3.1 Simulation Result

The Simulation Waveform and data flow diagram of Convolutional Encoder is shown in Fig.4 . the convolutional Encoder is simulated in modelsim.

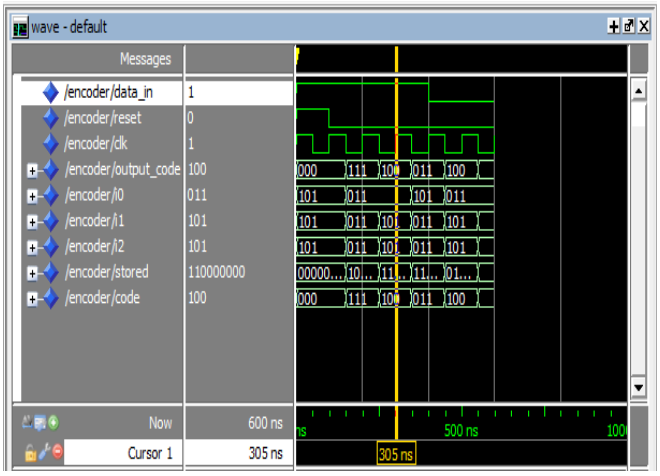

Figure 4: Output waveform for convolutional Encoder

Input Bit : X = {01101}

Encoded Bit : Y={10110110101101101101110110110101110110110110101}

Shift register: S={101100000}

4. Conclusion

By over viewing the paper, it can be analyzed that Convolutional encoding with Viterbi decoding is a powerful method for forward error detection and correction. It has been widely deployed in many wireless communication systems to improve the limited capacity of the communication channels. This design has been simulated in MODELSIM 6.3f for the constraint length of K=9 and code rate of 1/3 input sequence.

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