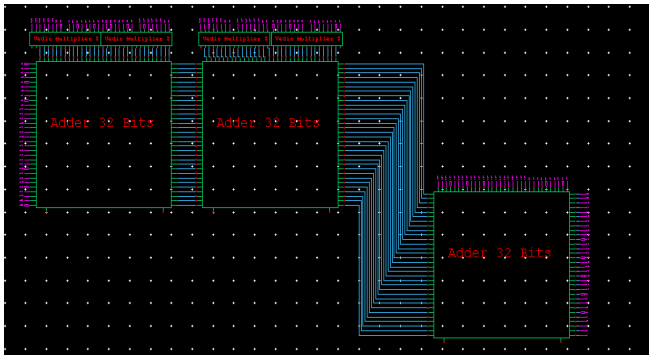

Figure 15: Schematic of 16-bit Multiplier

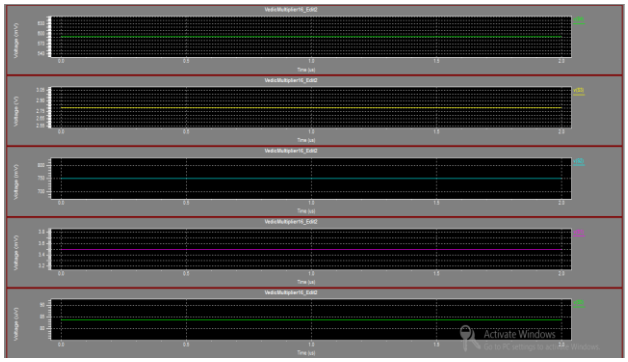

Figure 16: Output of 16-bit Multiplier in 180nm Technology

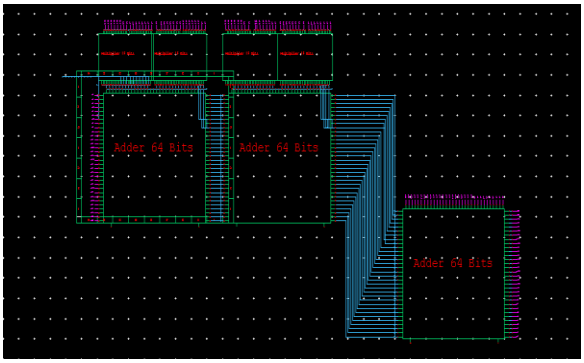

Figure 17: Schematic of 32-bit Multiplier

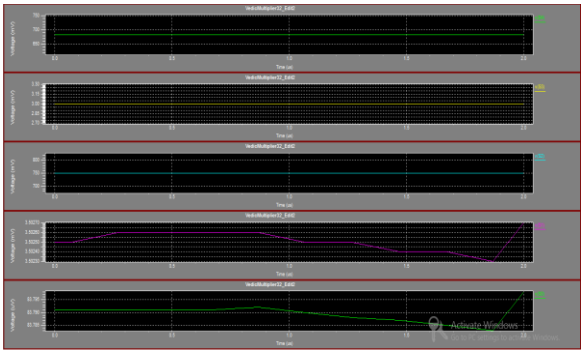

Figure 18: Output of 32-bit Multiplier in 180nm Technology

The output of 4-bit multiplier, 8-bit multiplier , 16-bit multiplier , 32-bit multiplier on 180nm technology is shown in above fig and its parameter on 180nm technology is shown in table below.

Multiplier	*Technology*	*Parameter*	
		No. of gates	*Power*
4-bit multiplier	180nm	240	2.6689×10^{-3}
8-bit multiplier	180nm	1638	1.6733×10^{-3}
16-bit multiplier	180nm	3276	5.0198×10^{-3}
32-bit multiplier	180nm	6552	2.1836×10^{-2}

3. Conclusion

In the present paper we generated a full adder using this full adder we generate 4-bit, 8-bit,16-bit & 32 -bit adder. We use these adder and generated the 4-bit , 8-bit, 16-bit & 32-bit multiplier . Also all the multipliers are generated using a Ancient Indian Vedic Mathematics technique.And we will see the result of adder & multipliers on 180nm technology.In that no. of gates are continuously increasing according to that power level change but when we apply same input then power increases. In the proposed work we can used the concept of pipelining to improve the generated result.

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