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A Hierarchical Design of 32-bit Vedic Multiplier

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Abstract: ***Many processors devote a considerable amount of processing time in performing arithmetic operations particularly multiplication operations therefore high-speed multiplier is much desired. There are various methods of multiplication in Vedic mathematics, Urdhva tiryagbhyam, being a general multiplication formula is equally applicable to all cases of multiplication. This is more efficient in the multiplication of large numbers with respect to speed and area. In that we will see the different types of multiplier that will be generated using a Vedic Mathematics. In that we will proposed a 4-bit binary multiplier using this sutra. A new 4-bit adder is proposed which when used in multiplier, . Also we proposed 8-bit adder, 16 bit adder & 32 bit adder using this adder we proposed an 8-bit multiplier, 16 bit multiplier & 32 bit multiplier using a Vedic Mathematics (Urdhva Tiryagbhyam sutra) for generating the partial products. Also this paper proposed the design of high speed Vedic Multiplier using the techniques of Ancient Indian Vedic Mathematics.***

Keywords: VLSI, Urdhva Tiryagbhyam sutra, Adder, Multiplier.

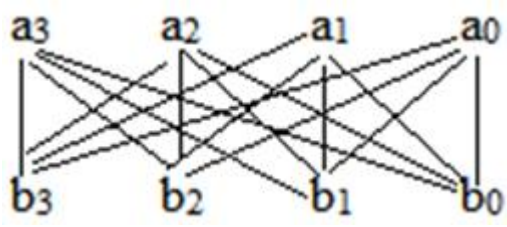
1. Introduction

Multipliers are essential in implementation of systems realizing many important functions such as fast fourier transforms and multiply accumulate. Multiplier is one of the key hardware blocks in designing arithmetic operation, signal and image processors. Many transform algorithms like the basic building blocks in Fast Fourier transforms, DCT, DFT etc., make use of multipliers. High performance multipliers using Vedic mathematics are proposed and conclude that it is suitable for high-speed complex arithmetic circuits.

The basic idea behind all these attempts was the fast implementation of the multiplier and addition of the partial products . With advances in technology, many researchers have tried to design multipliers using Vedic sutras , which offer high speed , low power consumption , and regularity of layout and less area or even combination of them in multiplier Multiplier is time-consuming operations in many of the digital signal processing applications and computation can be reduced using the Vedic sutras and the overall processor performance can be improved for many applications. Therefore, the goal is to create hybrid architectures that is comparable in speed, area and power, but requires less area than a design using a standard multiplier. The motivation behind this work is to explore the Design and implementation of hybrid multiplier architecture. The proposed pipelined Vedic-Array multiplier is based on the Vedic Sutras.

1.1 Vedic Mathematics

An illustration of Urdhva Tiryagbhyam sutra is shown in Figure 1



The 4x4 multiplication has been done in a single line in Urdhva Tiryagbhyam sutra [1], whereas in shift and add(conventional) method, four partial products have to be added to get the result. Thus, by using Urdhva Tiryagbhyam Sutra in binary multiplication, the number of steps required calculating the final product will be reduced and hence there is a reduction in computational time and increase in speed of the multiplier. Now we will see the multiplication of two decimal numbers using the Urdhva Tiryagbhyam sutra which is shown in fig no.2

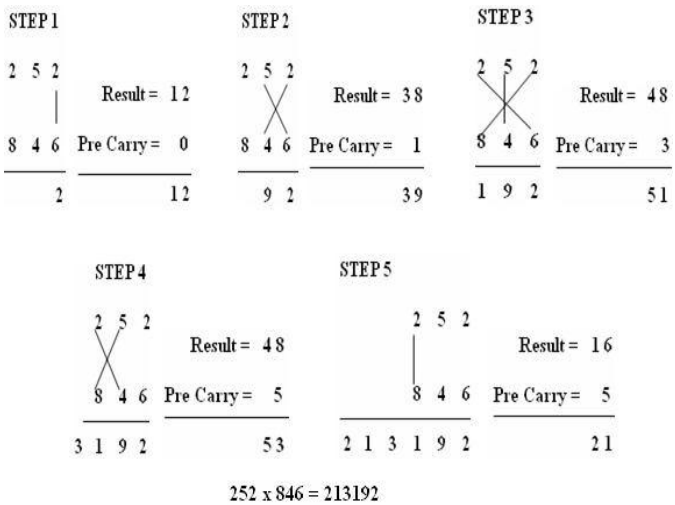


Figure 2: Multiplication of two decimal numbers – 252 x 846

2. Implemented Work

ADDER:- Addition is the most common and often used arithmetic operation on microprocessor, digital signal processor, especially digital computers. In electronics, an adder is digital circuit which is used to perform the addition of binary digits. In vlsi system design using adders we are increasing the performance of the module.[1].Schematic of adder is shown in fig.1 & its output waveform shown in fig.2

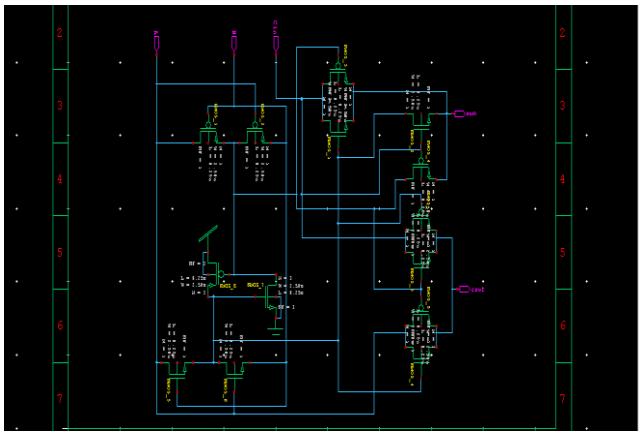


Figure1: Schematic of Adder

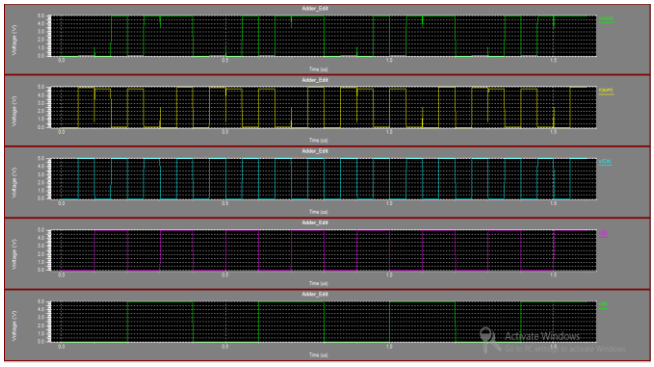


Figure 2: Output of adder in 180nm technology

Full Adder: This type of adder is implemented with the help of half-adder.Full-adder has three inputs and two outputs. The first two inputs are A and B and the third input is an input carry designated as CIN.The output carry is designated as COUT and the normal output is designated as S. We can see that the output S is an EXOR between the input A and the half-adder SUM output with B and CIN inputs. COUT will be an OR function.

Using the full adder we can generate 4-bit adder using this 4-bit adder we can generate 8-bit add again we are using 4-bit adder to generate 16-bit adder and using 16-bit adder we generate 32-bit adder which is shown in fig 3,5,7 & fig 9. & its output waveform shown in fig.4,6,8 & fig.10

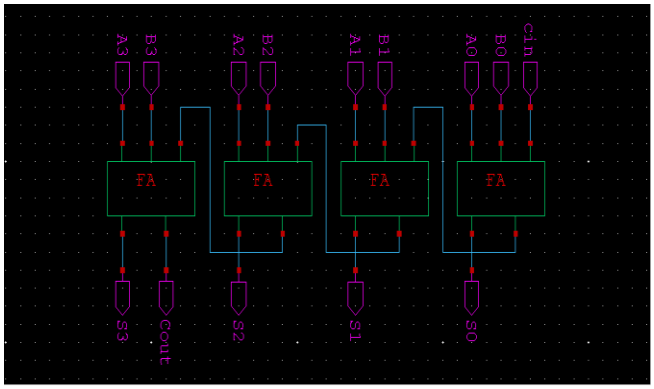


Figure 3: Schematic of 4-bit adder

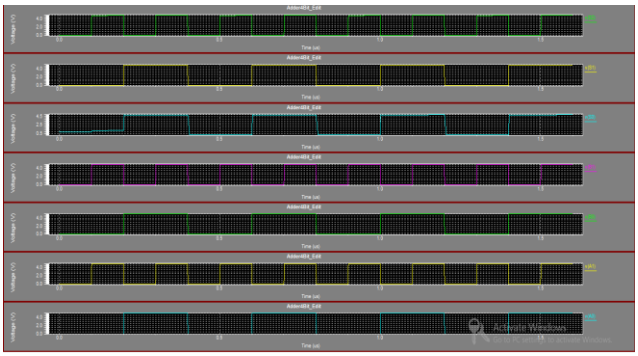


Figure 4: Output of 4-bit adder in 180nm technology

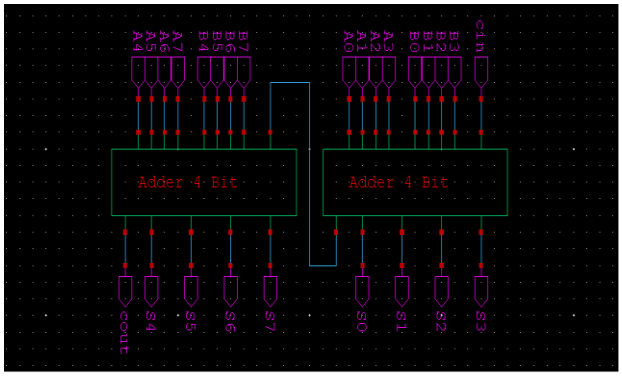


Figure 5: Schematic of 8-bit adder

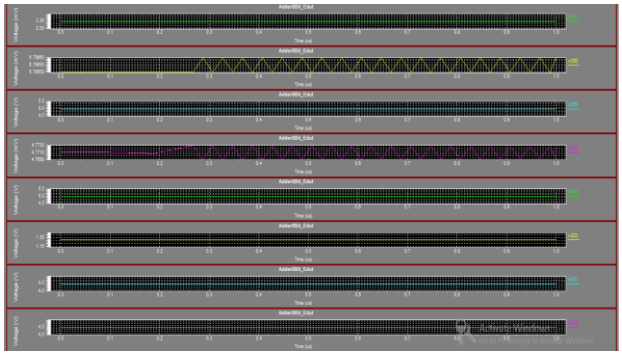


Figure 6: Output of 8-bit adder in 180nm technology

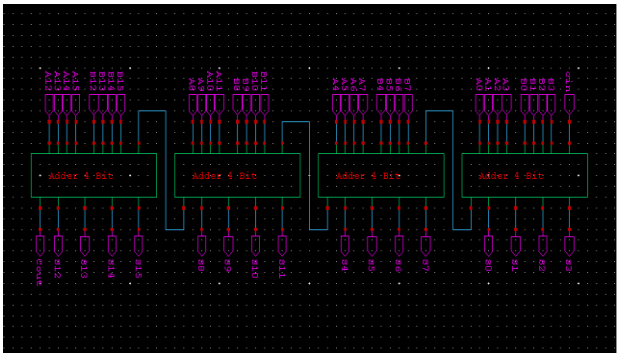


Figure 7: Schematic of 16-bit adder

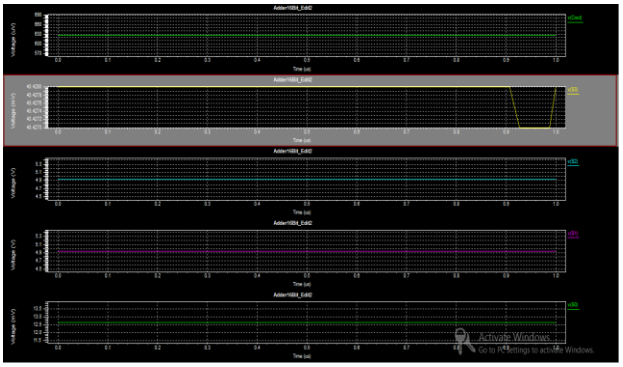


Figure 8: Output of 16-bit adder in 180nm technology

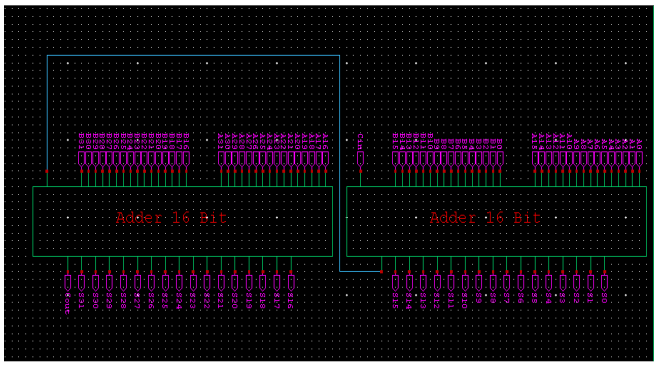


Figure 9: Schematic of 32-bit adder

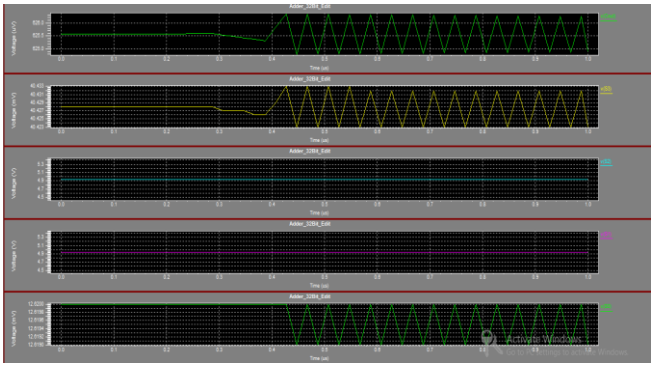


Figure 10: Output of 32-bit adder in 180nm technology

The output of Full adder, 4-bit adder, 8-bit adder,16-bit adder & 32-bit adder on 180nm technology is shown in above fig and its parameter on 180nm technology is shown in table below.

Type of adder	*Technology*	*Parameter*	
		No. of gates	*Power*
Full adder	180nm	14	8.7704×10^{-5}
4-bit Adder	180nm	56	5.0427×10^{-4}
8-bit Adder	180nm	112	2.9435×10^{-6}
16-bit Adder	180nm	224	3.4530×10^{-4}
32-bit Adder	180nm	448	1.4821×10^{-3}

When we used the concept of adder we generate the 4-bit multiplier, 8-bit multiplier, 16-bit multiplier , 32-bit multiplier which is shown in fig and fig 11,13,15,17. & its output waveform shown in fig.12,14,16 & fig.18.

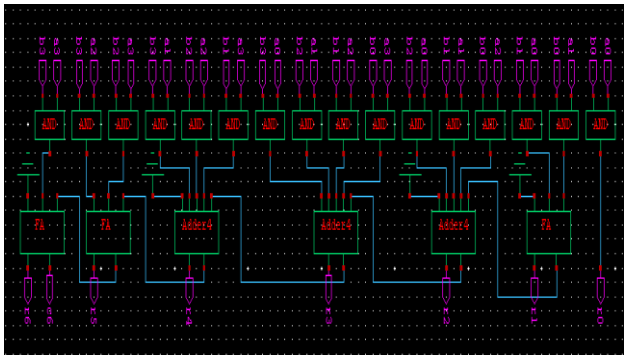


Figure 11: Schematic of 4-bit Multiplier

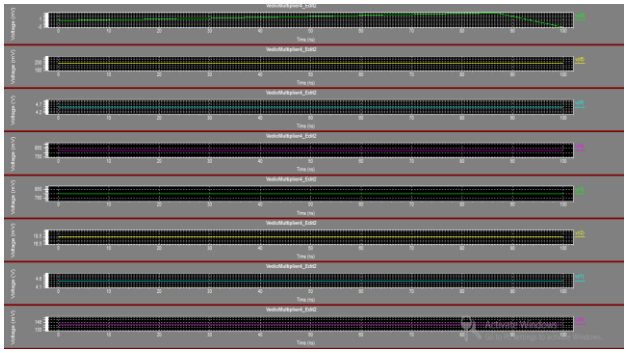


Figure12: Output of 4-bit Multiplier in 180nm technology

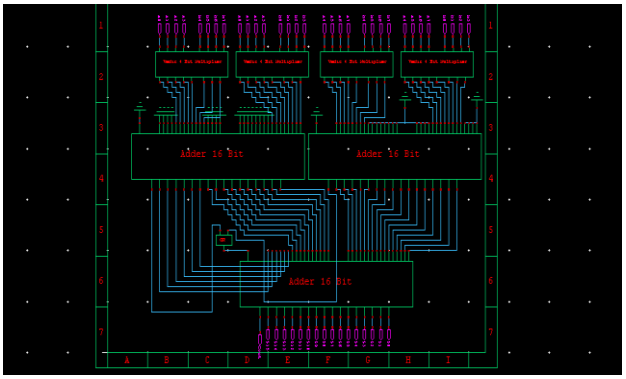


Figure 13: Schematic of 8-bit Multiplie

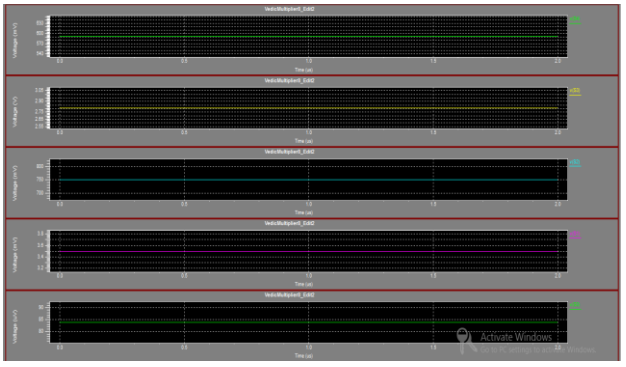


Figure 14: Output of 8-bit Multiplier in 180nm Technology

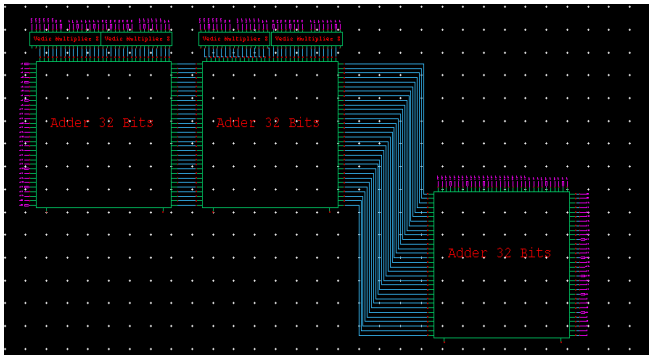


Figure 15: Schematic of 16-bit Multiplier

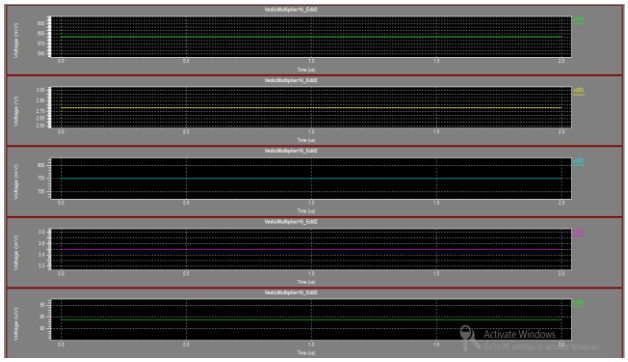


Figure 16: Output of 16-bit Multiplier in 180nm Technology

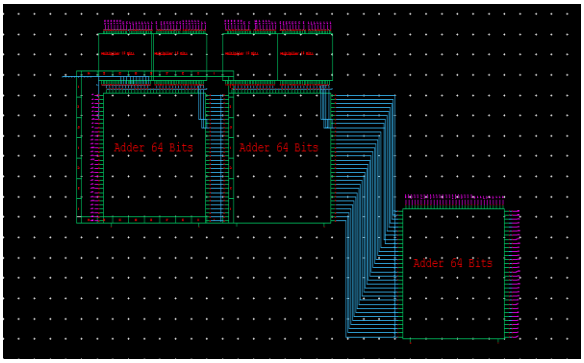


Figure 17: Schematic of 32-bit Multiplier

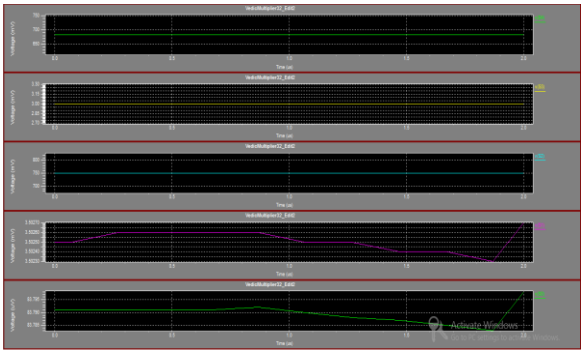


Figure 18: Output of 32-bit Multiplier in 180nm Technology

The output of 4-bit multiplier, 8-bit multiplier , 16-bit multiplier , 32-bit multiplier on 180nm technology is shown in above fig and its parameter on 180nm technology is shown in table below.

Multiplier	*Technology*	*Parameter*	
		No. of gates	*Power*
4-bit multiplier	180nm	240	2.6689×10^{-3}
8-bit multiplier	180nm	1638	1.6733×10^{-3}
16-bit multiplier	180nm	3276	5.0198×10^{-3}
32-bit multiplier	180nm	6552	2.1836×10^{-2}

3. Conclusion

In the present paper we generated a full adder using this full adder we generate 4-bit, 8-bit,16-bit & 32 -bit adder. We use these adder and generated the 4-bit , 8-bit, 16-bit & 32-bit multiplier . Also all the multipliers are generated using a Ancient Indian Vedic Mathematics technique.And we will see the result of adder & multipliers on 180nm technology.In that no. of gates are continuously increasing according to that power level change but when we apply same input then power increases. In the proposed work we can used the concept of pipelining to improve the generated result.

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