two 4:2 compressor, two full adder and one half adder and the architecture of same has been shown in fig 5 [1].

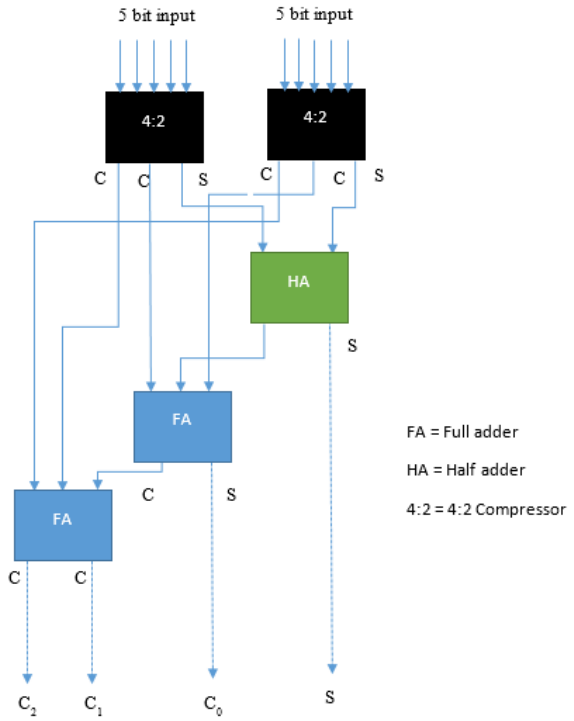

Figure 5: 7:2 compressor using 4:2 compressor, half adder and full adder [1]

7:2 compressor has also been coded in Verilog and tested in Xilinx ISE design suit 14.5. It has been seen that the proposed 7:2 compressor is 1.05 times faster than the conventional 7:2 compressor.

4. Proposed Methodology

In this paper 8 bit high speed multiplier architecture has been implemented using Vedic mathematics (Urdhwa Tiryakbhyam Sutra), proposed 4:2 and 7:2 compressors have been introduced for the addition of partial products, this approach significantly increase the speed of Vedic multiplier. Significance of 4:2 and 7:2 compressors has already been shown in previous section.

Further high speed 32 bit multiplier is designed using Urdhwa Tiryakbhyam, compressors and reconfigurable multiplication method.

4.1 8 Bit and 16 Bit Multiplier Architecture

8 bit multiplier architecture is implemented by Urdhwa Tiryakbhyam sutra. Now Let us consider two 8 bit multiplier and multiplicand X_7-X_0 and Y_7-Y_0 has to be multiplied this can be achieved by Urdhwa Tiryakbhyam method discussed in section 3. The following equation shows the procedure to generate all partial products. After that all partial product has been added using proposed compressors, full adder and half adder.

$$P_0 = X_0Y_0 \quad (1)$$
$$P_1 = X_0Y_1+X_1Y_0+C_1 \quad (2)$$
$$P_2 = X_2Y_0+X_0Y_2+ X_1Y_1+C_2 \quad (3)$$
$$P_3 = X_3Y_0+ X_0Y_3+ X_2Y_1+ X_1Y_2+C_3+ C_4 \quad (4)$$
$$P_4 = X_4Y_0+ X_0Y_4+ X_3Y_1+ X_1Y_3+ X_2Y_2+C_5+C_6 \quad (5)$$
$$P_5 = X_5Y_0+ X_0Y_5+ X_4Y_1+ X_1Y_4+X_3Y_2+ X_2Y_3 +C_7+ C_8+ C_9 \quad (6)$$
$$P_6 = X_6Y_0+ X_0Y_6+ X_5Y_1+ X_1Y_5+ X_4Y_2+ X_2Y_4+ X_3Y_3+C_{10}+C_{11}+ C_{12} \quad (7)$$
$$P_7 = X_7Y_0+ X_0Y_7+ X_6Y_1+ X_1Y_6+ X_5Y_2+ X_2Y_5+ X_3Y_4+X_4Y_3+C_{13}+C_{14}+C_{15}+C_{16} \quad (8)$$
$$P_8 = X_7Y_1+ X_1Y_7+ X_6Y_2+ X_2Y_6+ X_5Y_3+ X_3Y_5+ X_4Y_4+C_{17}+C_{18}+C_{19}+C_{20} \quad (9)$$
$$P_9 = X_7Y_2+ X_2Y_7+ X_6Y_3+ X_3Y_6+ X_4Y_5+ X_5Y_4+C_{21}+C_{22}+C_{23}+C_{24} \quad (10)$$
$$P_{10} = X_7Y_3+ X_3Y_7+ X_6Y_4+ X_4Y_6+ X_5Y_5+ C_{25} + C_{26}+ C_{27}+ C_{28} \quad (11)$$
$$P_{11} = X_7Y_4+ X_4Y_7+ X_6Y_5+ X_5Y_6+ C_{29}+ C_{30}+ C_{31} \quad (12)$$
$$P_{12} = X_7Y_5+ X_5Y_7+ X_6Y_6+ C_{32}+ C_{33}+ C_{34} \quad (13)$$
$$P_{13} = X_7Y_6+ X_6Y_7+ C_{35}+ C_{36} \quad (14)$$
$$P_{14} = X_7Y_7+ C_{37}+ C_{38} \quad (15)$$
$$P_{15} = X_7Y_7 \quad (16)$$

Equations (1) to (16) denote all the vertical and crosswise partial products and their addition according to Urdhwa Tiryakbhyam C_1 to C_{38} are carries. P_{15}-P_0 denote 16 bit output where P_0 is LSB and P_{15} is MSB.

16 bit high speed multiplier has also been implemented using Urdhwa Tiryakbhyam Sutra and using above mentioned equations. Compressors and look ahead carry adder has been used to add all partial products. A significant improvement has been observed in 16 bit multiplier as compared to conventional multiplier. Both 8 bit and 16 bit multiplier has been coded in Verilog language and synthesized in Xilinx ISE 14.5.

4.2 32-Bit High Speed Multiplier Architecture

However a different approach of multiplication with use of reconfigurable multiplier [13] in combination with Urdhwa Tiryakbhyam and compressors has been used to design a very efficient architecture for 32 bit multiplication.

To implement 32 bit multiplier A and B defined as the 2n-bits wide multiplicand and multiplier, respectively. A_H, B_H are their respective n most significant bits whereas A_L, B_L are their respective n least significant bits. A_L*B_L, A_H*B_L, A_L*B_H, A_H*B_H is the crosswise products. The product of A and B can be expressed as follows:

$$\text{PRODUCT (32 BIT)} = (A_H*B_H)\,2^{2n} + (A_H*B_L + A_L*B_H)\,2^n + A_L*B_L \text{ [13]}$$

Fig 6 describes the methodology used to implement 32 bit multiplier that is very efficient in terms of its speed. All the 16 bit and 8 bit multiplication have been implemented using Vedic Mathematics Urdhwa Tiryakbhyam Sutra. Final product of 32 bit multiplier has been calculated using above mentioned reconfigurable multiplier formulae.

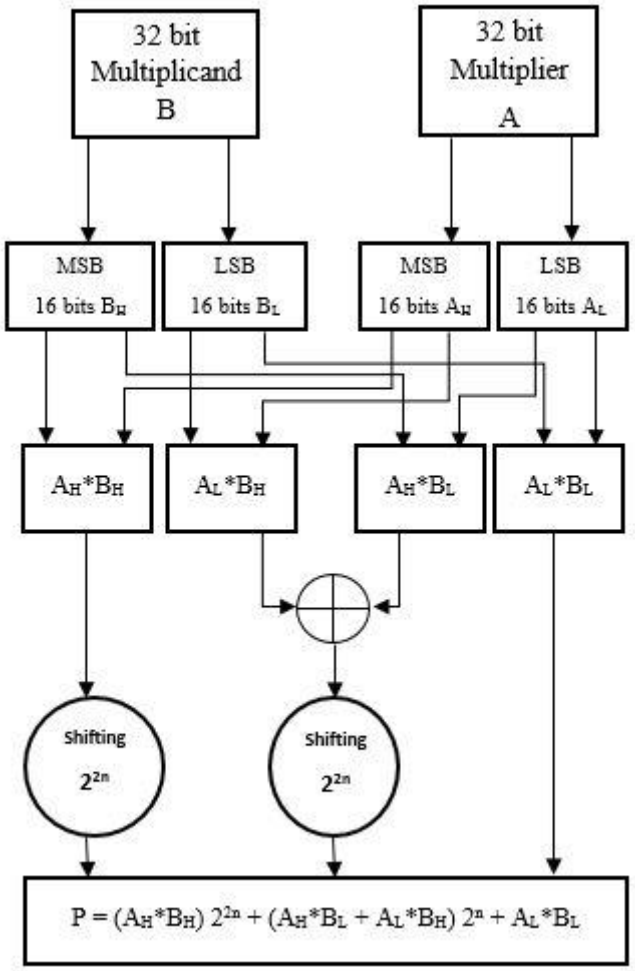

Figure 6: 32 bit proposed multiplier architecture

32 bit multiplier is coded in Verilog HDL (Hardware Description Language). Logic synthesis and simulation was done using EDA (Electronic Design Automation) tool in XilinxISE14.5 - Project Navigator and ISim simulator integrated in the Xilinx package. Spartan6 device XC6SLX16 has been used for synthesis in Xilinx.

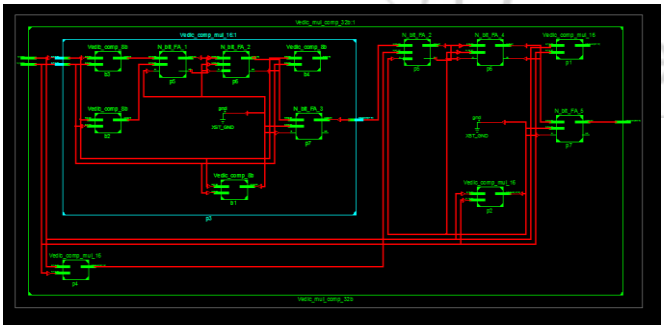

Figure 7: RTL of proposed 32 bit multiplier

upon comparison with various available multiplier proposed multiplier is best in speed. RTL and Simulation results have been shown in fig 7 and fig 8. Below simulation results have been shown.

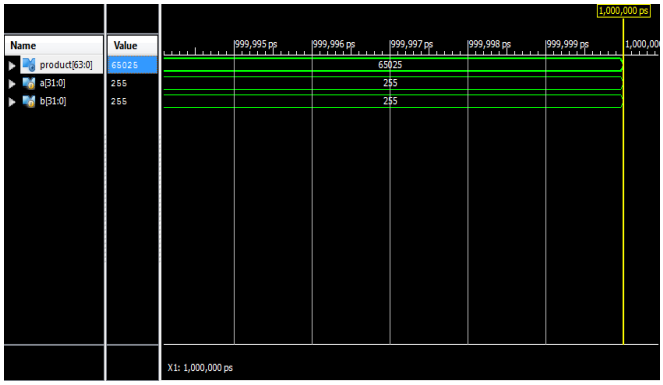

Figure 8: Simulation Result of proposed 32 bit multiplier

5. Results

The proposed 32 bit multiplier is coded in Verilog language, Simulated and synthesized using Xilinx XST for Spartan 6 xc6slx16-3csg324. Outputs are generated and verified for various possible inputs using Xilinx test bench.

Various popular multiplier such Vedic Multiplier, booth Multiplier and Conventional multiplier has also been implemented in Verilog HDL and compared with proposed 32 bit multiplier in terms of logic delay and route delay. A significant performance has been seen in proposed multiplier. All the results are tabulated in Table 1

Table 1: Comparison of Various Multiplier Architecture

Architecture	*Proposed 32 multiplier*	*Vedic Multiplier*	*Booth's multiplier*
Total Delay(ns)	44.249	63.120	128.068
Logic Delay(ns)	11.121	14.998	42.342
Route Delay(ns)	33.128	48.122	85.726
Logic level(ns)	38	57	75

From Table 1 it is evident that the proposed multiplier has reduction in total delay and logic level upon comparison with various multiplier it has been seen proposed multiplier is almost 2 times faster than Booth's multiplier and 1.5 times faster than conventional Vedic multiplier.

6. Conclusion

This paper presents a novel way of realizing 32 bit high speed multiplier using various research methods such as Urdhwa Tiryakbhyam sutra, compressors and reconfigurable multiplication method, methodology to implement same has also been discussed. As speed is major concern proposed multiplier is best in speed. As future work multiplier performance can be tested in ALU and can be compared with other existing multiplier.

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