

Design of 8 x 8 Vedic Multiplier using Quaternary-Logic & Pipelining Architecture

Vivek D. Wanjari¹, Prof. R. N. Mandavgane², Prof. Shailesh Sakhare³

¹M.Tech (IV SEM), Electronics Engineering (Comm.), SDCOE, Selukate, Wardha, India

²Associate Professor and Head, Dept. of E&T Engineering, BDCOE, Sewagram, Wardha, India

³Assistant Professor, Dept. of Electronics Engineering M SDCOE, Selukate, Wardha, India

Abstract: *In recent years the growth of the portable electronic is forcing the designers to optimize the existing design for better performance. A multiplication is the important operation used in various applications like DSP processor, math processor and in various arithmetic circuits. In VLSI system the overall performance is strongly depends on the performance of arithmetic circuits like multiplier. Designers find the solution of these by implementing technique of calculation based on Indian Vedas mathematics called as Vedic multiplier, which offers simple way of multiplication. The multi valued logic (MVL) provides the key benefit of a higher density per integration circuit area compared to traditional two valued binary logic. All so the Quaternary logic offers the benefit of easy interfacing to binary logic because radix 4 allow for the use of simple encoding/decoding circuits. This paper present design of 8x8 Vedic multiplier using Tanner EDA tool & simulated using T-spice simulator. With the help of pipelining technique 8x8 Vedic multiplier circuit level has been proposed in these paper, as it does not increase the hardware that much, but which increase the speed and requires less computation gives us better speed. The two stages pipelining is used to optimize Delay and Power and compared with previously normal 8x8 Vedic multiplier results.*

Keywords: VLSI, Multi-valued logic (MVL), Quaternary logic, Vedic multiplier, Digital signals processing.

1. Introduction

A multiplier is one of the most important parts in any processor and most of the instruction in a typical processor is multiplication. Multiplication process is used in many neural computing and DSP applications like Instrumentation and Measurement, Communications, and Audio and Video processing, Graphics, Image Enhancement, 3-D Rendering, Navigation, Radar, GPS, and control applications like Robotics, Machine Vision and Guidance. In digital logic, the device size is reduced by reducing the size of the transistor. But up to a limit, because the size of transistor cannot be reduced indefinitely. The multi-valued logic apply to the multiplier design, word length & no of transistor can be greatly reduced. There are various multipliers for binary logic Such as Array multiplier, Booth multiplier, and Wallace tree multiplier and a Vedic multiplier. In recent years Vedic multiplier has caught the Attention because of its superiority over other multipliers. If the Functional blocks designed in multi-valued logic are used in Vedic multiplier's architecture, it will surely enhance the performance of multiplier and hence the whole area & power consumption of chip. The performance of two levels binary logic is limited due to interconnects which occupy a large area on a VLSI chip. In VLSI circuit, total 70% of the area is divided to interconnection, 20% to insulation, and 10% to device. One can achieve a cost-effective way of utilizing Interconnections by using a larger set of signals over the same area in multiple-Valued logic (MVL) devices, allowing easy implementation of circuits. In MVL advantage of binary logic is retained. The higher radix in Use is the ternary and the quaternary logic. The Binary logic has many drawbacks and limitations. A signal cannot always be just ON or OFF or DON'T CARE, and HIGH IMPEDANCE. It does not mean that these states can result in inefficient processing of the data. Also, digital logic results in longer

word-lengths which is get increase the number of interconnections and hence the chip size. Multiplier design in Vedic mathematics has improved conventional delay time, area size to minimizing power dissipation while still maintaining the high performance. The low power and high speed multipliers can be implemented with different logic style.

2. Vedic Mathematics

A 'Veda' is a Sanskrit word that means 'knowledge'. The name Vedic Mathematics which is used & heard many times with reference to the techniques for solving problems mentally. The techniques of math that is Vedic mathematics were rediscovered in the early twentieth century from ancient Indian sculptures by Sri Bharati Krishna Tirthaji Maharaj. These methods can be directly applied to Trigonometry, plain & spherical geometry, conics, calculus and applied mathematics of various kinds. Total 16 sutras or formulae given in ancient Vedas out of these two sutras are useful for multiplication namely Nikhilam sutra. That means "all from 9 and last from 10" and Urdhva Tiryakbhyam sutra that means "vertically and crosswise". The Urdhva Tiryakbhyam sutra is more popular than Nikhilam sutra since it is applicable in all cases.

3. Multi-Value Logic (MVL)

It was proposed by Jan Lukasiewicz in 1919. Followed by Emil Post, American logician born in Poland the MVL employs more than two discrete levels of a signal, such as ternary & quaternary logic. There are two logic systems are available in ternary logic. Those are balanced ternary logic - 1, 0 and 1 and simple ternary logic 0, 1 and 2. The 0, 1, 2 and 3 logic levels are used by quaternary logic.

4. Operating Mode of MVL

MVL can be employed in either Voltage-Mode or Current-Mode. In voltage-mode MVL, operating voltage range is divided into the number of logical values to be represented, whereas, in current-mode MVL, currents are usually defined to have logical levels that are integer multiples of a reference current unit. For higher radix MVL system, current-mode is always preferred over voltage-mode because currents can be copied, scaled and algebraically sign-changed with a simple current mirror. The frequently used linear sum operation can be performed simply by wiring, resulting in a reduced number of active devices in the circuit. It is believed that current-mode MVL designs can allow better noise margin than voltage-mode MVL designs.

5. Urdhva-Tiryakbhyam Sutra

Urdhva Tiryakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. It literally means "Vertically and crosswise". It is based on a novel concept through which the generation of all partial products can be done and then, concurrent addition of these partial products can be done. Thus parallelism in generation of partial products and their summation is obtained. The Urdhva Tiryakbhyam sutra (method) was selected for implementation since it is applicable to all cases of multiplication. Multiplication of two no's using Urdhva Tiryakbhyam sutra is performed by vertically and crosswise, crosswise means diagonal multiplication and vertically means straight above multiplication and taking their sum. Thus any multi-bit multiplication can be reduced down to single bit multiplication and addition using this method. Moreover, the carry propagation from LSB to MSB is reduced due to one step generation of partial product.

6. Concept of Pipelining

Pipelining is one of the popular methods to realize high performance computing platform. Pipelining is a technique where multiple instruction executions are overlapped. It comes from the idea of a water pipe continue sending water without waiting the water in the pipe to be out. By pipelining the unit of a system we can produce result in every clock cycle. It leads to a reduction in the critical path. It can either increase the clock speed (or sampling speed) or reduces the power consumption at same speed in a system.

7. Multipliers

A multiplier is an essential component. Longer word-lengths in binary logic make the multiplier large and complex. In binary logic, the size of the device is reduced by reducing the sizes of the transistors. But it has a limit, since the sizes of transistors cannot be reduced indefinitely. By applying MVL to the multiplier design, word-lengths and the area can be reduced. This will enhance the performance of multipliers and hence the whole chip.

7.1 A 2x2 Vedic Multiplier

In 2x2 bit multiplier, the multiplicand has 2 bits each and the result of multiplication is of 4 bits. So in input the range of inputs goes from (00) to (11), output lies in the set of (0000, 0001, 0010, 0011, 0100, 0110, 1001). By using Urdhva Tiryakbhyam, multiplication takes place. Here multiplicands a And b are taken to be (10) both. The first step is the vertical multiplication of LSB of both multiplicands, and second step is the crosswise multiplication and addition of the partial products. Then Step 3 involves vertical multiplication of MSB of the multiplicands and addition with the carry propagated from Step 2.

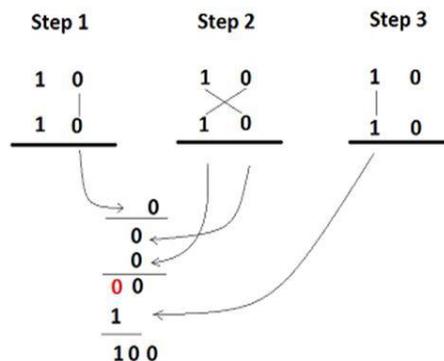


Figure 1: 2X2 Multiplication using Urdhva Tiryakbhyam Sutra.

7.2 A Multiplication of two Decimal Numbers 252 x 846.

For Example, let us consider the multiplication of two decimal numbers 252 x 846 by Urdhva-Tiryakbhyam method. The digits on the both sides of the line are multiplied and added with the carry from the previous step. This generates one of the bits of the result and a carry. This carry is added in the next step and hence the process goes on. If more than one line are there in one step, all the results are added to the previous carry. In each step, least significant bit acts as the result bit and all other bits act as carry for the next step. Initially the carry is taken to be zero.

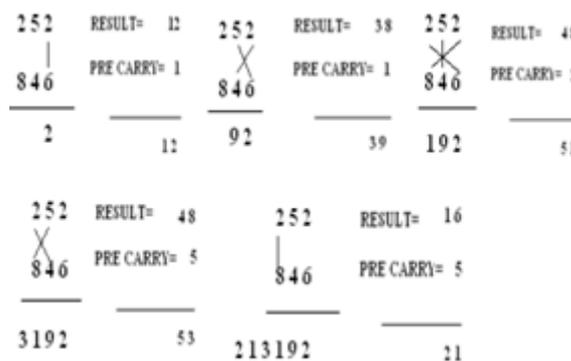


Figure 2: Example of Multiplication of Three Digits No.

7.3 A 4x4 Vedic Multiplier

The block diagram of 4x4 Vedic Multiplier is shown in Figure2. This multiplier is modelled using structural style of modelling using VHDL. In this paper first a 2x2 Vedic Multiplier is implemented using the above mentioned method. The 4x4Vedic Multiplier is designed. Using four

2x2 Vedic Multipliers After that 8x8 Vedic Multiplier is implemented using four 4x4 Vedic Multipliers by using pipeline concept. Finally the results will be compared with the standard results.

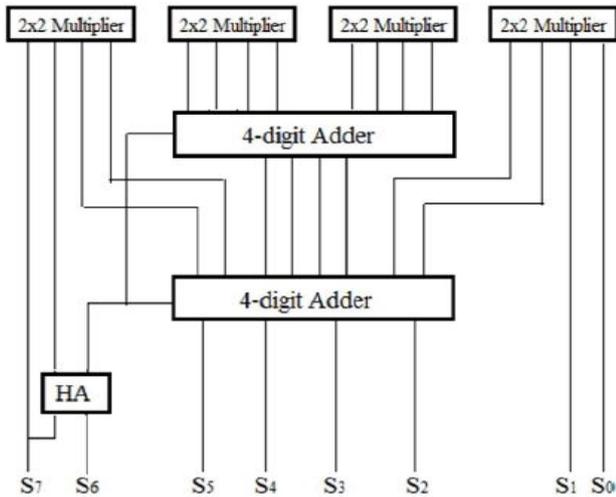


Figure 3: A Quaternary 4x4 Vedic Multiplier

8. Simulation & Results

Figure 3 shows Four Quadrant Vedic multiplier. It can be surely concluded that the Application of current-mode MVL reduces the number of adders in the multiplier architecture as the number of bits to be processed goes on increasing. Furthermore, proposed 4x4 quaternary multiplier and by using pipeline architecture design of 8x8 Vedic Multiplier, which shows great reduction in the circuitry because of MVL.

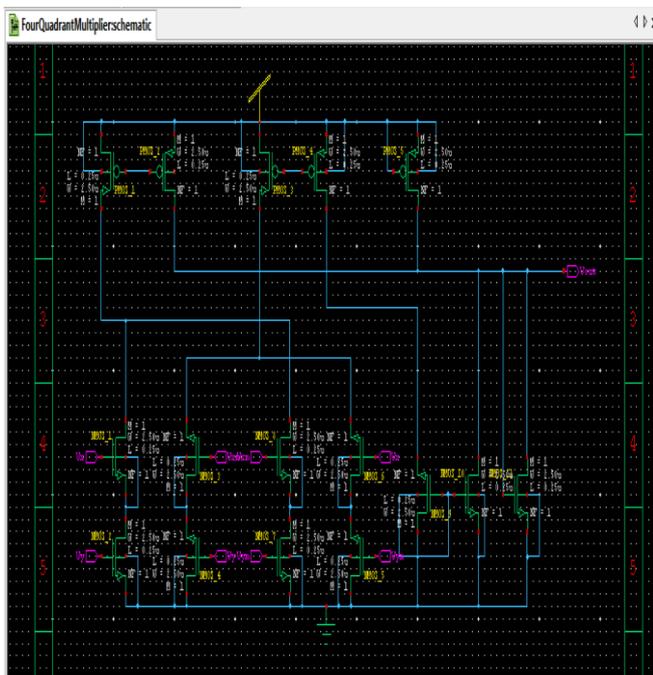


Figure 4: Synthesize result of Four Quadrant Vedic Multiplier

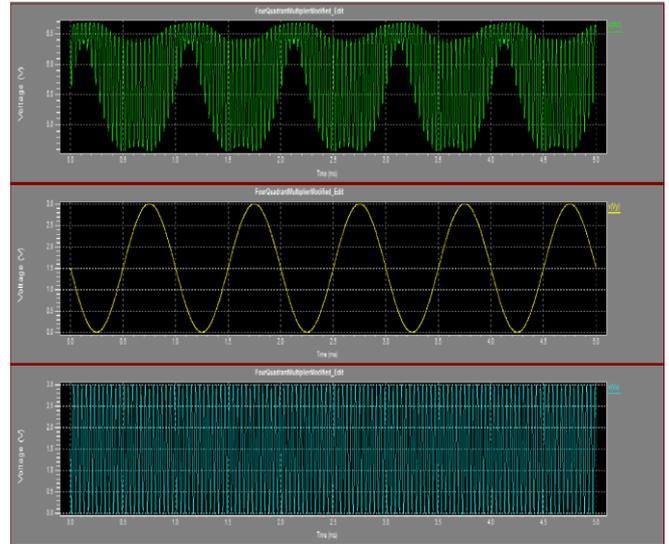


Figure 5: Simulation result of Four Quadrant Vedic Multiplier

Table 1: Results Comparison Quadrant Multipliers at different voltage level

Sr. No	Parameters	Values For 7v supply	Values For 5v supply
1.	Technology used	CMOS 180 nm	CMOS 180 nm
2.	Average Power Consumption	1.4324e-04 watt	1.2662e-04 watt
3.	No. of Gate Counts	11	11
4.	Absolute Area	9720e-06 meter	9720e-06 meter
5.	Total Simulation Time	3.44 sec	3.72 sec

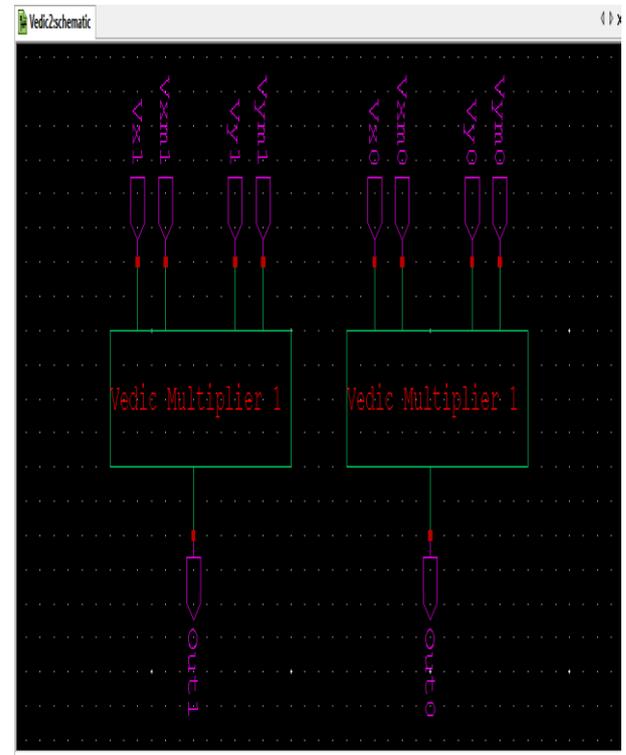


Figure 6: A 2-Sample/Bit Vedic Multiplier.

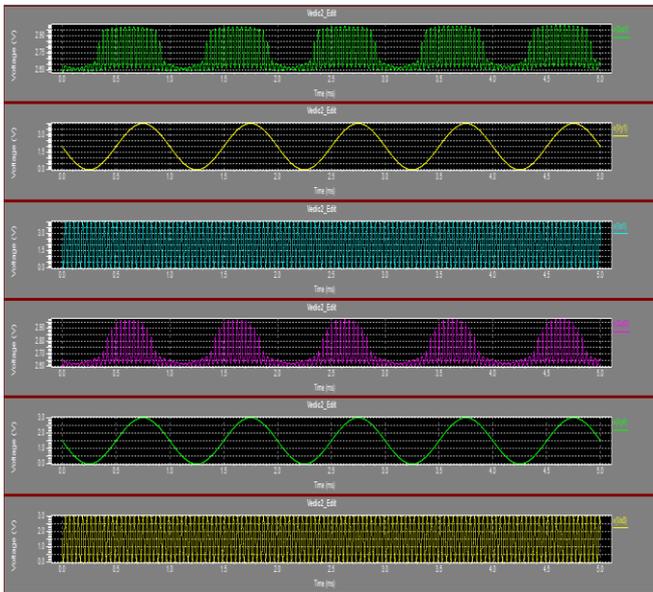


Figure 7: Simulation result of 2-Bit Vedic Multiplier

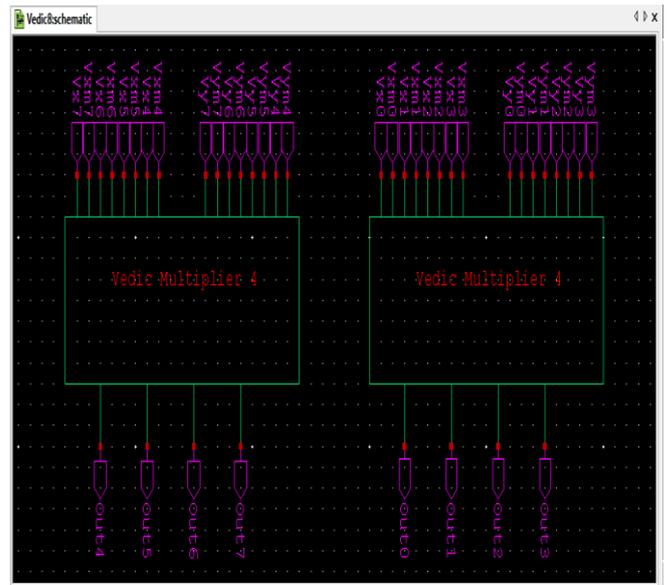


Figure 10: An 8-Sample/Bit Vedic Multiplier.

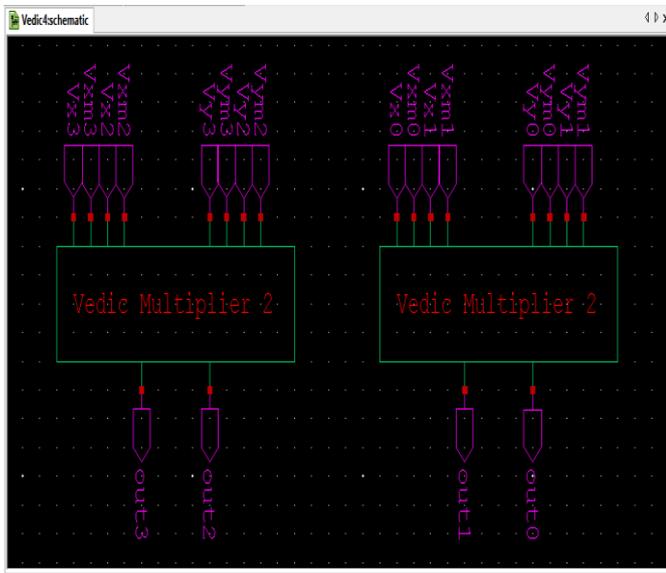


Figure 8: 4-Sample/Bit Vedic Multiplier

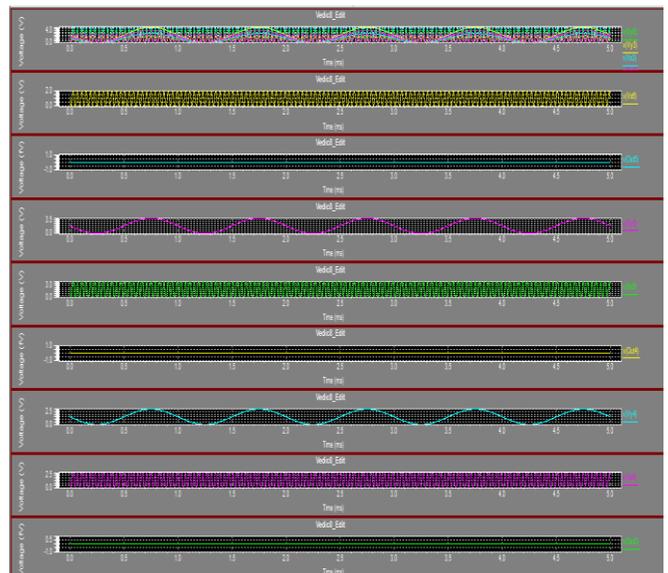


Figure 11: Simulation result of 8-Bit Vedic Multiplier

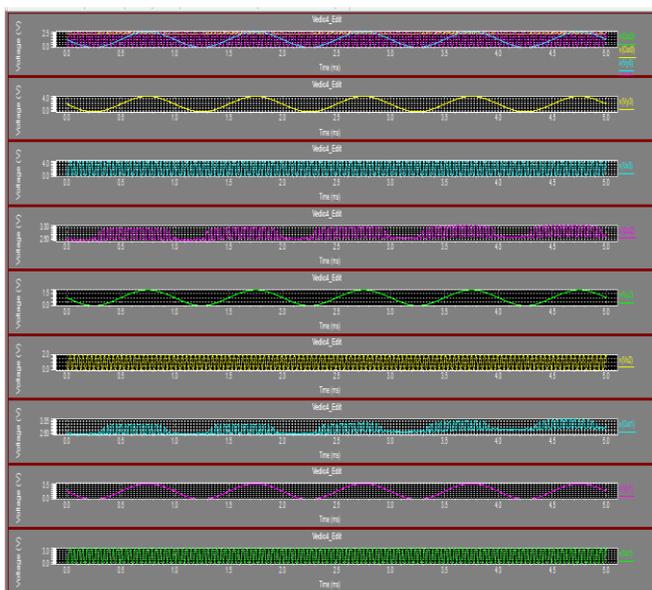


Figure 9: Simulation result of 4-Bit Vedic Multiplier

Table 2: Results Comparison Quadrant Multipliers at different voltage level

Sr. No	Parameters	2-Bit Multiplier Values For 5v supply	4-Bit Multiplier Values For 5v supply	8-Bit Multiplier Values For 5v supply
1	Technology used	CMOS 180nm	CMOS 180 nm	CMOS 180nm
2	Average Power Consumption	1.7158e-002 Watt	3.4427e-002 Watt	6.8853e-002 Watt
3	No. of Gate Counts	41	81	161
4	Absolute Area	129e-06 Meter	2.99e-06 Meter	518e-06 Meter
5	Total Simulation Time	14.08 Sec	25.91 Sec	28.98 Sec

9. Conclusion

The paper shows the efficient use of Vedic multiplication method in order to multiply two numbers. Here we introduce the concept of pipelining so that lesser number of LUTs

verifies that the hardware requirement is reduced, Thereby reducing the power consumption without compromising delay so much.

10. Scope of Future Work

An improvement in multiplication speed by using new techniques can greatly improve system performance. This project can be extended for the reconfigurable architecture.

11. Acknowledgement

I wish to Prof. R. N. Mandavgane and other contributor to give their contribution for developing this topic related search. I also thankful to all the authors of different books which guide me a lot.

References

- [1] Ashish S. Shende, M. A. Gaikwad, D. R. Dandekar. "Design of Efficient 4×4 Quaternary Vedic Multiplier Using Current-Mode Multi-Valued Logic", Int. J. on Recent Trends in Engineering and Technology, Vol. 10, No. 2, Jan 2014.
- [2] Diogo Brito, Jorge R. Fernandes, Jose Monteiro. "Quaternary Logic Lookup Table in Standard CMOS", IEEE Transaction on Very Large Scale Integration (VLSI) System 2014.
- [3] Riya Saini, Tina G. Galani, R. D. Daruwala. "Efficient Implementation of Pipelined Double Precision Floating Point Unit on FPGA", International Journal of Emerging Trends in Electrical and Electronics (IJETEE – ISSN: 2320-9569) Vol. 5, Issue. 1, July-2013.
- [4] Ashish S. Shende, M. A. Gaikwad, D. R. Dandekar. "Application of Current-Mode Multi-Valued Logic in the Design of Vedic Multiplier", International Journal of Computer Applications (0975 – 8887) Recent Trends in Engineering Technology-2013.
- [5] Deeraj Jain, Dr. Ajay Somkuwar. "Implementation and Performance Analysis of a Vedic Multiplier Using Tanner EDA Tool", IJSRD–International Journal for Scientific Research & Development vol. 1, Issue 5, 2013.
- [6] Arun K. Patro, Kunal N. Dekate. "A Transistor Level Analysis For a 8-Bit Vedic Multiplier", International Journal of Electronics Signals and Systems (IJESS) ISSN: 2231- 5969, Vol-1 Iss-3, 2012.
- [7] S.Kokila, R.Ramadhurai, L.Sarah. "VHDL Implementation of Fast 32X32 Multiplier based on Vedic Mathematics", International Journal of Engineering Technology and Computer Applications Vol.2, No.1, Apr 2012.
- [8] Aniruddha Kanhe, Shishir Kumar Das, Ankit Kumar Singh. "Design and Implementation of Floating Point Multiplier based on Vedic Multiplication Technique", International Conference on Communication, Information & Computing Technology (ICCICT), Oct. 19-20, 2012.
- [9] Sumit R. Vaidya. "Design of High Performance 8x8-bit Multiplier Based on Vedic Mathematics in ASIC",

Dissertation for M.Tech. Project, BDCOE, RTM Nagpur University, January 2011

- [10] Sumit R. Vaidya and Deepak Dandekar. "Delay-Power Performance Comparison of Multipliers in VLSI Circuit Design", International Journal of Computer Networks & Communications (IJCNC), Vol.2, No.4, July 2010.

Author Profile



Mr. Vivek Wanjari is a PG scholar doing his M.Tech in Electronic (comm.) branch from SDCE Institute of Technology selukate, RTMNU University, and Wardha. He received his B.E. (Electronics and Telicomm. Engineering) Degree from D.M.I.E.T.R college of Engineering, R.T.M.N.U University, Wardha in 2013.



Mrs. Rajashree N. Mandavgane received her B.E degree and M.Tech degree from R.T.M.N.U University, Maharashtra, India. She is presently working as associate Professor and Head in the department of Electronics and Communication Engineering, BDCOE Institute of Technology, sevagram, Wardha. She is having a total of 23 years of teaching experience. With a subject specialization in general and digital electronics.



Mr. Shailesh Sakhare has completed his B.E and M.Tech in R.T.M.N.U University. He has Five years of teaching experience in various engineering colleges. Currently he holds the post of Assistant professor in the Department of Electronics Engineering, SDCE Institute of Technology, selukate, Wardha, Maharashtra, India. He has published more than 2 research papers in international journals. He has attended various International and National conferences.