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Hardware Implementation of MLI Based Dynamic Voltage Restorer

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Abstract: ***The Dynamic voltage restorer [IDVR], a custom power device has been used to protect sensitive loads from the effect of voltage sags on the distribution feeder. This paper presents the implementation aspects of the DVR system with the MLI working against voltage sags/swell by using a microcontroller. The scope of this paper is to facilitate the use of MLI based DVR in voltage restoration process by correcting the voltage fluctuations. The hardware implementation is carried out. DC-DC converter is used to adjust the DC link voltage considering the amount of voltage sag so that the maximum possible output voltage levels are generated for a wide range of voltage sags.***

Keywords: Power quality, Dynamic voltage Restorer [DVR], Multilevel Inverter [MLI], Pulse width modulation [PWM]

1. Introduction

A common characteristic of most electronics is that they are sensitive to voltage variations. Computers and other sensitive loads can lower their performance or even shutdown the process they are in control due to those variations. Voltage variations can be classified as disturbances that produce voltages below the nominal value, which are called voltage sags, and disturbances that produce voltages above the nominal value, which are called voltage swells.

Voltage sag is defined as a sudden reduction of supply voltage down 90% to 10% of nominal, followed by a recovery after a short period of time. Atypical duration of sag is 10ms to 1 minute. Voltage sag can cause loss of production in automated processes since voltage sag can trip a motor or cause its controller to malfunction. Voltage swell is defined as sudden increasing of supply voltage up 110% to180% in RMS voltage at the fundamental frequency with duration from 10ms to 1 minute. Switching off a large inductive load or energizing a large capacitor bank is atypical system event that causes swells. During power disturbances Dynamic Voltage Restorer (DVR) installed in front of a critical load will appropriately provide correction to that load only. Also DVR cannot provide compensation during full power interruptions. Voltage sag is a momentary decrease in RMS voltage lasting between half a cycle to a few seconds. It is generally caused by faults in the power system and is characterized by its magnitude and duration. Voltage sag magnitude is defined as the net RMS voltage during voltage sag, which is usually in per unit of the nominal voltage level. The voltage sag magnitude depends on various factors like the type of fault, the location of the fault and the fault impedance.

Voltage sag/swell is most important power quality problems challenging the utility industry can be compensated and power is injected into the distribution system. By injecting voltage with a phase advance with respect to the sustained source-side voltage, reactive power can be utilized to help voltage restoration [1]. Dynamic Voltage Restorer, which consists of a set of series and shunt converters connected back-to-back, three series transformers, and a dc capacitor installed on the common dc link [3]. The Pulse-width modulation of Z-source inverter has recently been proposed as an alternative power conversion concept as they have both voltage buck and boost capabilities [4].The Z-source converter employs a unique X-shaped impedance network on its dc side for achieving both voltage-buck and boost capabilities this unique features that cannot be obtained in the traditional voltage-source and current-source converters. The proposed system is able to compensate long and significantly large voltage sags [2], [5] and [9].

Passivity-based dynamical feedback controllers can be derived for the indirect stabilization of the average output voltage. The derived controllers are based on a suitable stabilizing "damping injection" scheme [7]. Transformerless self-charging dynamic voltage restorer series compensation device used to mitigate voltage sags.

A detailed analysis on the control of the restorer for voltage sag mitigation and dc-link voltage regulation are presented [8]. Installation of the world's first Dynamic Voltage Restorer (DVR) on a major use. Utility system to protect a critical customer plant load from power system voltage disturbances. The installed system at an automated yarn manufacturing and weaving factory provides protection from disturbances [10].

The modeling and simulation of ZSI based DVR is presented [11] and [13]. The modeling and simulation of IDVR is presented [12] and [15]. Simulation of MLI based DVR is presented in [16].In this paper the modeling and implementation of Multilevel inverter based dynamic voltage restorer for voltage sag compensation is presented. The simulation results are presented to show the effectiveness of the proposed control method.

2. Dynamic Voltage Restorer

The control strategy is designed using the in-phase compensation technique. Voltage sag is detected as a sudden change in the magnitude of the load voltage.

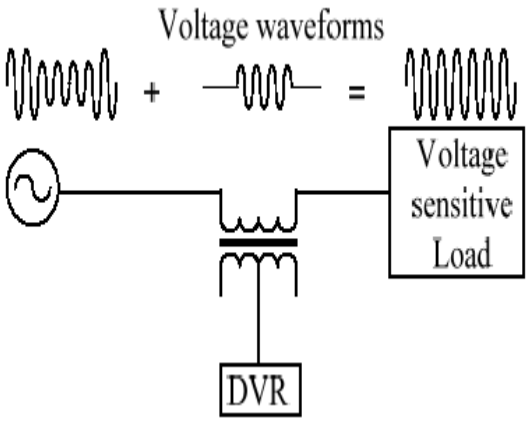

Figure 1: Basic Operation of DVR

Dynamic voltage restorer was originally proposed to compensate for voltage disturbances on distribution systems. A typical DVR scheme is shown in Figure 1. The restoration is based on injecting AC voltages in series with the incoming three-phase network, the purpose of which is to improve voltage quality by adjustment in voltage magnitude, wave-shape, and phase shift. These are important voltage attributes as they can affect the performance of the load equipment. Voltage restoration involves energy injection into the distribution systems and this determines the capacity of the energy storage device required in the restoration scheme.

Figure 2 shows the proposed DVR. It consists of energy storage, a dc/dc converter, a multilevel inverter and the injection transformers. The capacitor C is used as a filter. The main aim in the proposed topology is to adjust the dc link voltage according to the amount of voltage sag. The dc output voltage of the energy storage (Vin) is given to a dc/dc converter as its input voltage. The dc/dc converter offers a variable dc link voltage (Vdc) so that it can be adjusted considering the amount of voltage sag. A new method for application of a multilevel inverter in the DVR structure is proposed in this paper. The proposed method relies on the adjusting the dc voltage input of the multilevel inverter using a dc/dc converter according to the voltage sag. As a result, for a wide range of voltage sag, the proposed DVR generates all of the possible voltage levels which is not possible in the existing methodologies. Cascaded seven level inverter is used.

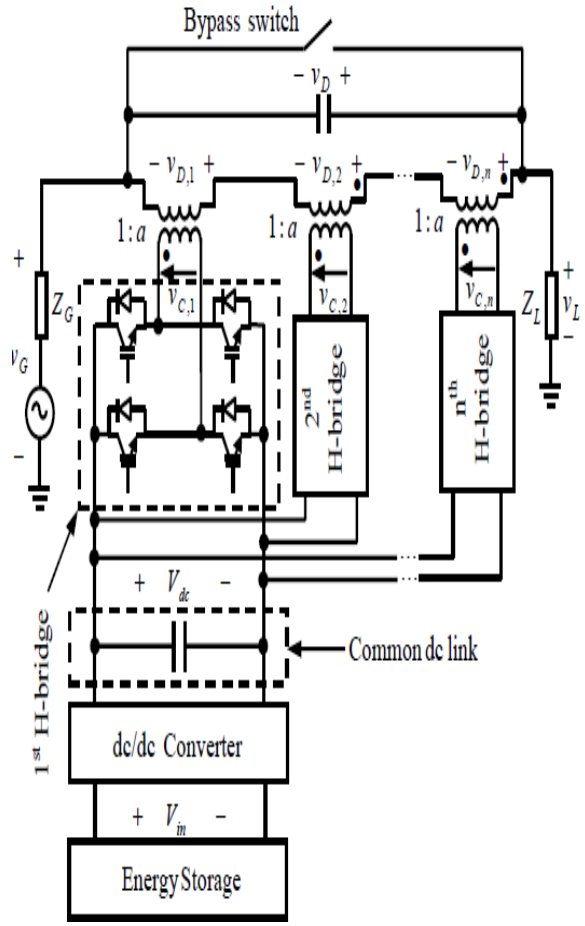

Figure 2: Block Diagram of MLI based DVR

Considering the fact that in the proposed topology the number of output voltage levels is maximum for a wide range of voltage sags, its quality improves considerably. The CHB multilevel inverter is used in this paper. It is important to note that the multilevel inverter should have a common dc link otherwise a dc/dc converter is required for each H-bridge. In order to use one common dc link, an injection transformer for each H-bridge is required. The H-bridges are supplied from one common dc link and the output voltages of them are added together via the injection transformers. The total resulting voltage is the injection voltage which compensates the voltage sag.

3. PIC16F887A Microcontroller

The hardware is implemented for the above Multilevel Level Inverter Based Dynamic Voltage Restorer for single phase. In the hardware implementation we make use of the PIC16F887A Microcontroller. The pin description details are explained in the following.

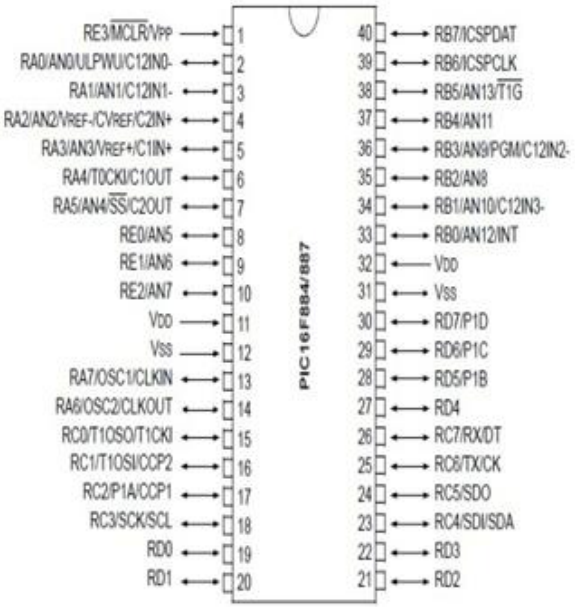

Figure 3: Pin Diagram of PIC16F887A

Table 1: Description of pins (1-12)

Name	Number (DIP 40)	Function	Description
RE3/MCLR/Vpp	1	RE3	General purpose input Port E
		MCLR	Reset pin. Low logic level on this pin resets microcontroller.
		Vpp	Programming voltage
RA0/AN0/ULPWU/C12IN0-	2	RA0	General purpose I/O port A
		AN0	A/D Channel 0 input
		ULPWU	Stand-by mode deactivation input
		C12IN0-	Comparator C1 or C2 negative input
RA1/AN1/C12IN1-	3	RA1	General purpose I/O port A
		AN1	A/D Channel 1
		C12IN1-	Comparator C1 or C2 negative input
RA2/AN2/Vref-/CVref/C2IN+	4	RA2	General purpose I/O port A
		AN2	A/D Channel 2
		Vref-	A/D Negative Voltage Reference input
		CVref	Comparator Voltage Reference Output
		C2IN+	Comparator C2 Positive Input
RA3/AN3/Vref+/C1IN+	5	RA3	General purpose I/O port A
		AN3	A/D Channel 3
		Vref+	A/D Positive Voltage Reference Input
		C1IN+	Comparator C1 Positive Input
RA4/T0CKI/C1OUT	6	RA4	General purpose I/O port A
		T0CKI	Timer T0 Clock Input
		C1OUT	Comparator C1 Output
RA5/AN4/SS/C2OUT	7	RA5	General purpose I/O port A
		AN4	A/D Channel 4
		SS	SPI module Input (*Slave Select*)
		C2OUT	Comparator C2 Output
RE0/AN5	8	RE0	General purpose I/O port E
		AN5	A/D Channel 5
RE1/AN6	9	RE1	General purpose I/O port E
		AN6	A/D Channel 6
RE2/AN7	10	RE2	General purpose I/O port E
		AN7	A/D Channel 7
Vdd	11	+	Positive supply
Vss	12	-	Ground (GND)

Table 2: Description of pins (13-26)

Name	Number (DIP 40)	Function	Description
RA7/OSC1/CLKIN	13	RA7	General purpose I/O port A
		OSC1	Crystal Oscillator Input
		CLKIN	External Clock Input
RA6/OSC2/CLKOUT	14	OSC2	Crystal Oscillator Output
		CLKO	Fosc/4 Output
		RA6	General purpose I/O port A
RC0/T1OSO/T1CKI	15	RC0	General purpose I/O port C
		T1OSO	Timer T1 Oscillator Output
		T1CKI	Timer T1 Clock Input
RC1/T1OSO/T1CKI	16	RC1	General purpose I/O port C
		T1OSI	Timer T1 Oscillator Input
		CCP2	CCP1 and PWM1 module I/O
RC2/P1A/CCP1	17	RC2	General purpose I/O port C
		P1A	PWM Module Output
		CCP1	CCP1 and PWM1 module I/O
RC3/SCK/SCL	18	RC3	General purpose I/O port C
		SCK	MSSP module Clock I/O in SPI mode
		SCL	MSSP module Clock I/O in I^2C mode
RD0	19	RD0	General purpose I/O port D
RD1	20	RD1	General purpose I/O port D
RD2	21	RD2	General purpose I/O port D
RD3	22	RD3	General purpose I/O port D
RC4/SDI/SDA	23	RC4	General purpose I/O port A
		SDI	MSSP module *Data* input in SPI mode
		SDA	MSSP module *Data* I/O in I^2C mode
RC5/SDO	24	RC5	General purpose I/O port C
		SDO	MSSP module *Data* output in SPI mode
RC6/TX/CK	25	RC6	General purpose I/O port C
		TX	USART Asynchronous Output
		CK	USART Synchronous Clock
RC7/RX/DT	26	RC7	General purpose I/O port C
		RX	USART Asynchronous Input
		DT	USART Synchronous Data

Table 3: Description of pins (27-40)

Name	Number (DIP 40)	Function	Description
RD4	27	RD4	General purpose I/O port D
RD5/P1B	28	RD5	General purpose I/O port D
		P1B	PWM Output
RD6/P1C	29	RD6	General purpose I/O port D
		P1C	PWM Output
RD7/P1D	30	RD7	General purpose I/O port D
		P1D	PWM Output
Vss	31	-	Ground (GND)
Vdd	32	+	Positive Supply
RB0/AN12/INT	33	RB0	General purpose I/O port B
		AN12	A/D Channel 12
		INT	External Interrupt
RB1/AN10/C12INT3-	34	RB1	General purpose I/O port B
		AN10	A/D Channel 10
		C12INT3-	Comparator C1 or C2 Negative Input
RB2/AN8	35	RB2	General purpose I/O port B
		AN8	A/D Channel 8
RB3/AN9/PGM/C12IN2-	36	RB3	General purpose I/O port B
		AN9	A/D Channel 9
		PGM	Programming enable pin
		C12IN2-	Comparator C1 or C2 Negative Input
RB4/AN11	37	RB4	General purpose I/O port B
		AN11	A/D Channel 11
RB5/AN13/T1G	38	RB5	General purpose I/O port B
		AN13	A/D Channel 13
		T1G	Timer T1 External Input
RB6/ICSPCLK	39	RB6	General purpose I/O port B
		ICSPCLK	Serial programming Clock
RB7/ICSPDAT	40	RB7	General purpose I/O port B
		ICSPDAT	Programming enable pin

The pin diagram of PIC16F887A is shown in Figure 3

Table 1, 2 and 3 gives the pin description of the microcontroller used.

4. Switching Pulse

The switching device used here is MOSFET (IRFP460). Here we make use of twelve switches.

Figure 4: MOSFET (IRFP460)

The PowerMESH™ is the evolution of the first generation of MESH OVERLAY™. The layout refinements introduced greatly improve the Ron*area figure of merit while keeping the device at the leading edge for what concerns switching speed, gate. This MOSFET IRFP460 finds application in Switched mode power supply (SMPS), High speed switching devices, DC-AC converters, Uninterruptible power supply (UPS) and in motor drives.

5. Implementation of Dynamic Voltage Restorer

The hardware setup of MLI based Dynamic voltage restorer is shown in Figure5. Twelve switching pulse devices are used namely S1, S2, S3, S4, S5, S6, S7, S8, S9, S10, S11 and S12.Fig6, Figure7, Figure8, Figure9 and Figure10 shows the switching pulses of switches S1 & S3, S2 & S4, S5 & S7, S6 & S8, S10 & S12.A LCD is connected to the setup to show the load applied. By varying the load and frequency as required, we get the desired output waveform. The response of MLI based DVR for voltage sag compensation, Uncompensated voltage, an injected voltage (seven level cascaded MLI) compensated voltages, Voltage sag compensation and voltage swell compensation are shown in Figure11, 12, 13, 14 & 15.

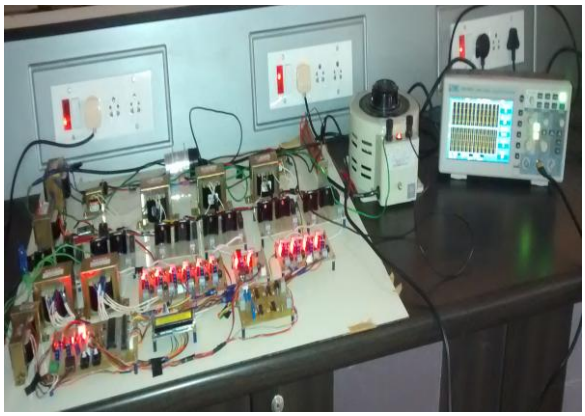

Figure 5: Hardware setup of MLI based DVR

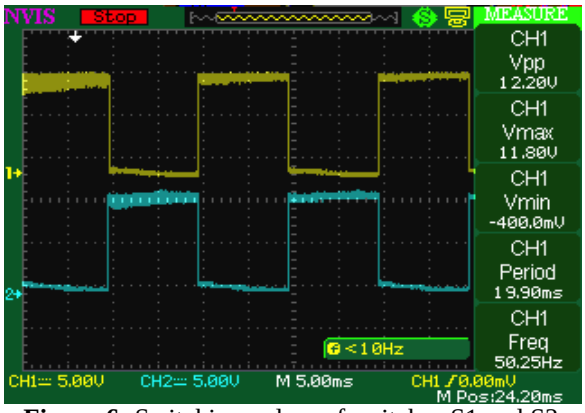

Figure 6: Switching pulses of switches S1 and S3

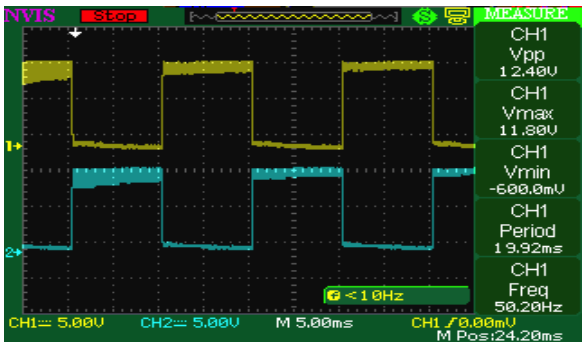

Figure 7: Switching pulses of switches S2 and S4

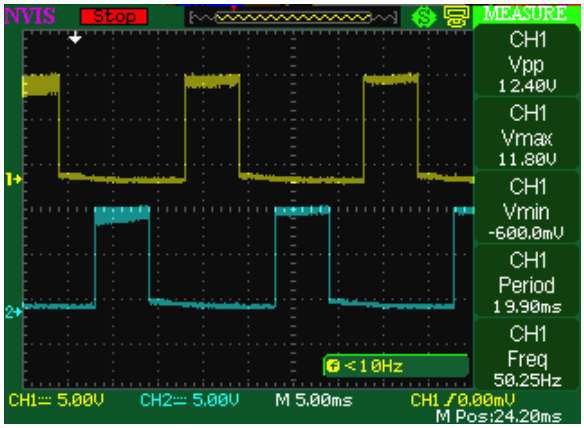

Figure 8: Switching pulses of switches S5 and S7

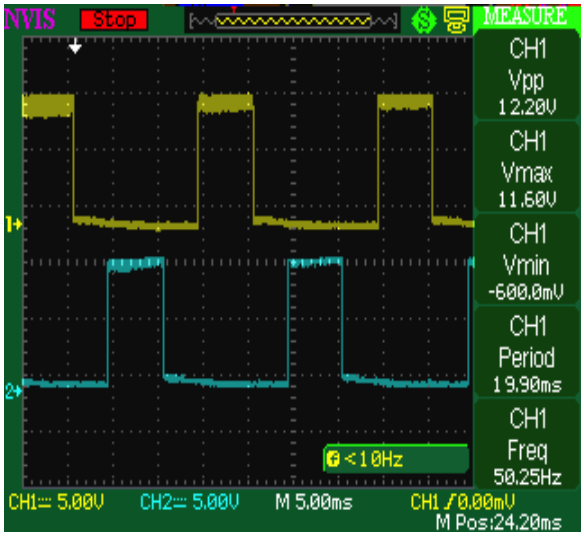

Figure 9: Switching pulses of switches S6 and S8

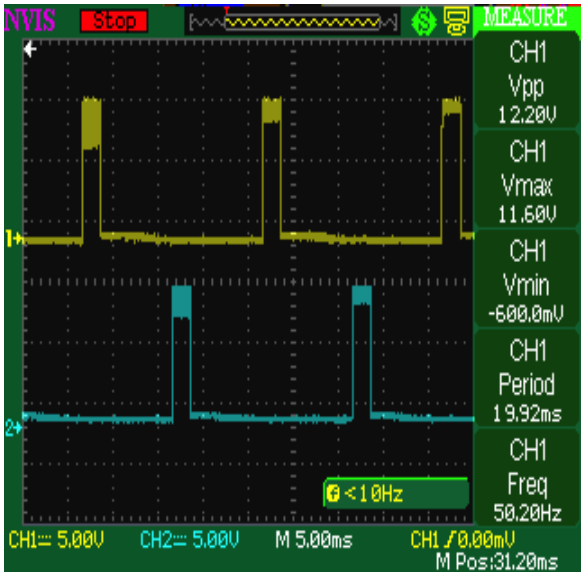

Figure 10: Switching pulses of switches S10 and S12

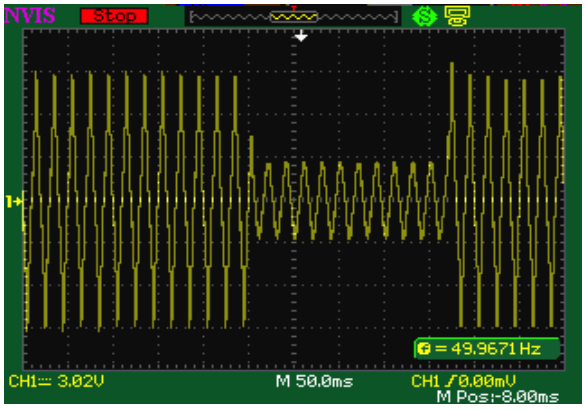

Figure 11: Uncompensated voltage

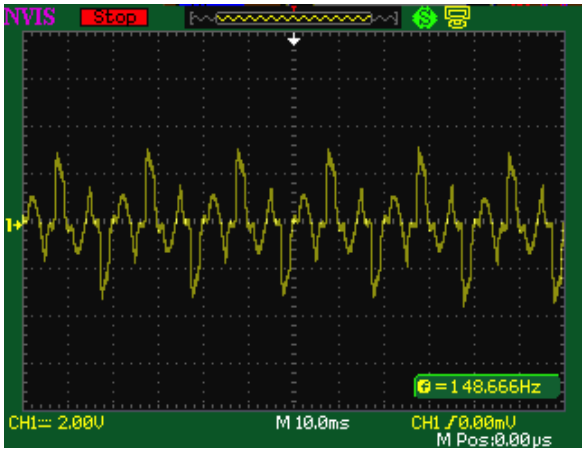

Figure 12: Injected voltage

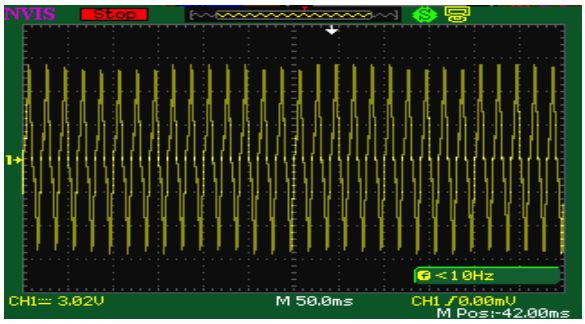

Figure 13: Compensated Voltage

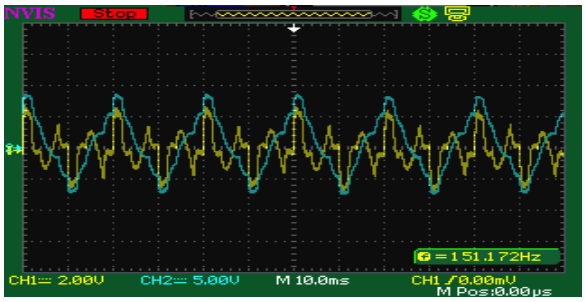

Figure 14: Voltage sag compensation

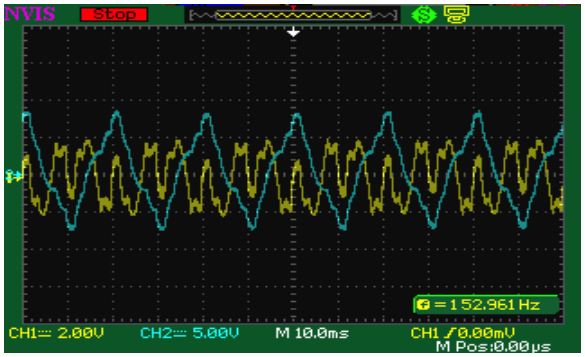

Figure 15: Voltage Swell compensation

6. Conclusion

The implementation of MLI based DVR system using microcontroller has been presented. DVR is an effective custom power device for voltage sag mitigation. The impact of voltage sag/swell on sensitive equipment is severe. Therefore, DVR is considered to be an efficient solution due to its low cost, small size and fast response. The simulation results indicate that the implemented control strategy compensates for voltage sags/swells with high accuracy. The results show that the control technique is simple and efficient method for voltage sag compensation.

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