1) Existing Vedic Multiplier
2) Proposed Multiplier.

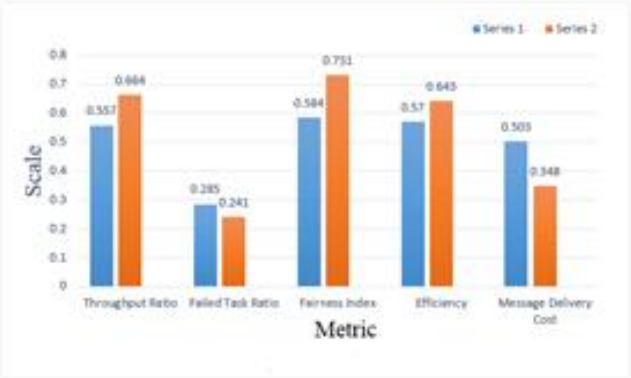

Figure 4: Performance analysis of proposed system vs existing systems

The overhead reduction achieved for computing Different Multiplier on analysis result, is visualized using a pie chart.

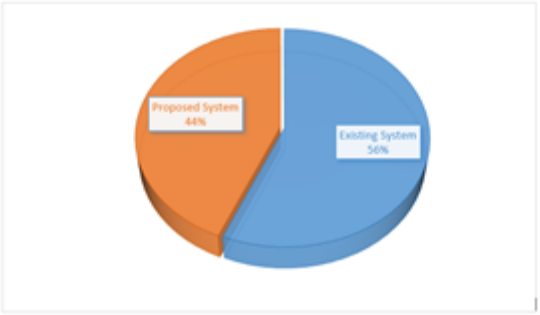

Figure 5: Computational Overhead

The values and the graph proves that this system is more efficient than any existing location calibration techniques based on the ground of fairness, adaptability, scalability and minimal cost for communication and calibration and has minimal computational overhead.

5. Conclusion

This entire work is based on creating a area delay and power efficient Vedic multiplier based on carry select adder. This paper presents a novel way of realizing a high speed multiplier using Urdhva Tiryagbhyam sutra and carry select addition technique. A 4-bit modified multiplier is designed. The 8-bit multiplier is realized using four 4-bit Vedic multipliers and proposed carry select adders. Carry select adders(CSLA) are modified such as all the redundant logic operations present in the conventional CSLA are eliminated and proposed a new logic formulation for CSLA. In the proposed scheme, the carry select (CS) operation is scheduled before the calculation of final-sum, which is different from the conventional approach. The proposed 8-bit multiplier gives a total delay of 15.050 ns which is less when compared to the total delay of any other renowned multiplier architecture. Results also indicate a 13.65% increase in the speed when compared to normal Vedic multiplier without carry select adder technique.

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