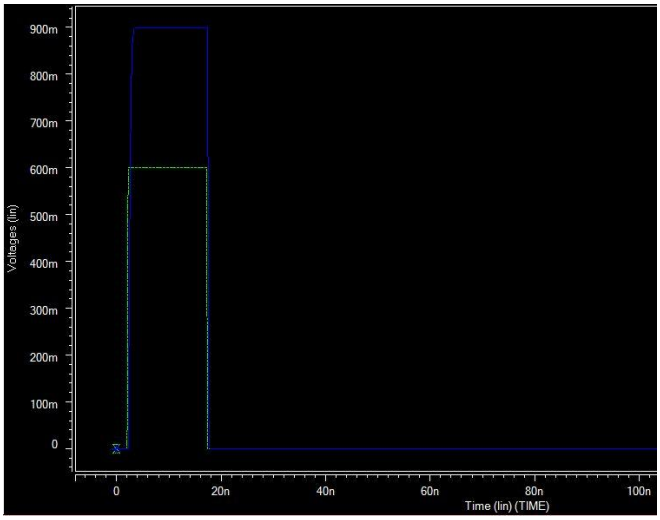
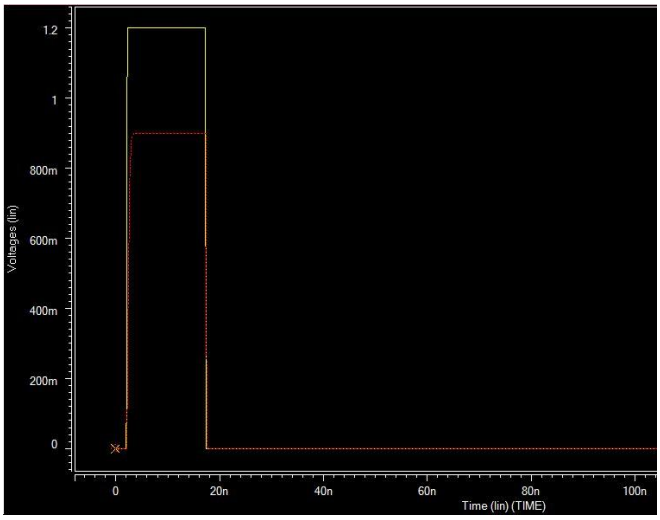


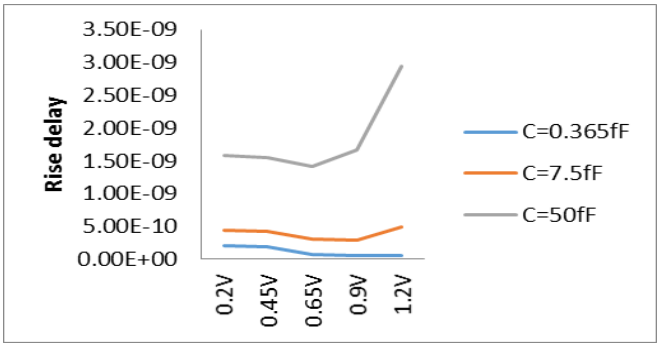

(c)



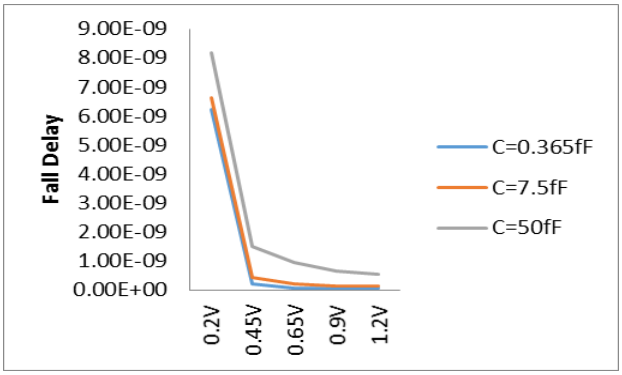

(d)

**Figure 6:** (a) Level shifting 0.1V to 0.9V, (b) Level shifting 0.3V to 0.9V, (c) Level shifting 0.6V to 0.9V, (d) Level shifting 1.2V to 0.9V.

The delay analysis has done using the transition time of 0.2ns. The load capacitance is varied in the range of 0.365fF to 50fF and the input voltage also varied from 0.2V to 1.2V. The result is shown in Figure 7.




(a)

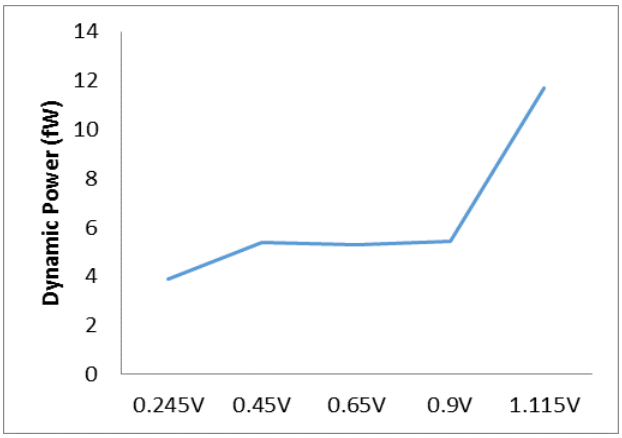



(b)

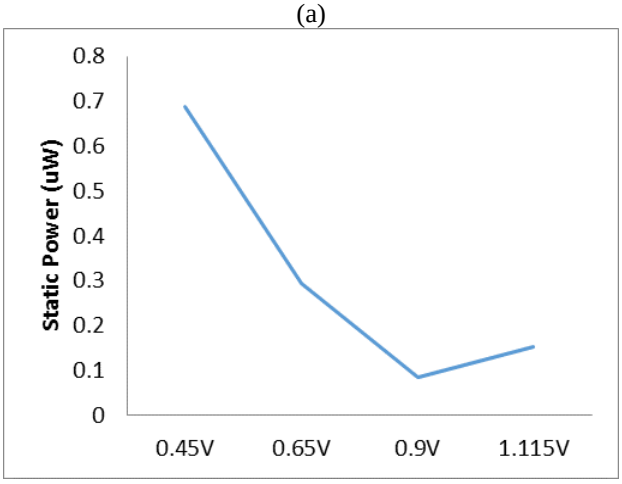
**Figure 7:** (a) Rise delay, (b) Fall delay

It can be observed from the graph that the delay of the cell is minimum at the nominal operating voltages. It is also observed that the transition time of the input signal affect delay significantly only when it is more than 1ns, so effect of transition time is not considered.

Similarly we have power analysis for the ELS. The power analysis is done using standard load capacitance of 7.5fF and transition time of 9.2ns. The power consumption data of the proposed ELS can be seen in Figure 8. The static and dynamic power consumption is least in the normal operating voltages.




(a)




(b)

**Figure8:** (a) Dynamic power consumption, (b) Static power consumption.

## 5. Conclusions

We have presented new ELS suitable for robust logic voltage shifting from near/sub-threshold to above threshold domain and isolating the shutdown region from the active region. The proposed ELS is designed for wide range of operating voltages. The circuit exploits the strategy to give the wide operating voltage at delay values less than 0.5ns at nominal operating voltage. It is also optimized for low power consumption, dynamic power consumption is 5fF and the static power consumption is near 100nW.

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