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Comparison of the Traditional VSI & CSI with Novel ZSI for Study the Pre-Dominate Harmonics Effect

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Abstract: ***This paper presents an Impedance Source Inverter for A.C electrical drives. The impedance source inverter employs a unique combination of inductor and capacitor impedance network couple with inverter main circuit and rectifier. By controlling the short circuit provide through duty cycle, voltage, current and the impedance source inverter systems using IGBT provide ride-through capability during voltage sags, reduces line harmonics, buck-boost the voltage, high reliability, and extends output voltage range. Analysis, simulation, and experimental results will be presented to demonstrate these new features. It reduces pre-dominate harmonics, electromagnetic interference noise and it has low common made noise. MATLAB simulations have been performed to analyses these issues.***

Keywords: pre-dominant harmonics, motor drives, Z-source inverter

1. Introduction

Traditional voltage source inverter (VSI) and current source inverter (CSI) are commonly used in many power electronic applications. Recently, a Z-source inverter is introduced as a new topology of power electronic converters. The ZSI is a buck-boost inverter that has special features which cannot be observed in the traditional inverters. The power source. The unique feature of the Z-source

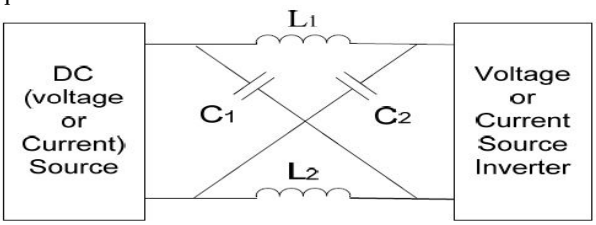


Figure 1: General structure of Z-source converter

Inverter is that its output voltage can theoretically be changed between zero and infinity. The main circuit of the Z-source and its operating principle has been described in. A comparison between three types of inverters: traditional PWM inverter, dc/dc boosted PWM inverter and Z-source inverter for fuel cell vehicles are investigated in [2]. The control methods, to obtain a maximum voltage gain and to minimize the voltage stress across the inverter for any desired voltage gain have been described in [3]. Application of Z-source inverter for adjustable speed drives by controlling the boost factor is presented in [4,5] .This paper presents a pre dominate harmonic analysis of symmetrical Z-source inverter.

2. Circuit topology and operating states of a three-phase ZSI

Fig-2 shows the topology of the three phase Z-source inverter, where the impedance network is placed between the power source and the inverter.

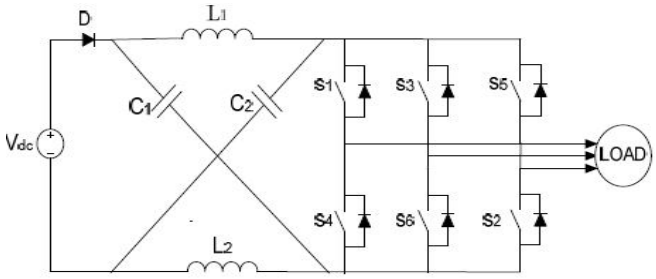


Figure 2: A three phase Z-source converter

As shown in table. I, a three phase Z-source inverter has nine possible switching states: six active states (vectors) when the dc voltage is impressed across the load, two zero states (vectors) when the load terminals are shorted through either the lower or the upper three switches and one shoot through state (vector) when the load terminals are shorted through both the upper and the lower switches of any one leg or two legs or all three legs. These switching states and their combinations introduce a new PWM method for the Z-source inverter.

Table 1: Switching states of a three phase ZSI

Switching states	S1	S4	S3	S6	S5	S2
Active states	1	0	0	1	0	1
	1	0	1	0	1	0
	0	1	1	0	0	1
	0	1	1	0	1	0
	0	1	0	1	1	0
	1	0	0	1	1	0
Zero states	1	0	0	1	0	1
	1	0	1	0	1	0
Shoot through states	1	1	S3	$\overline{s3}$	S5	$\overline{s5}$
	S1	$\overline{s1}$	1	1	S5	$\overline{s5}$
	S1	$\overline{s1}$	S3	$\overline{s3}$	1	1
	1	1	1	1	S5	$\overline{s5}$
	1	1	S3	$\overline{s3}$	1	1
	S1	$\overline{s1}$	1	1	1	1
	1	1	1	1	1	1

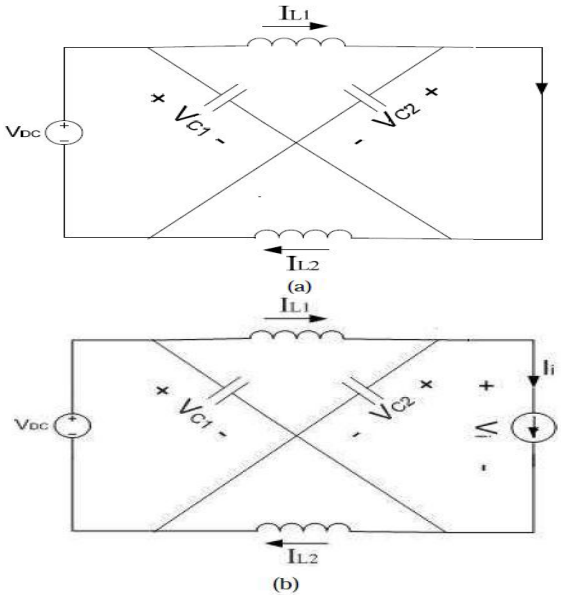


Figure 3: Operating modes of a Z-source inverter (a) shoot-through zero state (b) non shoot through states

Fig.3.a shows a shoot through switching state of the Z-source inverter where two switches of one leg or two legs or all three legs are turned on simultaneously. In this state, the diode D at input side is reverse biased and the capacitors, C1 and C2 charge the inductors, L1 and L2 and the voltage across the inductors are:
Assume the inductors (L1&L2) and capacitors (C1 &C2) have the same inductance and capacitance values respectively. From the above equivalent circuit

$V_{c1} = V_{c2} = V_c$ .....eqn (2.1)
$V_{L1} = V_{L2} = V_L$ .....eqn (2.2)
$V_L = V_c$, $V_d = 2V_c$ $V_i = 0$;

During the switching cycle T
$V_L = V_o - V_c$ .....eqn (2.3)
$V_d = V_o$
$V_i = V_c - V_L$ ($V_o = V_L - V_C$)
$V_i = 2V_c - V_o$.....eqn (2.4)
Where Vo is the dc source voltage and
$T = To + T_1$ ..... eqn (2.5)
The average voltage of the inductors over one switching period (T) should be zero in steady state
$V_L = V_L = T_o . V_c + T_1(V_o - V_c)/T = 0$
$V_L = (T_o . V_c + V_o . T_1 - V_c . T_1)/T = 0$
$V_L = (T_o - T_c)V_c/T + (T_1 . V_o)/T$
$V_c/V_o = T_1/T_1 - T_0$ .....eqn (2.6)

Similarly the average dc link voltage across the inverter bridge can be found as follows.

From equation 2.4
$Vi = Vi = (To.0 + T_1.(2Vc - Vo))/T$ ..eqn (2.7)
$Vi = (2Vc. T_1/T) - (T_1 Vo/T)$
$2Vc = Vo$
From equation 2.6
$T_1.Vo/(T_1 - To) = 2Vc. T_1/(T_1 - To)$
$Vc = Vo. T_1/(T_1 - To)$
The peak dc-link voltage across the inverter bridge is
$Vi = Vc - Vl = 2Vc - Vo$
$= T/(T_1 - To).Vo = B.Vo$
Where $B = T/(T_1 - To)$ i.e 1 .....eqn (2.8)
B *is a boost factor*

The output peak phase voltage from the inverter
$Vac = M.vi/2$ .....eqn (2.9)

Where M is the modulation index In this source
$Vac = M.B.Vo/2$ ....eqn (2.10)

In the traditional sources
Vac = M.Vo/2

For Z-Source inverter output voltage is as given below
Vac = M.B.Vo/2

The output voltage can be stepped up and down by choosing an appropriate buck – boost factor B_B
$B_B = B.M$ (it varies from 0 to) .....eqn (2.11)

The capacitor voltage can be expressed as
Vc1=Vc2=Vc=(1-To/T).Vo/(1-2To/T)

The boost factor B_B is determined by the modulation index M and the boost factor B. The boost factor B can be controlled by duty cycle of the shoot through zero state over the non-shoot through states of the PWM inverter. The shoot through zero state does not affect PWM control of the inverter. Because it equivalently produce the same zero voltage to the load terminal. The available shoot through period is limited by the zero state periods that are determined by the modulation index.

2.1Simulation results of the VSI, CSI and ZSI. Harmonic Order of the Frequency Spectrum

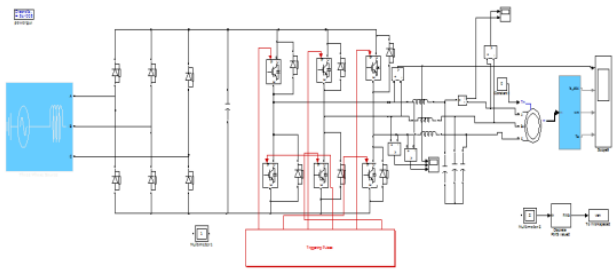
Let FN=**Fc/Fsine**
Where **n=jFN±K** Fc=carrier wave
Where j=1, 3, 4……. For K=2, 4, 6…….
J=2, 4, 6……For K=1, 3, 5……Such that '**n**' is not a multiple of 3.Their for line to line there are no 3rd order harmonics eliminated.

If FN=30 j=1. k=2, 4….
F of harmonic = **30 Fsine±2 Fsine**
30 Fsine±4 Fsine.
Here **j=2 k=1,3 60 Fsine±1 Fsine**
60Fsine±3 Fsine

There are **4 harmonics** i.e **28 Fsine,32 Fsine** and **59 Fsine,61 Fsine**
Harmonic order is **= j Fc ± K Fm**
Fm is α to our reference amplitude
j=even value k=odd value
i.e. j=odd value k=even value

To shift Fc to high frequency side we have to increase the frequency of the regular wave. If Fc is increases the number of switching per fundamental cycle will increase. Switching losses will increases. Efficiency of the power converter will decreases .Disadvantage of the six-step current waveform such as harmonic heating, torque pulsation and acoustic noise, can be significantly reduced by PWM wave shaping of the inverter's current wave. The PWM current wave with

reduced harmonics content are further filtered by the commutating capacitor bank to make the machine current nearly sinusoidal PWM.



Traditional PWM Voltage Source Inverter for Motor Drive

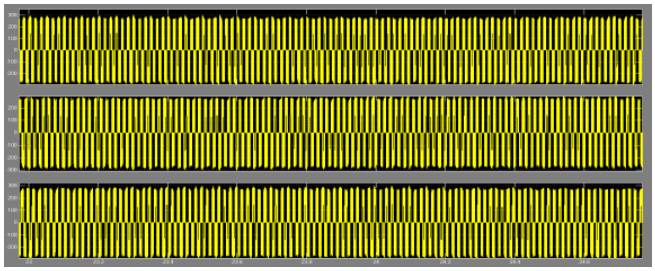


Figure 4: Inverter line-line voltage waveforms

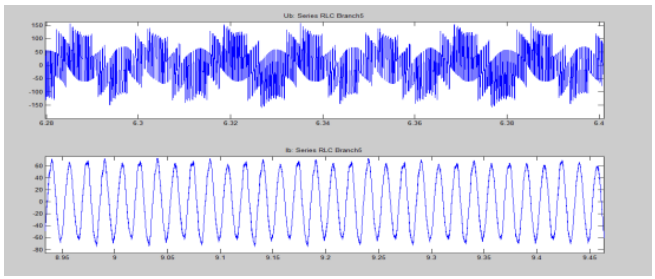


Figure 5: Inverter phase voltage and current waveform

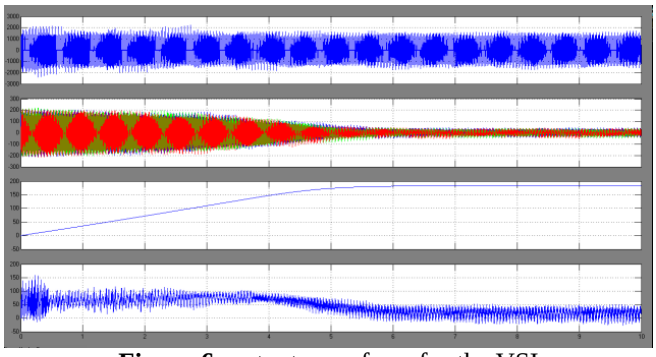


Figure 6: output waveform for the VSI

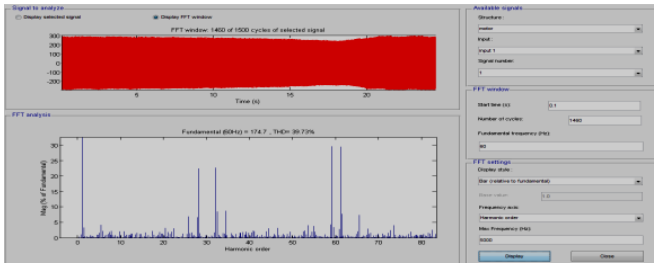


Figure 7: Voltage waveform THD 39.73%

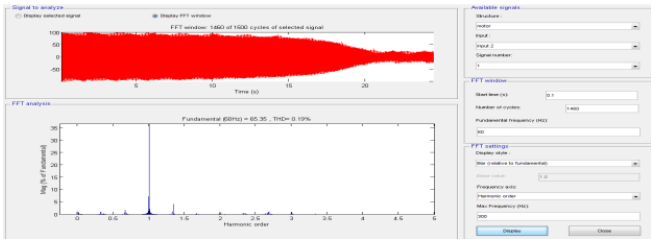
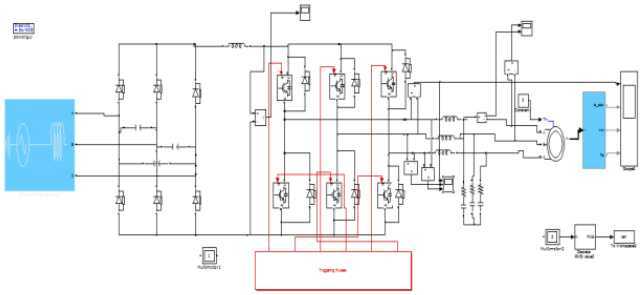


Fig 8 current waveform THD is 0.19%



Traditional PWM Current Source Inverter for Motor Drive

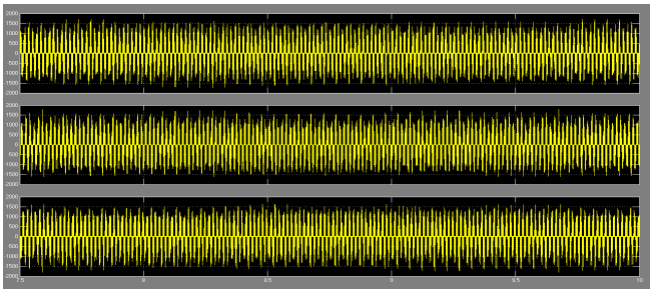


Figure 9: Inverter line-line voltage waveforms.

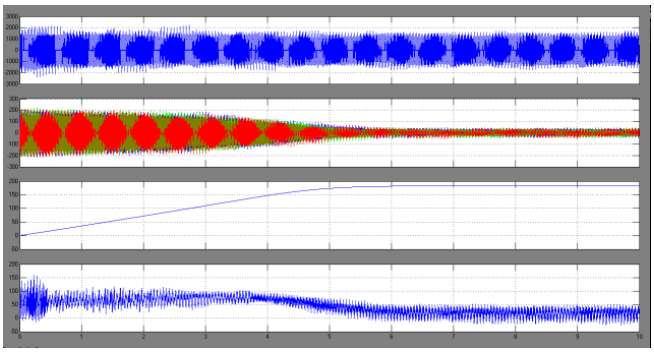


Figure 10: output waveform for the CSI

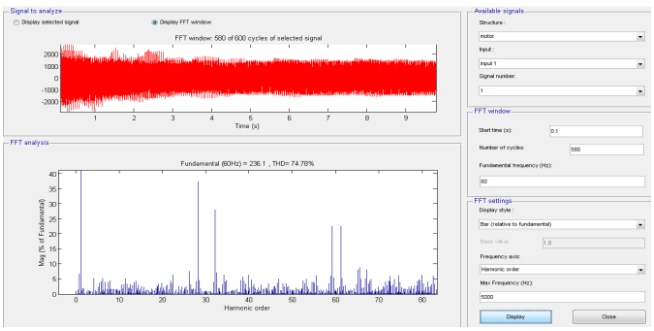


Figure 11: voltage waveform THD 74.78%

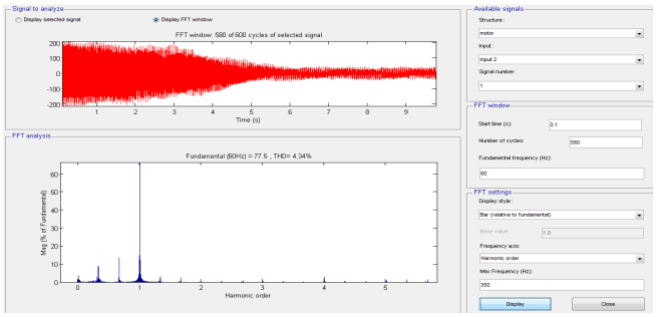


Figure 12: current waveform THD 4.34%

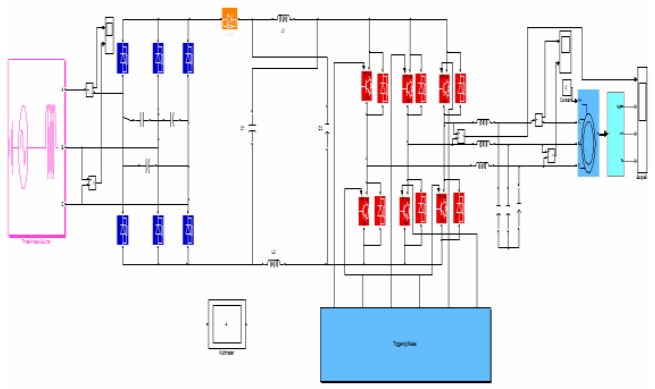


Figure 13: simulation of the Z-source inverter

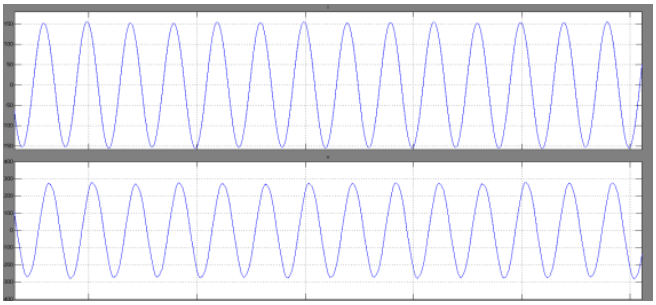


Figure 14: input voltage and current waveforms

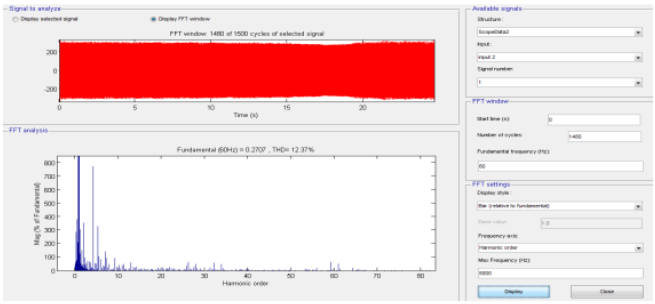


Figure 15: voltage waveform THD 12.37%

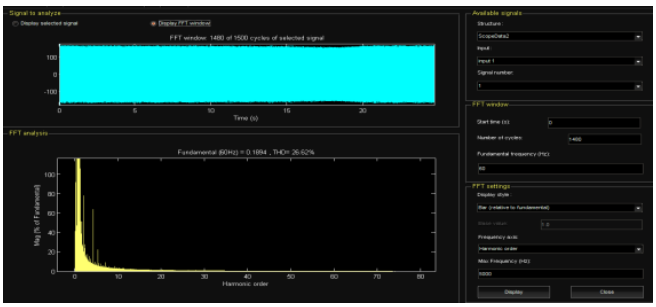


Figure 16: current waveform THD 26.62%

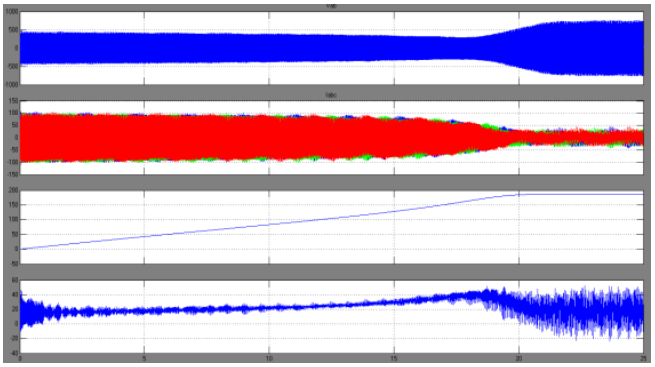


Figure 17: output wave form for the motor.

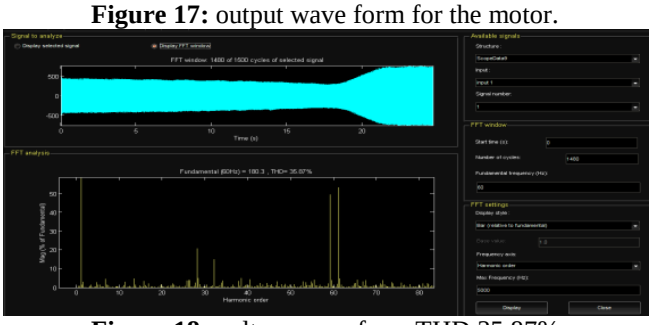


Figure 18: voltage waveform THD 35.87%

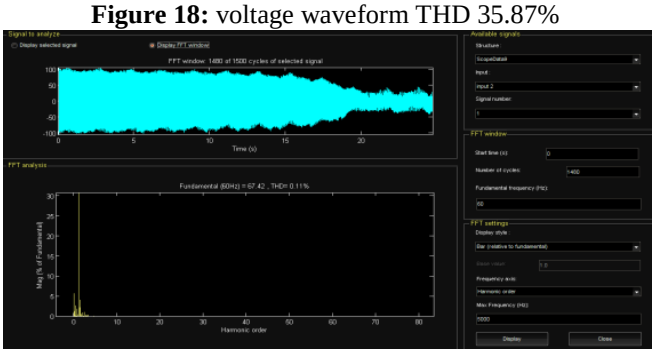


Figure 19: current waveform THD 0.11%

Table for the Total Harmonic distortion of the inverters VSI, CSI and ZSI

Harmonic order (6N±1)	VSI THD 39.73%	CSI THD 74.78%	ZSI THD 35.60%
5th	1.74%	1.52%	1.40%
7th	1.33%	1.70%	1.54%
11th	0.68%	3.37%	0.46%
13th	0.35%	3.11%	0.32%
Predominate harmonics order(FN=JFsin±KFsin)	VSI	CSI	ZSI
28th	22.40%	37.48%	20.00%
32nd	22.67%	28.09%	15.15%
59th	16.06%	22.68%	15.04%
61st	16.13%	22.72%	7.97%

3. Conclusions

Following common limitations and problems in VSI and CSI.

1. Obtainable output voltage is limited quite below the input line voltage.
2. Inrush and harmonic current from the diode rectifier can pollute the line.

Performance and reliability are compromised by the V-source inverter structure, because 1) miss-gating from EMI can cause short circuit-through that leads to destruction of the inverter, 2) the dead time that is needed to avoid short

circuit -through creates distortion and unstable operation at low speeds, and 3) common-mode voltage causes shaft current and premature failures of the motor. the Z-source inverter [7],has a niche for ASD systems to overcome the aforementioned problems [5].
A Z-source inverter based ASD system can:

1) Produce any desired output ac voltage, even greater than the line voltage, regardless of the input voltage, thus reducing motor ratings;
2) Provide ride-through during voltage sags without any additional circuits; 3) Reduce the harmonic current and common-mode voltage. The control method has been verified by simulation and experiments.

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