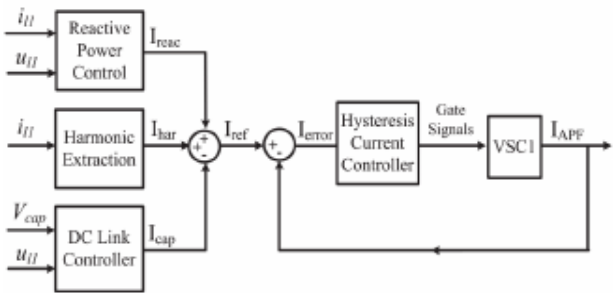

Figure 5. The control algorithm of Shunt Compensator

Shunt Compensator control system measures the load voltages (u_{l1}), dc capacitor voltage (V_{cap}), load currents (i_{l1}) and injected currents (I_{APF}). The controller processes the measured values and generates the required compensation signals. These signals are then compared in hysteresis controller and the required gate signals are generated.

When the distorted current or voltage signal is applied to EPLL, the harmonics and interharmonics of distorted signal (I_{har}) can be obtained from the *e(t)* signal of EPLL. DC link voltage control is achieved by using PI controller. The input of the PI controller is the error between the actual capacitor voltage V_{cap} and its reference value $V_{cap,ref}$. In order to keep DC link voltage at a constant level, shunt compensator must draw active power by drawing current (I_{cap}) in phase with line voltage. To draw a current in the same phase with system voltage, phase information of system voltage ($j_{Vload)}$ must be known. This can be achieved by using EPLL. With using phase of system voltage, DC link control reference current signal is created by multiplying the PI controller output and sine wave created by phase information of system voltage. The block diagram of reactive power control used in control method of Shunt Compensator module (VSC1) is shown in Fig. 6 [15]. Two identical EPLL units are used for voltage and current signals. The top portion of the unit is used for voltage and the bottom portion is used for current signal processing. The link between the two parts is to calculate the fundamental reactive current component (I_{reac}).

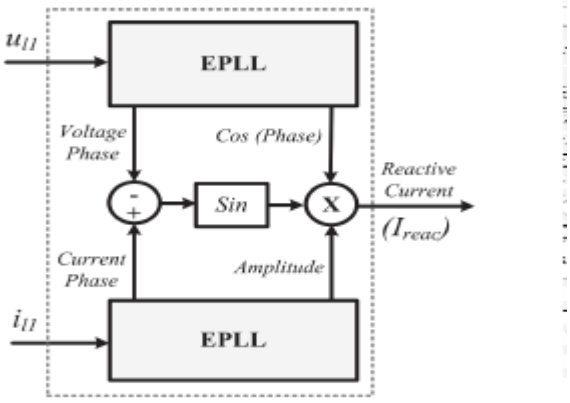

Figure 6. Block diagram of the proposed reactive-current extraction unit

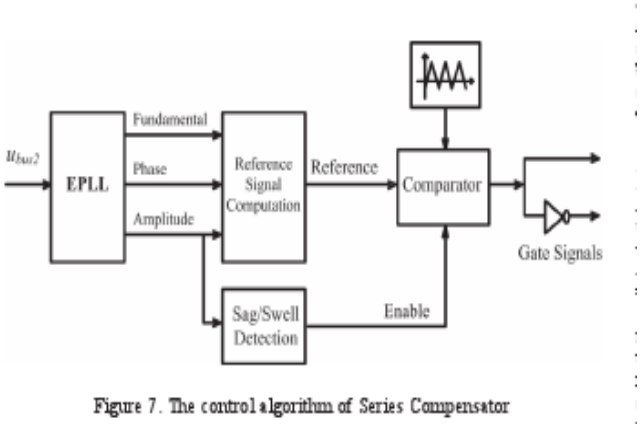

Figure 7. The control algorithm of Series Compensator

The main aim of the series VSC (VSC2) is to mitigate voltage sag/swell and interruption in Feeder-2. The control system of series compensator consists of sag/swell detection, reference voltage extraction and gate signal generation as shown in Fig. 7.

Simple and effective control algorithm is proposed for both sag/swell detection and reference voltage generation in this paper. The algorithm is based on the EPLL that extracts and directly provides the amplitude *A(t)*, phase angle *ş(t)* and fundamental component *A(t) cosş(t)* of the input signal for each phase independently. With the proposed method, the controller is able to detect balanced, unbalanced and single phase voltage sags/swells without an error. In this method, three EPLLs are used to track each of the three phases.

In the EPLL, the measured phase supply voltages are converted to per unit value. *A(t)* gives the amplitude of the tracked signal *u(t)*. If there is no sag or swell, *A(t)* signal is obtained as continuous 1 pu. By subtracting the *A(t)* signal from the ideal voltage magnitude (1 pu), the voltage sag/swell depth (S_{depth}) can be detected. The comparison of this value with the limit value of 10% (0.1 pu) gives information whether a fault occurred or not [16]. The voltage sag/swell detection based on EPLL method is presented in Fig. 8.

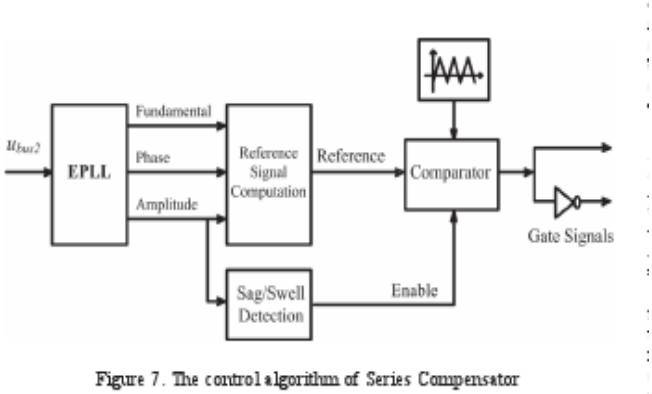

Figure 7. The control algorithm of Series Compensator

Reference voltage V_{error} is calculated according to voltage injection strategy by using magnitude *A(t)*, the output *y(t)* and Compensation method is used as voltage injection strategy. Pre-Sag Compensation (PSC) method tracks supply voltage continuously and if it detects any disturbances in supply voltage it will inject the difference voltage ($V_{error, presage)}$ between the sag or voltage at point common coupling

(PCC) and pre-fault condition, so that the load voltage can be restored back to the pre-fault condition.

If sag is accompanied by a phase jump, PSC method offers better performance by compensating voltage sags in the both phase angle and amplitude for sensitive loads [17]. Other voltage injection strategies such as in-phase, phase-advance and minimum energy injection compensation methods may not prevent the phase jump of the load voltage at the starting and ending instants of the sag compensation period [18].

PWM switching method is used as gate signal generation for series converter. The switching pulses are generated by comparing the reference voltage compensation signal V_{error} with a fixed frequency carrier triangular wave.

3.Simulation Results

The proposed IUPQC and its control schemes are tested through extensive case study simulations. In this section, simulation results obtained by PSCAD/EMTDC are presented, and the performance of the proposed IUPQC is analyzed. The system parameters of IUPQC system are provided in Table 1 and EPLL parameters are given in Table 2.

Table 1: System Parameters

System Parameters	Values
Fundamental Frequency (*f*)	50 Hz
Voltage Source (u_{s1})	11 kV (L-L, rms), phase angle 0°
Voltage Source (u_{s2})	11 kV (L-L, rms), phase angle 0°
Feeder-1 (R_{s1}+*j2vfL*$_{s1}$)	Impedance: 0,0015+j0,0785 ö
Feeder-2 (R_{s2}+*j2vfL*$_{s2}$)	Impedance: 0,0015+j0,0785 ö
Nonlinear Load (*L1*)	A three-phase diode bridge recti¿er that supplies a load of 100+j125.66 ö
Sensitive/Critical Load (*L2*)	150.0+j23.56 ö
DC Link Capacitor (C_{dc})	40 mF
DC Capacitor Voltage (V_{cap})	1700 V
Coupling Transformer (TR1)	2 MVA, 11/1 kV å/Y, Uk: 5%
Injection Transformer (TR2)	2 MVA, 1.2/8.0 kV, 10% Leakage reaktance
Power Transformer (TR3)	2 MVA, 11/6.3 kV å/ å, Uk: 10%

Table 2: EPLL Parameters

Parameters	Values
Integral Time Constant	0.02 s
K_A	500
K_i	30
Kp	300

A. Harmonic Distortion on Feeder-1

This case presents how VSC1 overcomes the load current harmonics with the proposed control algorithms. A three-phase diode bridge recti¿er is used as a harmonic current producing load. The nonlinear load contains lower and higher order harmonics with a total value of 25.08% THD before compensation. VSC1 eliminates the load current harmonics by injecting current that cancel harmonic currents of nonlinear load as shown in Fig. 9. The waveforms indicate the nonlinear load current (I_{l1}), its corresponding compensation current injected by VSC1 (i_{pf}), compensated Feeder-I current (i_{S1}) and the dc link capacitor voltage (V_{cap}) of Phase-A respectively. The results show that a successful reduction in harmonics of the nonlinear load current (i_{l1}) is obtained. A nonlinear load current with 25.08% THD is reduced to less than 5%. The PI controlled dc-link capacitor voltage is nearly kept at 1.7 kV.

B. Voltage Sag on Feeder-2

In this case, single line-to-ground unbalanced fault is considered, since it is most likely to occur in 70% of among all voltage sags in a distribution system [16]. 35% Single line-to-ground fault with 47.64o phase angle jump is investigated which occurs on Phase-A of BUS2 voltage between 0.3 s < t < 0.5 s. The sensitive/critical load (L2) voltage is not affected by voltage sag with the help of series compensator (VSC2). Fig. 10 shows the BUS2 voltage (u_{bus2}), series compensating voltage (u_{SE}), L2 load voltage (u_{l2}) and dc link capacitor voltage (V_{cap}).

C. Upstream Fault on Feeder-2

In this case study, the performance of VSC2 for upstream fault (interruption) mitigation on Feeder-2 is investigated. Single phase (L-G) interruption occurs on Phase- A of BUS2 voltage between 0.6 s < t < 0.8 s, and 25.27° phase angle jump occurs during the interruption. The sensitive/critical load (L2) voltage is not affected by voltage sag with the help of series compensator (VSC2). Fig. 11 shows the BUS2 voltage (u_{bus2}), series compensating voltage (u_{SE}) and L2 load voltage (u_{l2}) and the dc link capacitor voltage (V_{cap}).

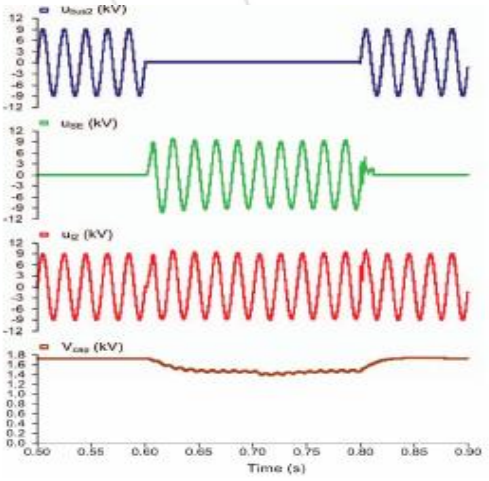

Figure 11. BUS2 voltage, series compensating voltage, load (L2) voltage and dc link capacitor voltage for Case C

4.Conclusion

In this paper, an improved IUPQC topology for simultaneous compensation of voltage and current in adjacent feeders has been proposed. An effective EPLL based control technique is used for IUPQC to detect and extract the PQ disturbances in multi-feeder system. Each phases of Series and Shunt Compensator are investigated independently with EPLL based controller. The performance of proposed IUPQC system is evaluated through extensive simulations for mitigating harmonics, unbalanced voltage sags with phase jumps and interruptions. The results of simulations show its effectiveness in handling these PQ issues, so that smooth and clean power flow to the loadsREFERENCES

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Author Profile

CH Rajender has obtained his b.tech degree from JNTU PULIVENDULA in 2010. Currently persuing M.tech power electronics in Sri Venkateshwara engineering college, Suryapet.

Dr. A. Srujana has obtained her B. Tech degree from KITS, Warangal, in 1998 and M. Tech degree From J.N.T.U Hyderabad, India, in 2002.She Has obtained her Ph.D from J.N.T.U , Hyderabad in 2011. She has 18 years of teaching experience. Presently She is working as Professor & Principal at Sri Venkateswara Engineering College, Suryapet